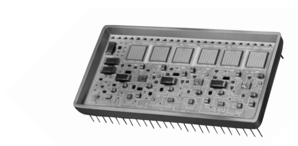


SMART POWER 3-PHASE MOTOR DRIVE

DESCRIPTION

The PWR-82330 is a smart Power 3-phase Motor Drive Hybrid. The PWR-82330 uses a MOSFET output stage with a 100 Vdc rating, and can deliver 5 A continuous, 10 A peak current to the load.

This new Smart Power Motor Drive has CMOS Schmitt trigger inputs for high noise immunity. High and low-side input logic signals are XOR'd in each phase to prevent simultaneous turn on of in-line transistors, thus eliminating a shoot through condition.

The internal logic controls the high and low-side gate drivers for each phase and can operate from +5 to +15 V logic levels. The internal charge pump circuitry provides the required voltage to high-side gate drives. This provides constant output performance for switching frequencies from dc to 50 kHz.

APPLICATIONS

Packaged in a small case, these hybrids are an excellent choice for high performance, high-reliability motor drives for Military and Aerospace servo-amps and speed controls.

Among the many applications are robotics; electro-mechanical valve assemblies; actuator systems; antenna and radar positioning; fan and blower motors for environmental conditioning; position control of mini-subs, drones, and RPV's; and compressor motors for cryogenic coolers.

The PWR-82330 hybrid is ideal for harsh military environments where shock, vibration, and temperature extremes are evident, such as missile applications including fin actuators and I.R. seeker head movement. The PWR-82330 operates over the -55°C to +125°C temperature range and is available with military processing.

FEATURES

- ***Small size (2.6" x 1.4" x 0.25")***
- ***100 Vdc Rating***
- ***5 A Continuous, 10 A peak Capability***
- ***High-Efficiency MOSFET Drive Stage***
- ***Direct Drive from Commutation Logic***
- ***Six Step Trapezoidal or Sinusoidal Drive***
- ***Four Quadrant Operation***
- ***Military Processing Available***

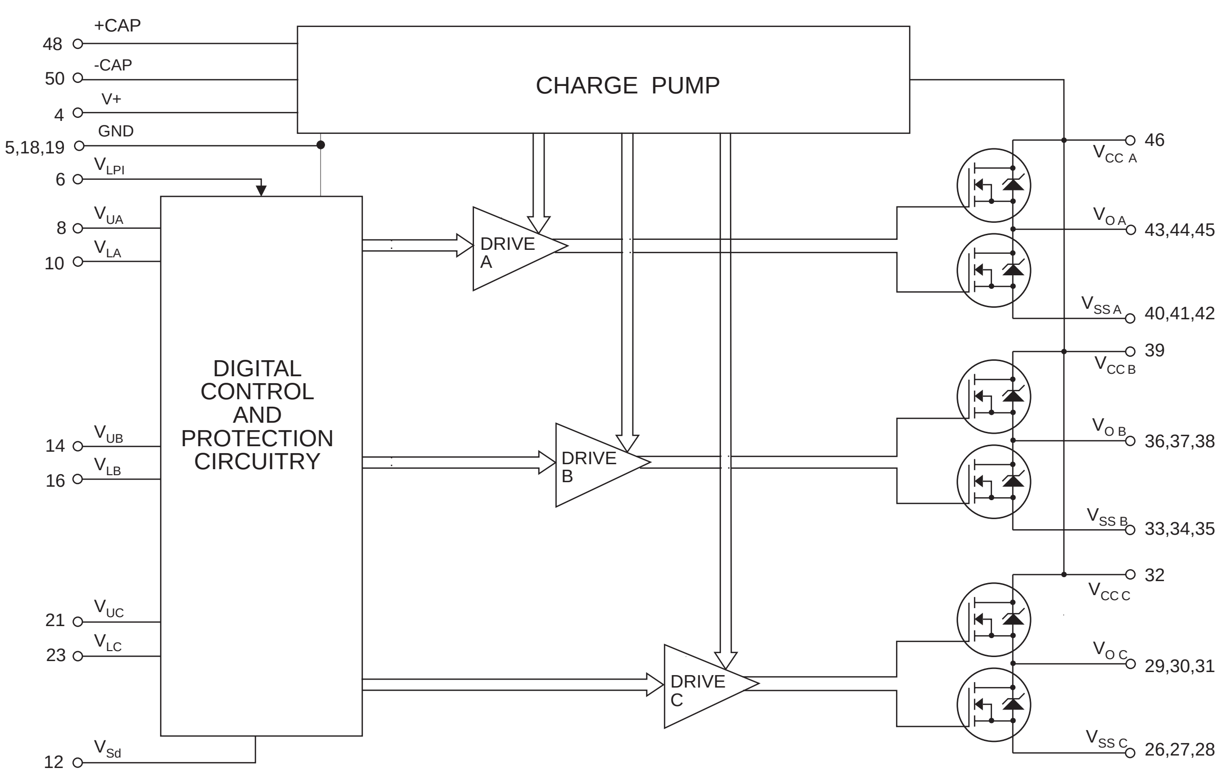


FIGURE 1. PWR-82330 BLOCK DIAGRAM

NOTES

TABLE 1. PWR-82330 ABSOLUTE MAXIMUM RATINGS (Tc = +25°C Unless Otherwise Specified)			
PARAMETER	**SYMBOL**	**VALUE**	**UNITS**
SUPPLY VOLTAGE	V_{CC}	100	V
INPUT VOLTAGE	V+	18	V
LOGIC POWER-IN VOLTAGE	V_{LPI}	18	V
INPUT LOGIC VOLTAGE	V_U, V_L, VSd	V_{LPI} + 0.5	V
OUTPUT CURRENT			
CONTINUOUS	I_O	5	A
PEAK	I_P	10	A
OPERATING FREQUENCY	f_O	50	kHz
CASE OPERATING TEMPERATURE	T_C	-55 to +125	°C
CASE STORAGE TEMPERATURE RANGE	T_{CS}	-55 to +150	°C

TABLE 2. PWR-82330 SPECIFICATIONS (T_C=+25°C Unless Otherwise Specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
OUTPUT						
Output Current Continuous	I_O				5	A
Supply Voltage	V_{CC}	see note 1		28	100	V
Output On-Resistance (each FET)	R_{ON}	Ip=5A (see note 2)			0.13	Ω
Instant Forward Voltage (intrinsic diode)	V_F	Ip=5A (see note 2)			1.25	V
Reverse Recovery Time (intrinsic diode)	trr	Id=1A, di_d/dt=160A/µs		160	500	nsec
Reverse Leakage Current	Ir	see note 3			250	µA
INPUT POWER						
Input Voltage (T_C=-55°C to +125°C)	V+		12	15	18	V
Logic Power-in Voltage	V_{LPI}		5		18	V
V+ Current	I+	V+ = 15V			150	mA
Logic Power Input Current	I_{LPI}	V_{LPI} = 15 V			5	mA
INPUT SIGNALS (See Figure 3)		**Pin Connections**				
Positive Trigger Threshold Voltage	V_P	V_{LPI} = 15 V			12.9	V
Negative Trigger Threshold Voltage	V_N	V_{LPI} = 15 V	2.1			V
Hysteresis Voltage	V_H	V_{LPI} = 15 V	1.6		10.8	V
Positive Trigger Threshold Voltage	V_P	V_{LPI} = 5 V			4.3	V
Negative Trigger Threshold Voltage	V_N	V_{LPI} = 5 V	0.9			V
Hysteresis Voltage	V_H	V_{LPI} = 5 V	0.3		3.6	V
SWITCHING CHARACTERISTICS		**Test 1 Conditions**				
(see FIGURE 2)		V_{LPI} = 15 V				
Upper Drive:		V+ = 15 V				
Turn-on Propagation Delay	td(on)	V_{CC} = +28 V			825	nsec
Turn-off Propagation Delay	td(off)	I_p = 10 A			1100	nsec
Shut-down Propagation Delay (see FIGURE 5)	tsd				1000	nsec
Turn-on Rise Time	tr				125	nsec
Turn-off Fall Time	tf				200	nsec
Lower Drive:						
Turn-on Propagation Delay	td(on)				825	nsec
Turn-off Propagation Delay	td(off)				1100	nsec
Shut-down Propagation Delay (see FIGURE 5)	tsd				1000	nsec
Turn-on Rise Time	tr				200	nsec
Turn-off Fall Time	tf				200	nsec
SWITCHING CHARACTERISTICS		**Test 2 Conditions**				
(see FIGURE 2)		V_{LPI} = 5 V				
Upper Drive:		V+ = 15 V				
Turn-on Propagation Delay	td(on)	V_{CC} = +28 V			1150	nsec
Turn-off Propagation Delay	td(off)	I_p = 10 A			1400	nsec
Shut-down Propagation Delay (see FIGURE 5)	tsd				1050	nsec
Turn-on Rise Time	tr				125	nsec
Turn-off Fall Time	tf				225	nsec

TABLE 2. PWR-82330 SPECIFICATIONS (continued) (T_C= +25°C Unless Otherwise Specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
SWITCHING CHARACTERISTICS (continued)		**Test 2 Conditions**				
		V_{LPI} = 5 V				
Lower Drive:		V+ = 15 V				
Turn-on Propagation Delay	td(on)	V_{CC} = +28 V			1150	nsec
Turn-off Propagation Delay	td(off)	Ip = 10 A			1400	nsec
Shut-down Propagation Delay (see FIGURE 5.)	tsd				1050	nsec
Turn-on Rise Time	tr				125	nsec
Turn-off Fall Time	tf				225	nsec
DEAD TIME	t_{dt}		400			nsec
MINIMUM PULSE WIDTH	t_{pw}		150			nsec
THERMAL						
Maximum thermal Resistance	θjc				7.5	°C/W
Junction Temperature Range	Tj	each transistor	-55		150	°C
Case Operating Temperature	T_{CO}		-55		125	°C
Case Storage Temperature	T_{CS}		-55		150	°C
WEIGHT					1.37 (39)	0z (g)

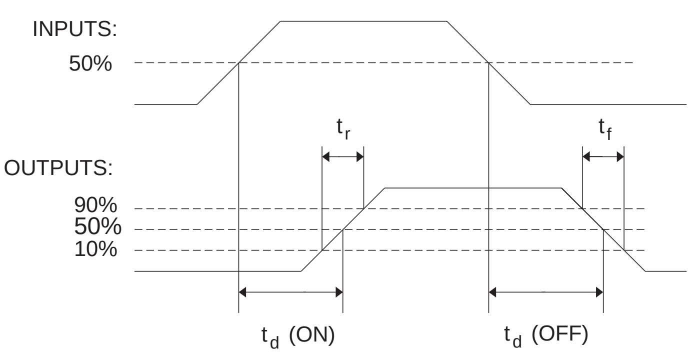
NOTES:

1. For Hi-Rel applications, derating per MIL-S-19500 should be observed. (Derate V_{CC} by 70%.)
2. Pulse Width ≤ 300 µs, duty cycle ≤ 2%
3. V_{CC} = 70 V, V_U, V_L, = logic '0'

INTRODUCTION

The 3-phase PWR-82330 is a 5 A motor drive hybrid which incorporates a 100 Vdc MOSFET output stage for high-speed and high-efficiency operation. This motor drive is ideal for use in high-performance motion control systems, servo amplifiers, and motor speed control designs. Furthermore, Multi-axis systems requiring multiple drive stages can benefit from the small size of this power drive.

The PWR-82330 can be driven directly from commutation logic, DSP, or a custom ASIC that supplies digital signals to control the upper and lower transistors of each phase. This highly integrated drive stage has schmitt trigger digital inputs that control the high and low side of each phase. Digital protection of each phase eliminates an in-line firing condition, by preventing simultaneous turn-on of both the upper and lower transistors. The logic controls the high and low-side gate drivers. Operation from 5 to 15 V logic levels can be programmed by applying the appropriate voltage to pin 6 (V_{LPI}). The PWR-82330 has a ground referenced low-side gate drive. An internal charge pump circuit supplies the required drive voltage to each of the three high-side transistors. This provides a continuous high-side gate drive even during a motor stall. The high and low-side gate drivers control the N-channel MOSFET output stage. The MOSFETs used in the PWR-82330 allow output switching up to 50 kHz. The PWR-82330 does not have an internal short-circuit or overcurrent protection, which if required, must be added externally to the hybrid.



(REFERENCE TABLE 2. ALSO)

FIGURE 2. INPUT/OUTPUT TIMING RELATIONSHIPS

DIGITALLY CONTROLLED INPUTS

The PWR-82330 uses the Schmitt triggered digital inputs (with hysteresis) to ensure high noise immunity. The trigger switches at different points for positive and negative going signals. Hysteresis voltage (V_H) is the difference between the positive going voltage (V_P) and the negative going voltage (V_N) (see FIGURE 3). The digital inputs have programmable logic levels, which allows the hybrid to be used with different types of commutation logic with an input voltage range of 5-15 V, such as TTL or CMOS logic. Pin 6 is the logic power input (V_{LPI}) for the digital circuitry inside the hybrid. **A 0.01 µF, 50 V ceramic capacitor must be placed between this pin (6) and GND as close to the hybrid as possible.** When using 15 V control circuitry, an external +15 Vdc power supply must be connected between pin 6 of the hybrid, and GND. The commutation / control circuitry can be as simple as discrete logic with PWM, or as sophisticated as a microprocessor or custom ASIC, depending on the system requirements. FIGURE 4 illustrates a typical interface of the PWR-82330 with a motor and commutation logic in a Servo-Amp System. (Refer to AN/H-3 application note for more details.)

SHUT-DOWN INPUT (VSd)

Pin 12 (Vsd) provides a digital shut-down input, which allows the user to completely turn-off both the upper and lower-output transistors in all 3 phases. Application of a logic '1' to the VSd input will latch the Digital Control / Protection circuitry thereby turning off all output transistors. The Digital Control/Protection circuitry remains latched in the off state and will not respond to signals on the V_L or V_U inputs while the VSd has a logic '1' applied. When the user or the sense circuitry (as in FIGURE 6) returns the VSd input to a logic '0', and then the user sets the V_L and V_U inputs to a logic '0' the output of the Digital Control / Protection circuitry will clear the internal latch. When the next rising edge (see FIGURE 5) occurs on the V_L or V_U digital inputs, the outputs transistors will respond to the corresponding digital input. This feature can be used with external current limit or temperature sense circuitry to disable the drive if a fault condition occurs (see FIGURE 6).

INTERNAL PROTECTION CIRCUITRY

The hybrid contains digital protection circuitry, which prevents in-line transistors from conducting simultaneously. This, in effect, would short circuit the power supply and would damage the output stage of the hybrid. The circuitry allows only proper input signal patterns to cause output conduction. TABLE 3 lists the input/output timing relationships. If an improper input requested that the upper and lower transistors of the same phase conduct together, the output would be a high impedance until removal of the illegal code from the input of the PWR-82330. **A dead time of 400 nsec minimum should still be maintained between**

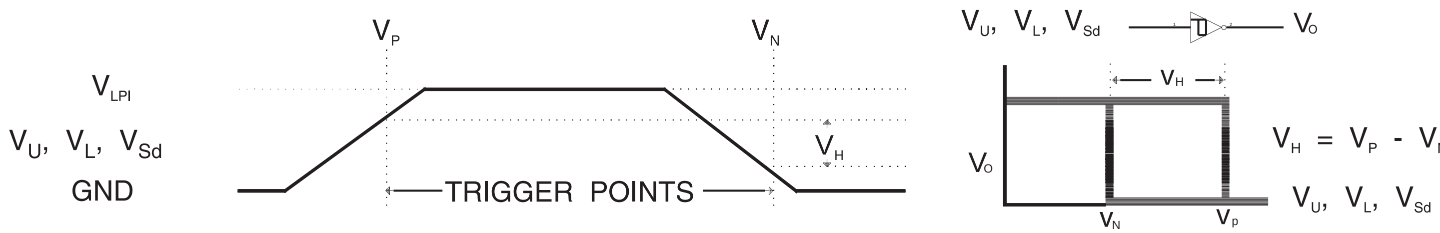


FIGURE 3. HYSTERESIS DEFINITION AND CHARACTERISTICS

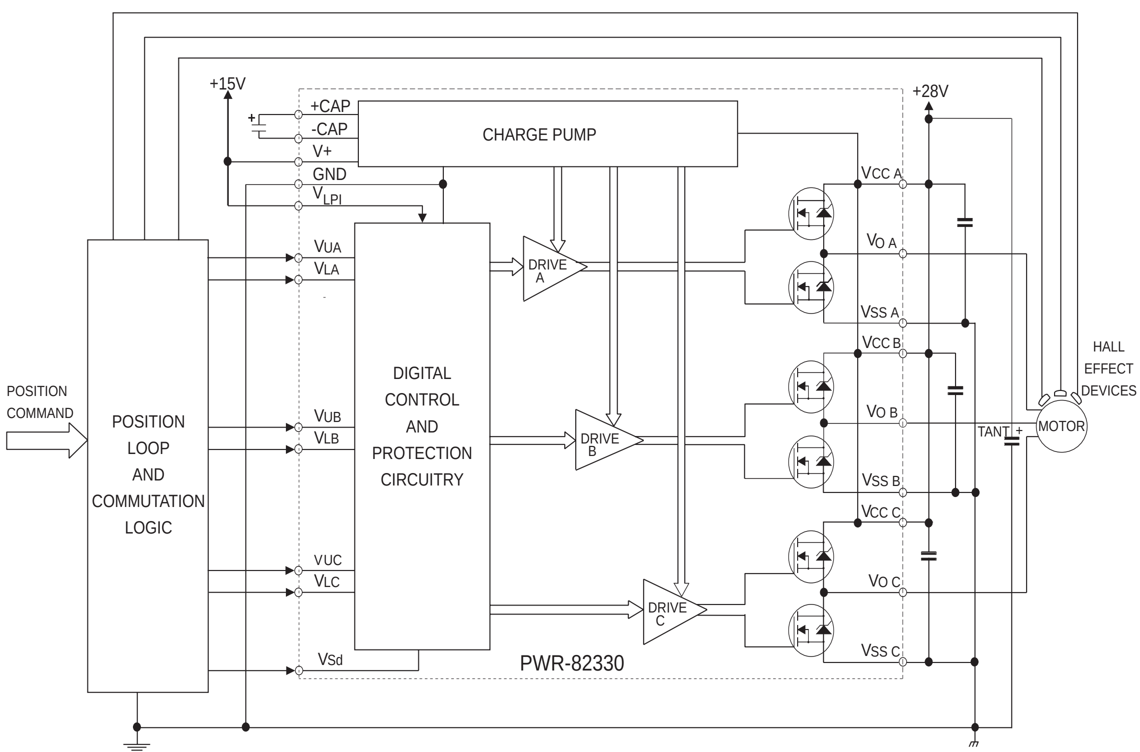


FIGURE 4. TYPICAL INTERFACE WITH A MOTOR AND COMMUTATION LOGIC

TABLE 3. INPUT/OUTPUT TRUTH TABLE									
INPUTS							OUTPUTS		
UPPERS			LOWERS			CONTROL			
VUA	VUB	VUC	VLA	VLB	VLC	VSd	VOA	VOB	VOC
1	0	0	0	1	0	0	H	L	Z
1	0	0	0	0	1	0	H	Z	L
0	1	0	0	0	1	0	Z	H	L
0	1	0	1	0	0	0	L	H	Z
0	0	1	1	0	0	0	L	Z	H
0	0	1	0	1	0	0	Z	L	H
0	0	1	1	1	0	0	L	L	H
0	1	0	1	0	1	0	L	H	L
0	1	1	1	0	0	0	L	H	H
1	0	0	0	1	1	0	H	L	L
1	0	1	0	1	0	0	H	L	H
1	1	0	0	0	1	0	H	H	L
0	0	0	0	0	0	0	Z	Z	Z
0	0	0	1	1	1	0	L	L	L
1	1	1	0	0	0	0	H	H	H
X	X	X	X	X	X	1	Z	Z	Z
H = High Level, L= Low Level, X=Irrelevant, Z= High Impedance (OFF)									

the signals at the VU and VL pins; this ensures the complete turn-off of any transistor before turning on its associated in-line transistor.

CHARGE PUMP

The PWR-82330 has an internal charge pump circuit to generate the drive voltage for the high side N-channel MOSFETs. The charge pump uses an oscillator to charge an external charge pump capacitor, Cc, from the Vcc supply. This oscillator will pump the voltage at pin 48 (+cap) of the hybrid higher than Vcc. The hybrid high side drivers use this voltage to ensure the proper gate drive.

An external 1 µF, 20% capacitor (Cc) is required between pins 48 and 50. If a polarized capacitor is used, the positive terminal must be connected to pin 48. The voltage rating of Cc must be 2x the maximum value of VCC.

PWR-82330 POWER DISSIPATION (SEE FIGURE 7)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and intrinsic diode losses.

V_{CC} = +28 V (Bus Voltage)

I_{OA} = 3 A, I_{OB} = 7 A (see FIGURE 7)

ton = 20 µs, T = 40 µs (period) (see FIGURE 7)

Ron = 0.13 Ω (on-resistance, see TABLE 2, Io = 5 A, Tc=+25°C)

ts1 = 325 ns, ts2 = 325 ns (see FIGURE 7)

fo = 25 kHz (switching frequency)

V_F is an intrinsic diode forward voltage, TABLE 2, Io = 5 A

1. Conduction Losses (PC)

$Pc = (\text{Imotor rms})^2 \times Ron$

$$I_{\text{motor rms}} = \sqrt{\left(I_{OB}^{2} - I_{OB}(I_{OB} - I_{OA}) + \frac{(I_{OB} - I_{OA})^{2}}{3}\right)\left(\frac{ton}{T}\right)}$$

$$I_{\text{motor rms}} = \sqrt{\left(7A^{2} - 7A(7A - 3A) + \frac{(7A - 3A)^{2}}{3}\right)\left(\frac{20us}{40us}\right)}$$

$Pc = (3.63\ A)^2 \times (0.13\ W)$

Pc = 1.71 Watts

2. Switching Losses (Ps)

$Ps = [\,Vcc\,(\,I_{OA}\,(ts1) + I_{OB}\,(ts2)\,)\,fo] / 2$

Ps = [28 V (3 A (325 ns) + 7 A (325 ns)) 25 kHz] / 2

Ps = 1.14 Watts

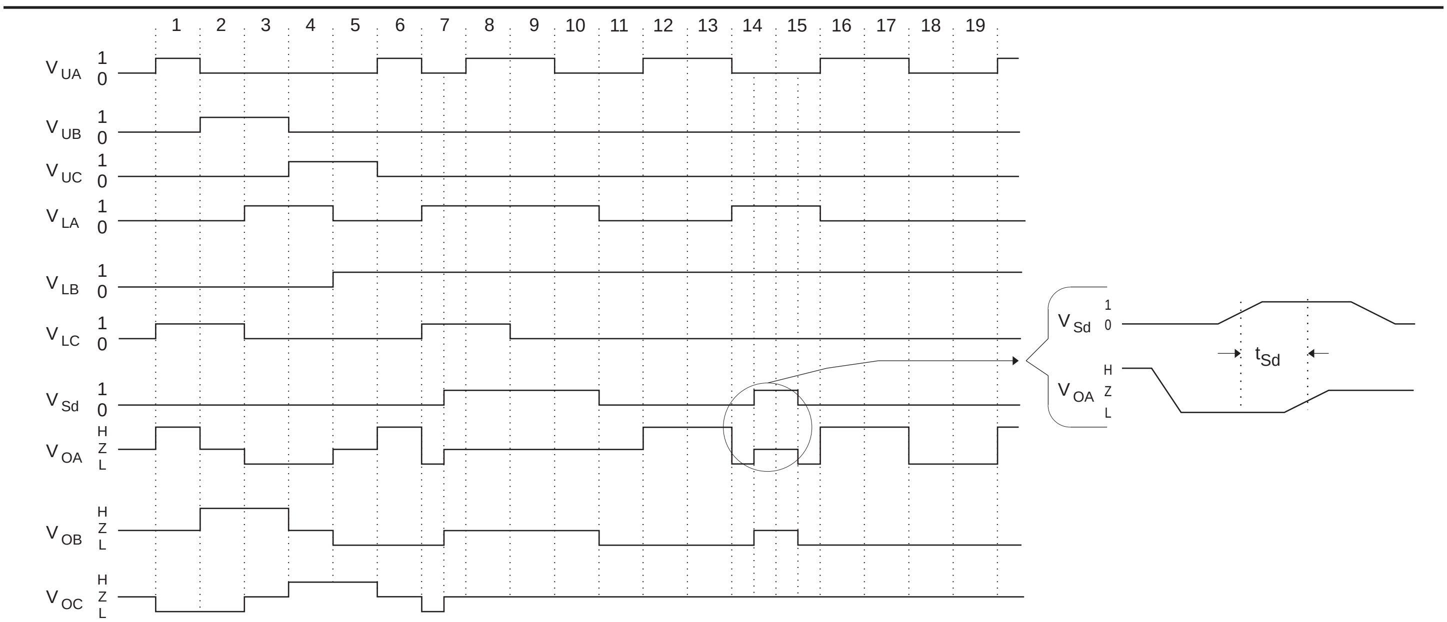


FIGURE 5. SHUT-DOWN (VSd) TIMING RELATIONSHIPS

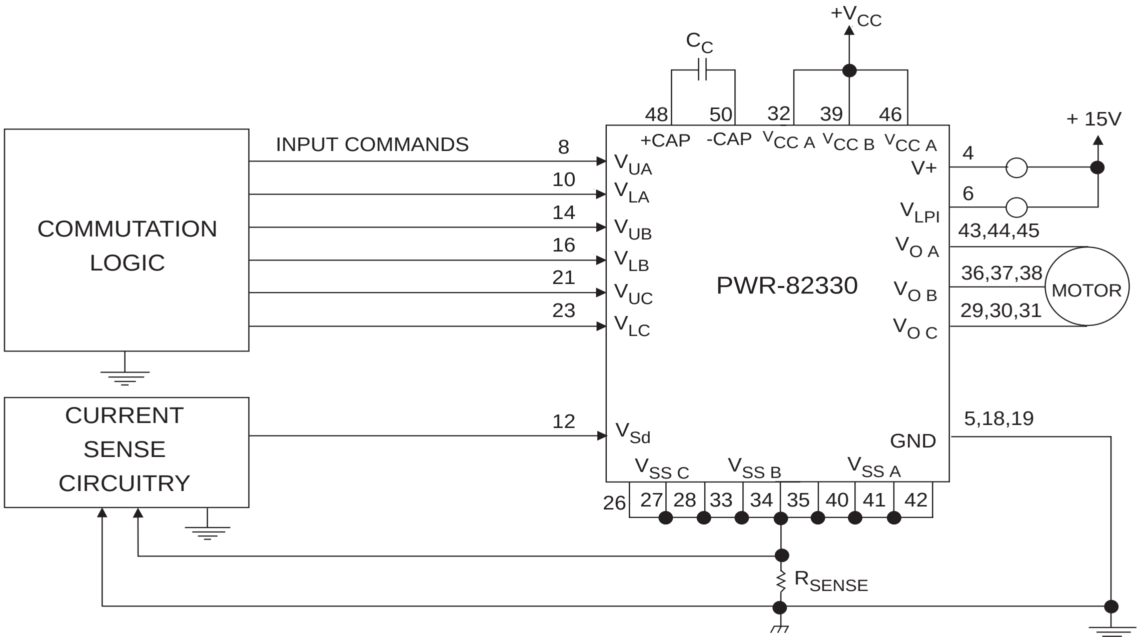


FIGURE 6. FUNCTIONAL SHUT-DOWN INPUT USED WITH CURRENT-SENSING CIRCUITRY

3. Intrinsic Diode Losses (Pd)

$P_d = I_d\,(avg) \times V_d\,(avg)$

$I_d(avg) = [(I_{OB} + I_{OA}) / 2] / 2 = [(7\text{ A} + 3\text{ A}) / 2] / 2 = 2.5\text{ A}$

$P_d = 2.5\text{ A} \times 1.25\text{ V}$

$P_d = 3.125$ Watts

TRANSISTOR POWER DISSIPATION (PQ)

To calculate the maximum power dissipation of the output transistor as a function of the case temperature use the following equation. (Reference FIGURE 8 to ensure you don't exceed the maximum allowable power dissipation of each transistor.

$P_Q = P_c + P_s + P_d$

TOTAL HYBRID POWER DISSIPATION (PTOTAL)

To calculate Total Power dissipated in the hybrid use:

$$P_{TOTAL} = \sum_{i=1}^{6} [\, PQi \,] \text{ where i = each transistor}$$

LAYOUT AND EXTERNAL COMPONENTS

Important Information - The following layout guidelines and required external components are critical to the proper operation of these motor drives.

Permanent damage will result to the motor drive if the user does not make the following recommended ground connections that will ensure the proper operation of the hybrid.

The V+ and logic grounds are on pins 5,18, and 19 (GND). The Vss connections for the output stage are on pins 26-28, 33-35 and 40-42 (VSS). **To prevent damage to the internal drive circuitry, the differential voltage between GND and Vss must not exceed ± 3 V max, dc or peak.** This includes the combined voltage drop of the associated ground paths and the voltage drop across Rsense (see FIGURE 9). For example, a value for Rsense of 0.1 Ω will give a voltage drop of 1.00 V at 10 A and allow enough margin for the voltage drop in the ground conductors. Locate Rsense 1" - 2" maximum from the hybrid. **It is critical that all ground connections be as short, and of lowest impedance, as the system allows.**

C1, C2, and C3 are 0.1 µF ceramic bypass capacitors that supply high frequency spiking. The voltage rating should be 2x the maximum system voltage. These capacitors should be located as close to the hybrid as possible. Please note, on FIGURE 9, that C1, C2, and C3 must go directly from terminal-to-terminal on the hybrid - **do not daisy chain along the power ground return.**

C4 and C5 are 0.01 µF, 50 V ceramic capacitors for power supply decoupling. Locate as close to the hybrid as possible. Cc is a 1 µF, 20% capacitor (either polarized or nonpolarized). If a polarized cap is used, the positive terminal must be connected to pin 48 of the hybrid. Voltage rating should be 2x the maximum system voltage.

Care must be taken to control the regenerative energy produced by the motor in order to prevent excessive voltage spiking on the Vcc line. Accomplish this by placing a capacitor or clamping diode between Vcc and high power ground return.

SWITCHING LOSSES

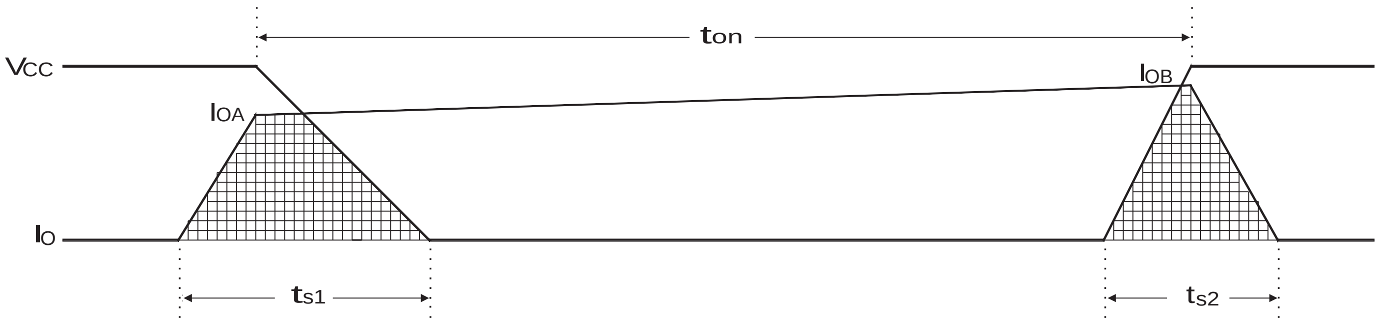


FIGURE 7. OUTPUT CHARACTERISTICS

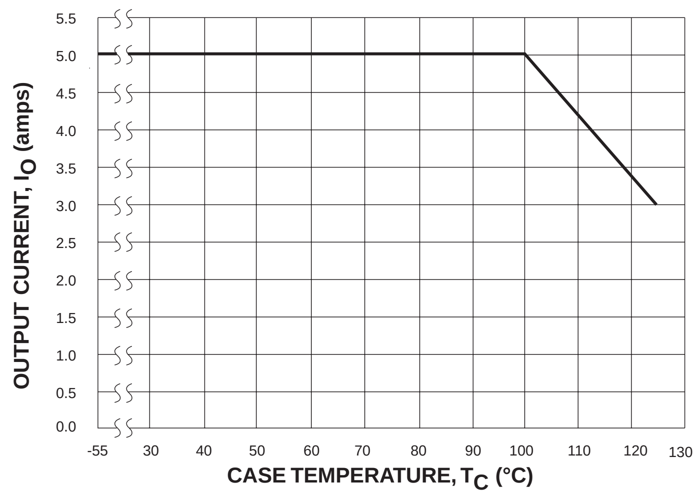
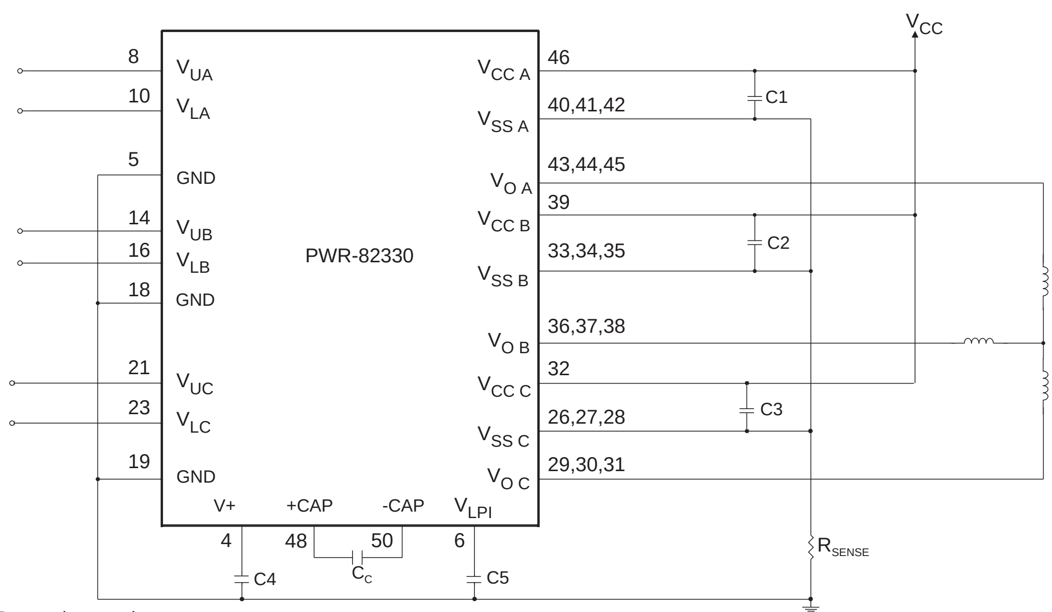


FIGURE 8. MAXIMUM ALLOWABLE CONDITIONS OUTPUT CURRENT VS. CASE TEMPERATURE

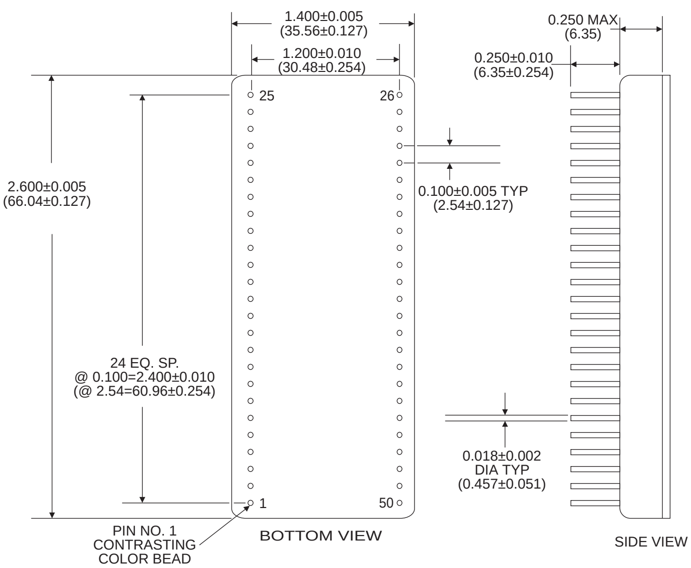


C1,C2,and C3=0.01 µF ceramic capacitors
C4 and C5=0.01 µF ceramic capacitors

FIGURE 9. GROUND CONNECTIONS

MOUNTING

The PWR-82330 package is designed for direct insertion to a printed wiring board. The heat transfer in a hybrid is from semiconductor junction to the bottom of the hybrid case. The flatness and maximum temperature of this mounting surface are critical to the performance and reliability, because this is the only method of dissipating the power generated in the hybrid. Use a mounting surface flatness of 0.004 inches/inch maximum. This interface can be improved with the use of a thermal compound or pad.



NOTES:
1. DIMENSIONS IN INCHES(MM). TOL = ±0.005(±0.127).
2. LEAD CONCENTRATION NUMBERS ARE FOR REFERENCE ONLY.

FIGURE 10. MECHANICAL OUTLINE

TABLE 4. PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	N/C	50	-CAP
2	N/C	49	N/C
3	N/C	48	+CAP
4	V+	47	N/C
5	GND	46	VC A
6	VLPI	45	VO A
7	N/C	44	VO A
8	VUA	43	VO A
9	N/C	42	VSS A
10	VLA	41	VSS A
11	N/C	40	VSS A
12	VSd	39	VCC B
13	N/C	38	VO B
14	VUB	37	VO B
15	N/C	36	VO B
16	VLB	35	VSS B
17	N/C	34	VSS B
18	GND	33	VSS B
19	GND	32	VCC C
20	N/C	31	VO C
21	VUC	30	VO C
22	N/C	29	VO C
23	VLC	28	VSS C
24	N/C	27	VSS C
25	N/C	26	VSS C

ORDERING INFORMATION

PWR-82330-XX0X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100
- Blank = None of the Above

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

NOTES

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