LH5494

4K × 9 Serial-to-Parallel FIFO

FEATURES

- Fast Cycle Times: 30/35 ns
  Frequency: 33/28.5 MHz
- Serial Data In; Parallel Data Out
- Serial Output for Cascading Input Register
- Two Read Enable Inputs and One Write Enable Input, Sampled on Rising Edge of the Appropriate Clock
- Fast-Fall-Through Time Internal Architecture Based on CMOS Dual-Port RAM Technology, 4096 × 9
- Fully Asynchronous Read and Write Operations
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Three-State Outputs with Output Enable
- Reset/Reread Capability
- TTL and CMOS Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5494 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 4096 nine-bit words. One LH5494 FIFO can input a serial bitstream, and output nine-bit bytes in parallel. Thus, a single LH5494 is capable of nine-bit-to-one-bit SIPO (Serial-In, Parallel-Out) operation.

An LH5494 has one one-bit serial input, and one nine-bit parallel output (read) port. And there is one one-bit serial output, which supports paralleling LH5494s for greater-word-width SIPO operation. This serial output also allows additional control bits to be inserted at will into the serial output bitstream.

The LH5494 architecture supports a very convenient method of *paralleling* multiple FIFOs for SIPO operation, without any additional logic being needed, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5494 combination remains capable of performing all of the operations which a standalone LH5494 can perform. Thus, if two LH5494s are paralleled, the combination can input a serial bitstream and output 18-bit halfwords for 1-bit-to-18-bit SIPO operation. This paralleling scheme extends without change to an *arbitrary* number of LH5494s.

The LH5494 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either totally full or else totally empty.

One edge-sampled enable control input, WEN, is provided for the input port; and two such control inputs, REN_1 and REN_2, are provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5494 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag

PIN CONNECTIONS

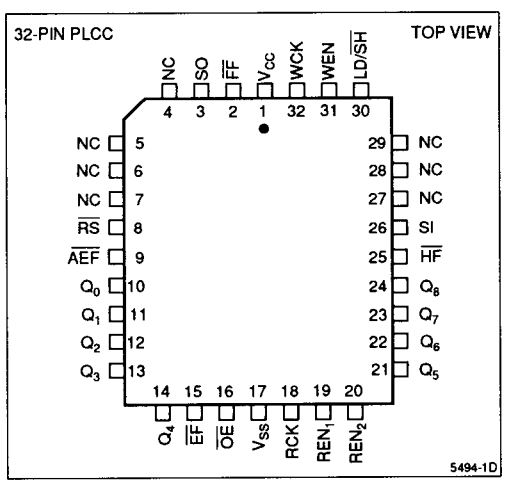


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

may be tied directly to WEN, and the Empty flag likewise may be tied directly to $\overline{REN_1}$ or to $\overline{REN_2}$, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 11.)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other

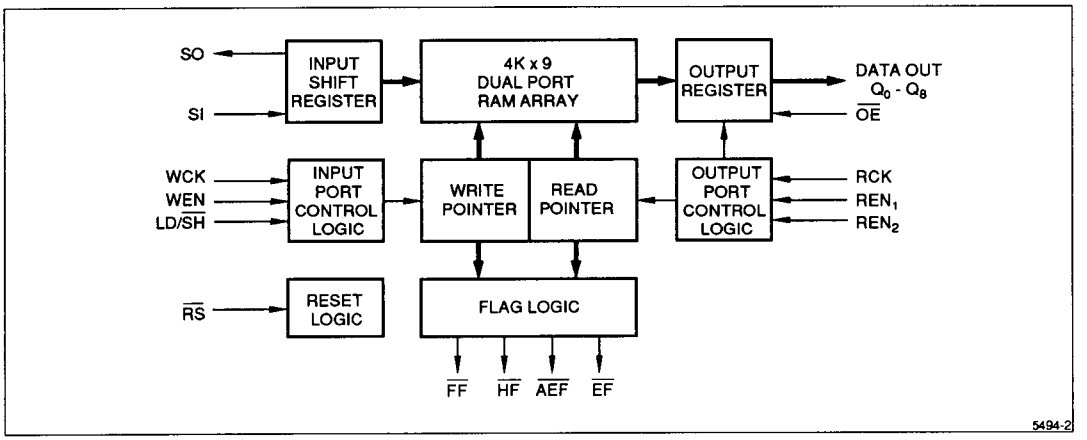


Figure 2. LH5494 Block Diagram

SIGNAL PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for Write operations.
RCK	Read Clock. A free-running clock input for Read operations.
SI	Serial Input. SI is sampled on the rising edge of WCK, whenever WEN is being asserted.
SO	Serial Output. A serial data output signal, to allow paralleled SIPO operation of multiple devices.
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever $\overline{REN_1}$ and $\overline{REN_2}$ are both being asserted.
WEN	Write Enable. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO.
LD/$\overline{SH}$	Load/Shift. An input signal which is sampled on the rising edge of WCK to control the load of parallel data from Input Shift Register into the FIFO.
$\overline{REN_1}$	Read Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both $\overline{REN_1}$ and $\overline{REN_2}$ must be asserted in order to enable a read operation.
$\overline{REN_2}$	Read Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both $\overline{REN_1}$ and $\overline{REN_2}$ must be asserted in order to enable a read operation.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating, when asserted, when the FIFO is empty.
$\overline{OE}$	Output Enable. An assertive-LOW signal which, when asserted, places the data outputs $Q_0 - Q_8$ in a low-impedance state.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to Vss Potential	−0.5 V to 7 V
Signal Pin Voltage to Vss Potential[3]	−0.5 V to Vcc + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IH} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at fc = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

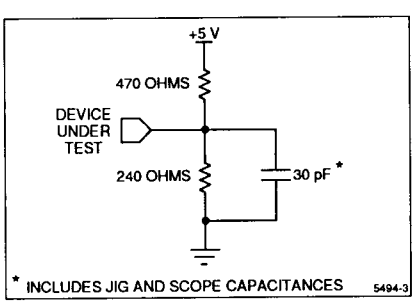


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance	7 pF
C_O (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-30		-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	33.3	–	28.5	MHz
t_{WC}	Write Clock Cycle Time	25	–	30	–	35	–	ns
t_{WH}	Write Clock HIGH Time	10	–	12	–	14	–	ns
t_{WL}	Write Clock LOW Time	10	–	12	–	14	–	ns
t_{RC}	Read Clock Cycle Time	25	–	25	–	35	–	ns
t_{RH}	Read Clock HIGH Time	10	–	10	–	14	–	ns
t_{RL}	Read Clock LOW Time	10	–	10	–	14	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_{ES}	Enable Setup TIme to Rising Clock	10	–	10	–	10	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_A	Data Output Access Time	–	20	–	22	–	25	ns
t_{SA}	Serial Output Access Time	–	20	—	22	–	25	ns
t_{OH}	Output Hold Time from Rising RCK	5	–	5	–	5	–	ns
t_{OL}	$\overline{OE}$ to Data Outputs Low-Z [2]	1	–	1	–	1	–	ns
t_{OZ}	$\overline{OE}$ to Data Outputs High-Z [2]	–	10	–	11	–	12	ns
t_{OE}	Output Enable to Data Valid	–	10	–	11	–	12	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	22	–	25	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	22	–	25	ns
t_{HF}	Clock to Half Flag Valid	–	35	–	37	–	40	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	37	–	40	ns
t_{RS}	Reset Pulse Width	25	–	30	–	35	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	12	–	15	–	ns
t_{RF}	Reset LOW to Flag Valid	–	30	–	32	–	35	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	22	–	25	ns
t_{FRL}	First Read Latency [4]	18	–	19	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	19	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN is being asserted, or else a rising edge of RCK occurs while REN_1 and REN_2 both are being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-Write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Read, shift, and/or write operations need not be deactivated during a reset operation, but failure to do so requires observance of the Reset Setup Time (t_{RSS}), to assure that the first write and/or first read following a reset operation will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' word being held in the output register consists of all zeroes. This data word is seen on the output bus ($Q_0 - Q_8$) whenever the output enable ($\overline{OE}$) is held LOW. Likewise, data in the input shift register is initialized to all zeroes after a reset operation.

Write

A shift operation is initiated on the rising edge of WCK, whenever WEN is HIGH and LD/$\overline{SH}$ is LOW. Data bits are shifted from MSB to LSB, with the data bit on the Serial Input (SI) replacing the contents of bit position D_7 in the input shift register, and the Serial Output (SO) copying the contents of bit position D_0.

A write operation consists of a parallel loading of data from the input shift register (bits $D_7 - D_0$), and the SI pin (bit D_8) to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both the edge-sampled Write Enable input (WEN) and the Load/Shift input (LD/$\overline{SH}$) are held HIGH.

When a full condition is reached, shift operations may continue; but write operations should be ceased, in order to prevent overwriting unread data. The state of the status flags has no direct effect on shift or write operations; that is, the execution of write operations is gated only by WEN, and the internal logic of the LH5494 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location is freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency time (t_{FWL}) after the first read operation from a full FIFO, in order to assure that a correct data word is written into the FIFO memory.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK) whenever both of the edge-sampled Read Enable inputs (REN_1 and REN_2) are held HIGH for the prescribed setup and hold times. Read data becomes valid on the Data Out pins ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK, provided that the Output Enable ($\overline{OE}$) is being held LOW. $\overline{OE}$ is an assertive-LOW asynchronous input. When $\overline{OE}$ is taken LOW, the $Q_0 - Q_8$ outputs are driven (i.e., are in a low-Z state) within a minimum time t_{OL}. When $\overline{OE}$ is taken HIGH, the $Q_0 - Q_8$ outputs are in a high-Z state within a maximum time t_{OZ}. The state of the four status flags has no direct effect on read operations; that is, the execution of read or shift operations is gated only by REN_1 and REN_2 and LD/$\overline{SH}$, and the internal logic of the LH5494 itself has no interlock to prevent underrunning valid data after the internal read pointer catches up to the write pointer – and passes it, if reading is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

When an empty condition is reached, read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the Empty Flag ($\overline{EF}$) is deasserted ($\overline{EF}$ = HIGH). The next read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write operation into an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

Status Flags are included for Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1 (page 5-119). Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

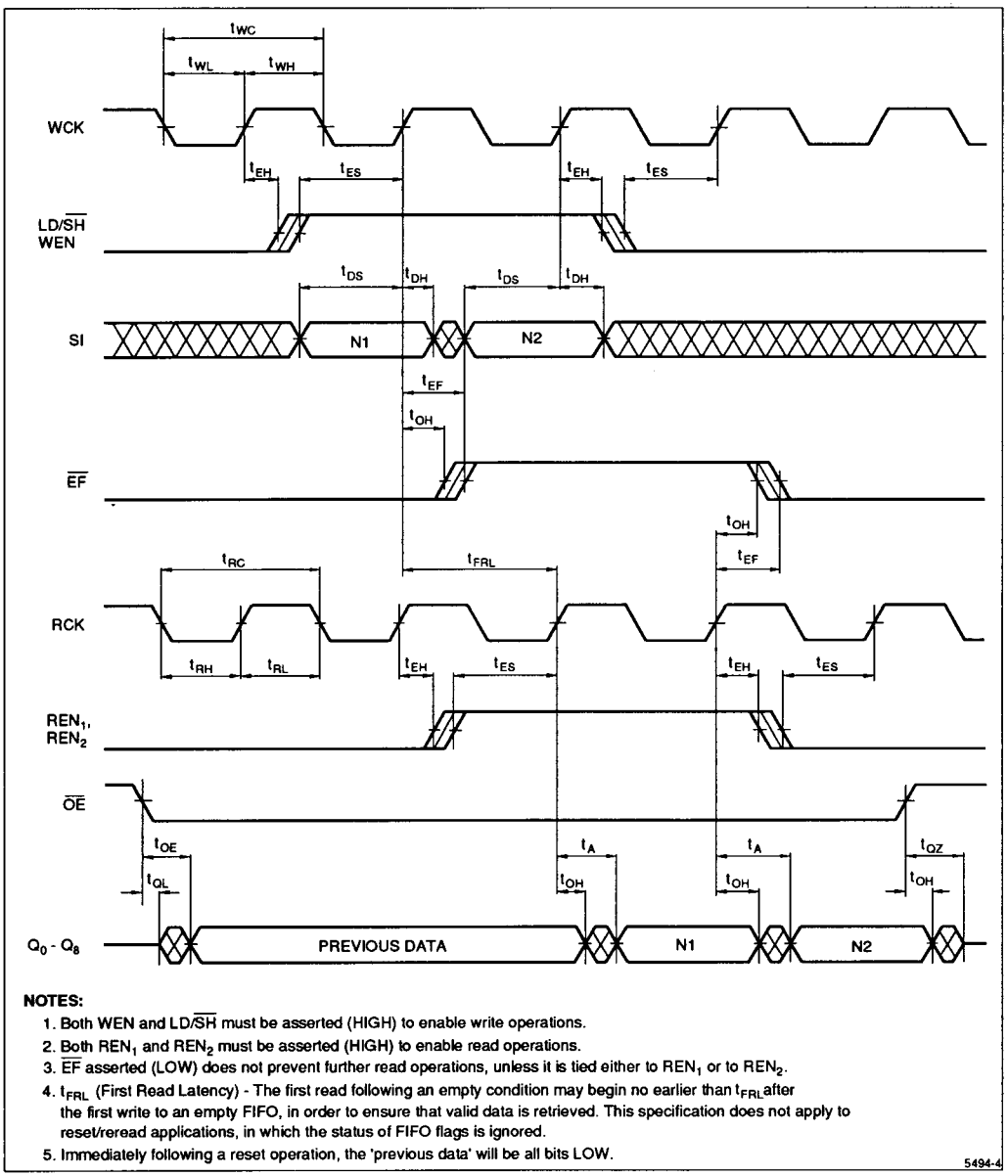
The FIFO can be made to reread previously read data through a reset operation, which initializes the internal read and write address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 words of old data, which previously had been written into and/or read from the FIFO, still then remain in

OPERATIONAL DESCRIPTION (cont'd)

the memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations.

The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data are being written to the FIFO following the Reset.

TIMING DIAGRAMS



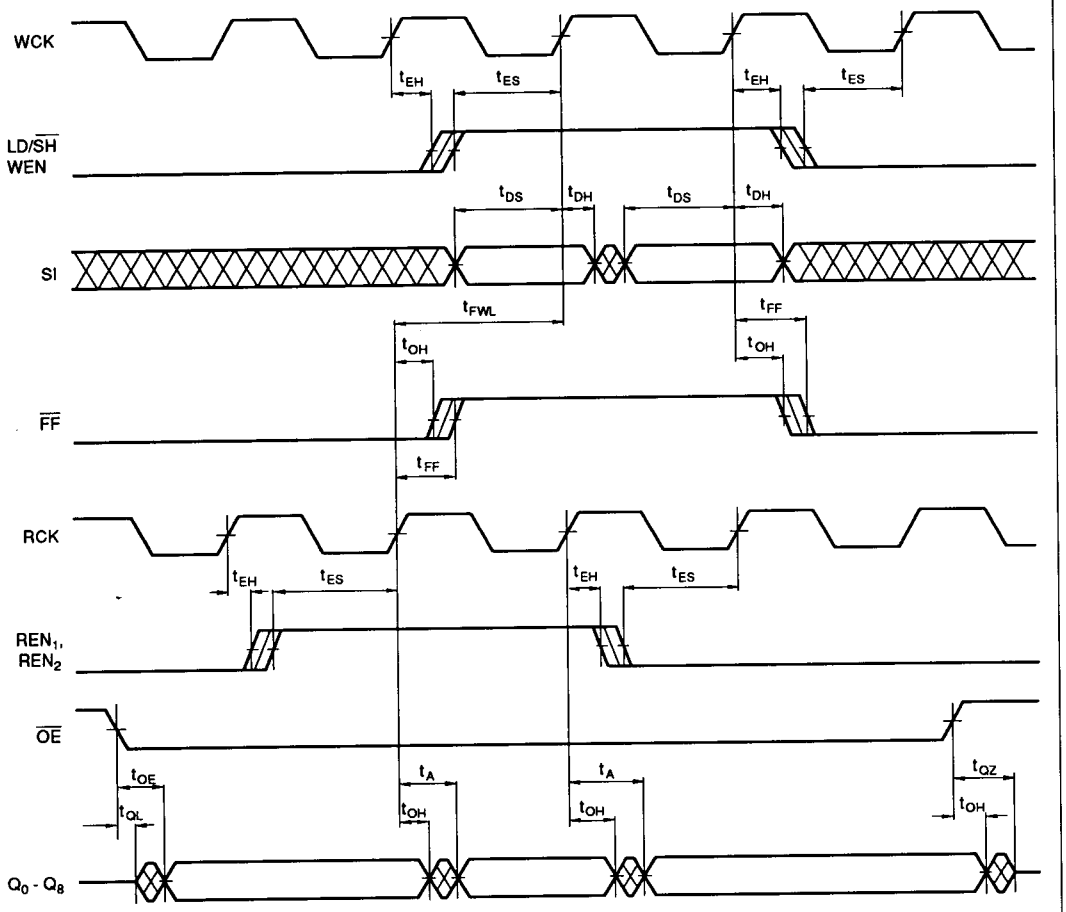
NOTES:

1. Both WEN and LD/$\overline{SH}$ must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ asserted (LOW) does not prevent further read operations, unless it is tied either to REN_1 or to REN_2.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, in order to ensure that valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.
5. Immediately following a reset operation, the 'previous data' will be all bits LOW.

5494-4

Figure 4. Write and Read Operations in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. Both WEN and LD/$\overline{SH}$ must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ asserted (LOW) does not prevent further write operations, unless it is tied to WEN.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5494-5

Figure 5. Read and Write Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)

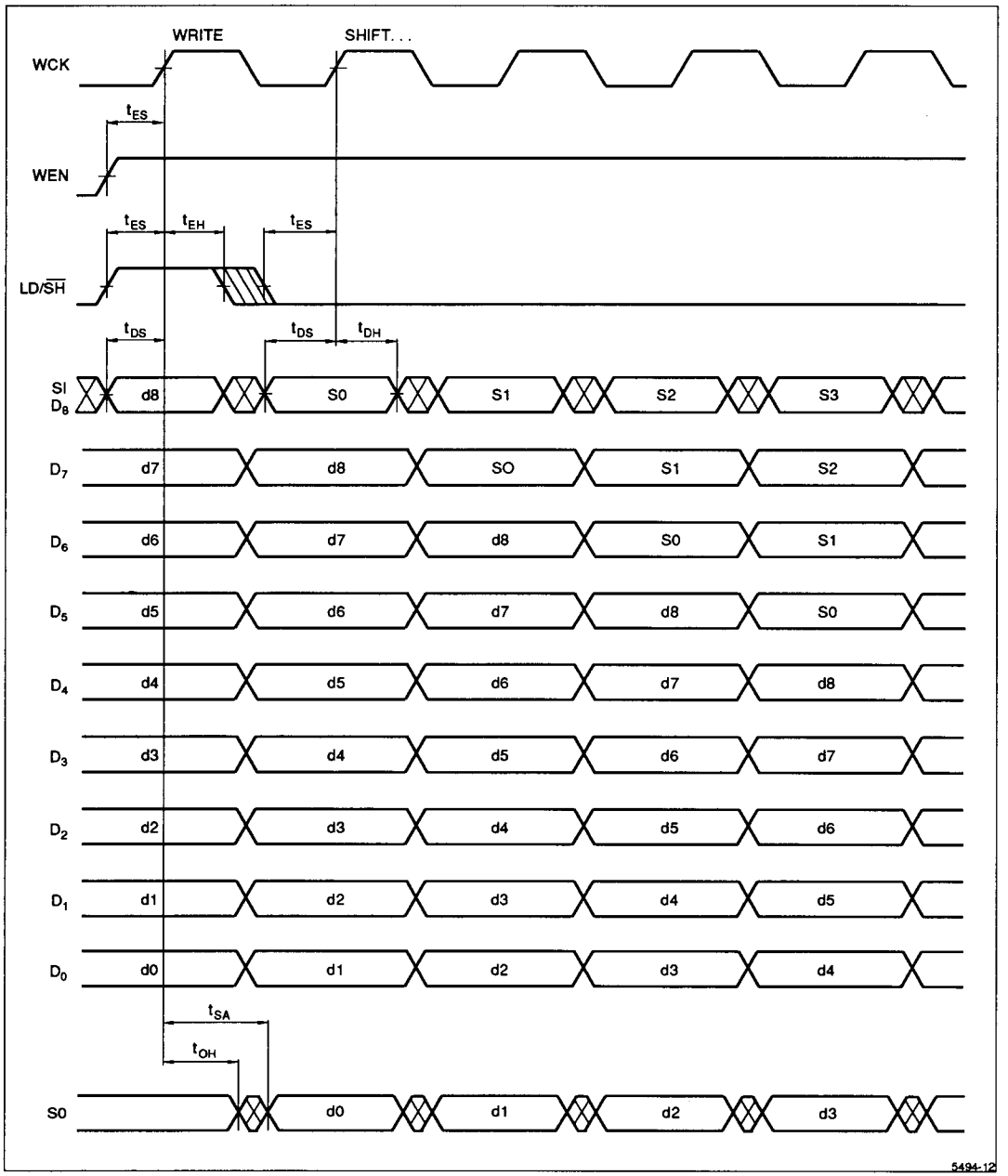
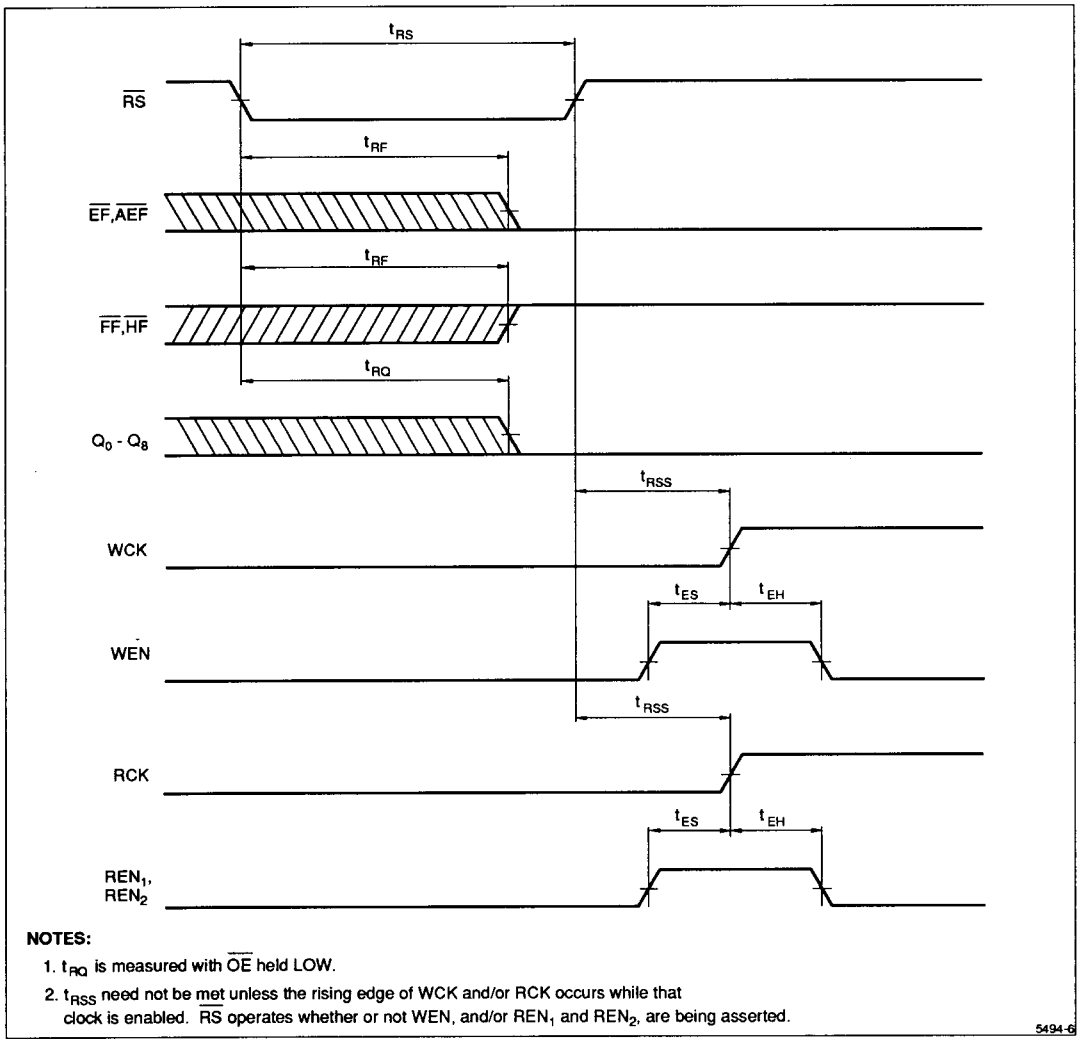


Figure 6. Serial Shift, Write Timing

TIMING DIAGRAMS (cont'd)



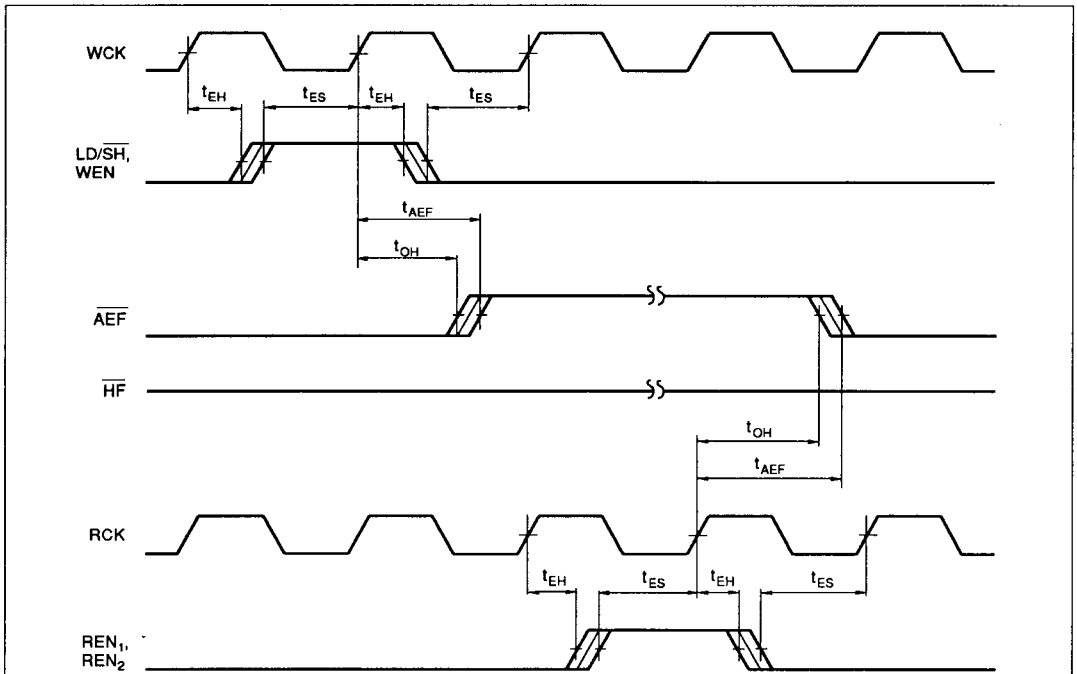
NOTES:

1. t_{RQ} is measured with $\overline{OE}$ held LOW.
2. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN, and/or REN_1 and REN_2, are being asserted.

5494-6

Figure 7. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to AE = AEF · $\overline{HF}$ = $\overline{\overline{AEF} + HF}$.

5494-7

Figure 8. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2048
1	1	0	1	8	2047	2049	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

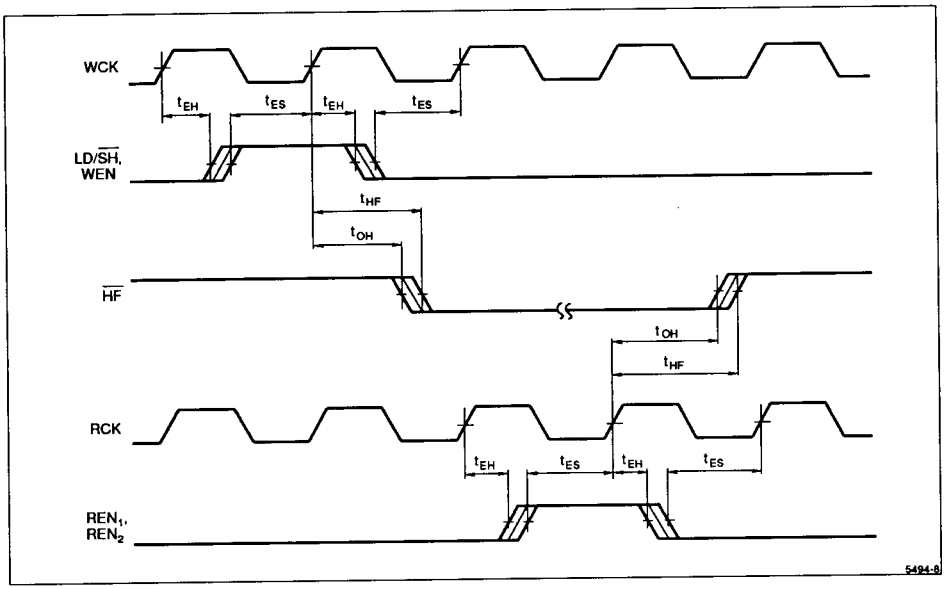
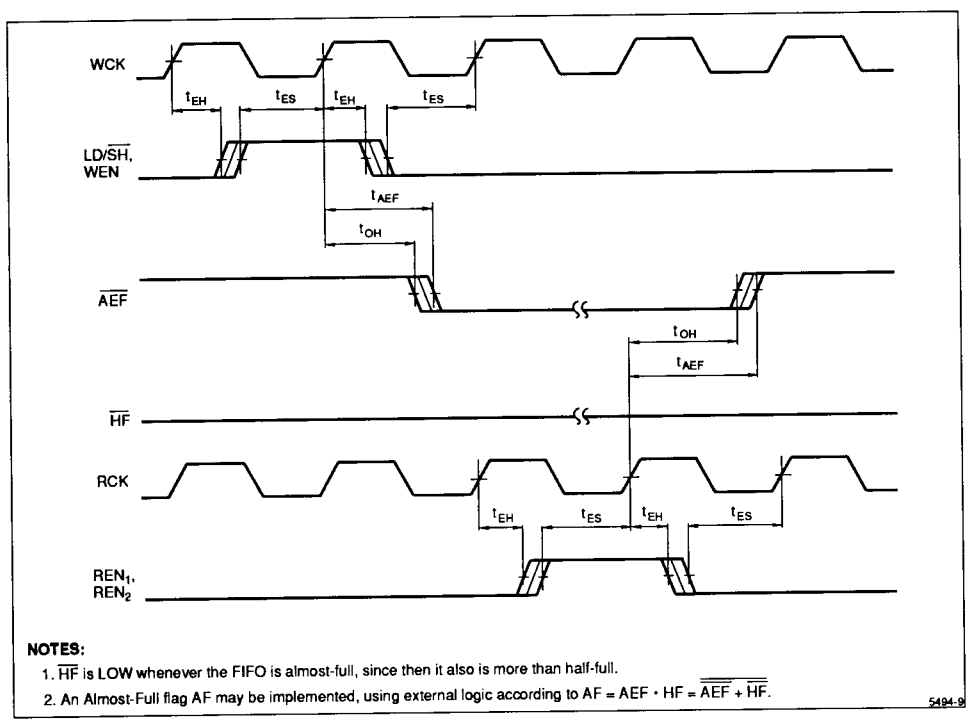


Figure 9. Half-Full Flag Timing



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to $AF = AEF \cdot HF = \overline{\overline{AEF} + \overline{HF}}$.

Figure 10. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Read and Write Operations

Read and write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. As such, the Read Enable (REN_1 and REN_2), Write Enable (WEN), and Load/Shift ($LD/\overline{SH}$) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the REN_1, REN_2, and WEN inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to WEN, in order to prevent 'overrun' write operations when the full condition is reached. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to REN_1 or REN_2, in order to prevent 'underrun' read operations when the empty condition is reached, while the other Read Enable input remains available for system control.

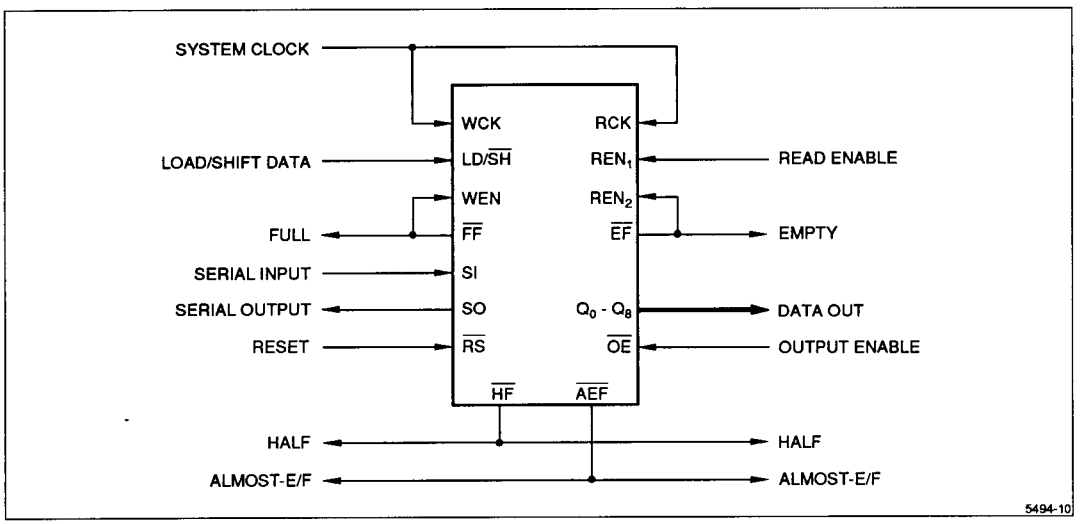


Figure 11. Synchronous Operation

OPERATIONAL MODES (cont'd)

Asynchronous Read and Write Operations

Write operations and read operations may be performed completely asynchronously relative to each other, when the RCK input and the WCK input are derived from clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to drive Read Enable or Write Enable inputs directly, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user, in order to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underrunning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

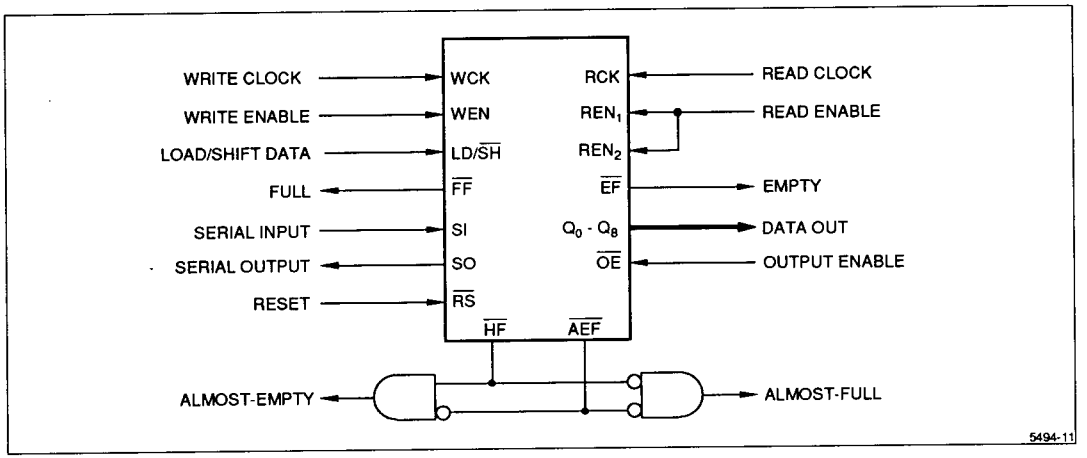


Figure 12. Asychronous Operation

OPERATIONAL MODES (cont'd)

Cascaded Operation

Cascaded operation allows LH5494 input shift registers to be extended in wordwidth, by interconnecting multiple LH5494 devices in a serial chain. The Serial Input (SI) of the first device in the chain serves as the 'effective-FIFO' serial input. The SI pin of any subsequent device is connected to the Serial Out (SO) pin of the preceding device in the chain. The final 'effective FIFO' serial output data (if needed) is taken from the SO pin of the last device in the chain.

In cascaded operation, the output port may be configured either for an increase in FIFO depth, or for an increase in FIFO wordwidth. When the output port is expanded in width, the Read Enable inputs (REN_1 and REN_2) and Output Enable ($\overline{OE}$) are common for all devices.

When the output port is expanded in depth, the common Data Out pins of multiple devices may be tied together. One Read Enable may then be used for system control, while the other Read Enable and $\overline{OE}$ are driven by decode logic to direct the flow of data. This decode logic should alternate read accesses from one device to the next in a sequential manner.

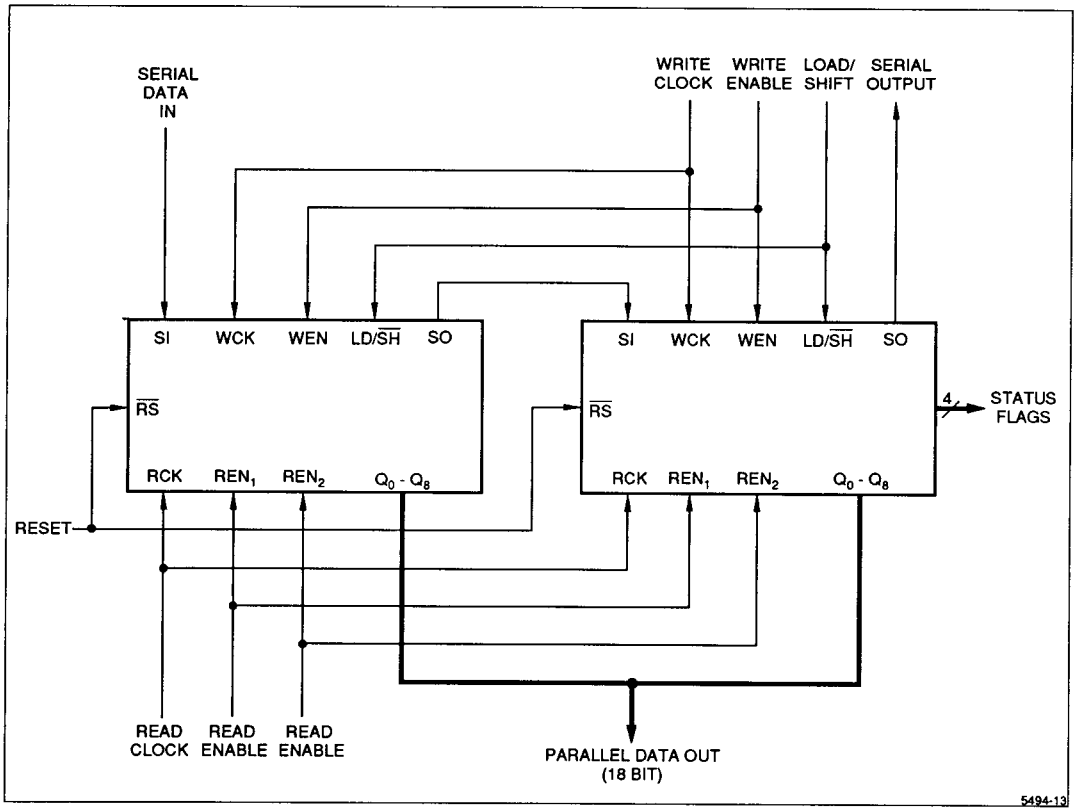


Figure 13. Cascaded Serial Operation (4096 × 18 Bit)

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