

5V, 300mA REGULATOR with RESET and ENABLE

Description

Block Diagram

Voltage Shutdown

Thermal Shutdown

Bandgap Reference

The CS-8120 is a 5V precision linear regulator with two microprocessor compatible control functions and protection circuitry included on chip. The composite NPN-PNP output pass transistor assures a low dropout voltage (1V @ 150mA) without requiring excessive supply current (2.5mA).

The CS-8120's two logic control functions make this regulator well suited to applications requiring microprocessorbased control at the board or module level. The ENABLE function controls the output stage. A high voltage (>2.9V) on the ENABLE pin turns off the regulator's pass transistor and sends

ENABLE

2

Comparator

TO VOU

ENABLE

RESET

the IC into Sleep mode where it draws only 250 μ A. The RESET function sends a RESET signal when the IC is powering up or whenever the output voltage moves out of regulation. The RESET signal is valid down to V_{OUT} =1V.

The CS-8120 design optimizes supply rejection by switching the internal bandgap reference from the supply input to the regulator output as soon as the nominal output voltage is achieved. Additional on chip filtering enhances rejection of high frequency transients on all external pins.

Output

Current

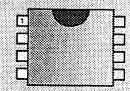
Error Amplifier

Features

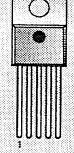
- 5V ± 4% Output Voltage
- Low Dropout Voltage (1V @ 150mA)
- Low Quiescent Current (2.5mA @ I_{OUT}=150mA)
- μP Compatible Control Functions
 - RESET ENABLE
- Low Current Sleep Mode IQ=250µA
- Protection Features
 Thermal Shutdown
 Short Circuit
 Overvoltage (60V)

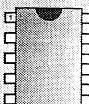
Package Options

8L PDIP



5L TO-220 Tab (Gnd) 14L SO Narrow







Bandgap

Supply

RESET

Cherry Semiconductor Corporation 2000 South County Trail East Greenwich, Rhode Island 02818 Tel: (401)885-3600 Fax (401)885-5786 Telex WUI 6817157



Absolute Maximum Ratings

DC Input Voltage	-0.7 to 26V
Transient Input Voltage	60V
Output Current	Internally Limited
Electrostatic Discharge (Human Body Model)	2kV
Operating, Junction and Storage Temperatures	40°C to 150°C
Lead Temperature (Soldering, 10s)	230°C

Electrical Cha	racteristics: V_{IN} =14V, I_{OUT} =5mA, -40°C	≤T _J ≤150°C u	nless otherwise sp	pecified	
PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
Output Stage					•
Output Voltage, V _{OUT}	7V≤V _{IN} ≤26V, 1mA≤I _{OUT} ≤300mA	4.8	5.0	5.2	<u>V</u>
Line Regulation	7V≤V _{IN} ≤26V			50	mV
Load Regulation	1mA≤I _{OUT} ≤300mA			50	mV
Supply Voltage Rejection	$V_{\rm IN}$ 14 $V_{\rm DC}$ + 1 $V_{\rm RMS}$ @120Hz, I _{LOAD} =2.5 Ω	54	70		dB
Dropout Voltage	$I_{OUT} = 300 \text{mA}$	Anno I de San Castron (1904-1904)	1.0	1.5	V
Quiescent Current	ENABLE=High, V _{IN} =12V ENABLE=Low, I _{OUT} =200mA		0.25 2.5	0.65 15	mA mA
Protection Circuits					
Short Circuit Current	0.0000000000000000000000000000000000000	300	600		mA
Thermal Shutdown		150	190		ъ
Overvoltage Shutdown		26	40		V
RESET Functions					
RESET Saturation Voltage	$1V < V_{OUT} < V_{RT_{OFF}} 3.1 k\Omega$ pull-up to V_{OUT}		0.1	0.4	V
RESET Output Leakage	ENABLE=Low		.0	25	μΑ
Current	V _{OUT} >V _{RTON} V _{RST} =V _{OUT}				<i>p.</i> 71
Power ON/OFF RESET Peak Output Voltage	3.1 k Ω pull-up to V_{OUT}		0.7	1.0	V
RESET Threshold ON (Vour Increasing)			V _{OUT} -0.10	V _{OUT} -0.04	V
RESET Threshold OFF (Vout Decreasing)		4.75	V _{OUT} -0.14		A Australian da
RESET Threshold Hysteresis		10	40		mV
ENABLE Functions					
ENABLE Input High Voltage	7V <v<sub>IN<26V</v<sub>		2.9	3.9	
ENABLE Input Low Voltage	7V <v<sub>IN<26V</v<sub>	1.1	2.1		V
ENABLE Input Hysteresis	7V <v<sub>IN<26V</v<sub>	0.4	0.8	2.8	V
ENABLE Input Current	Gnd <v<sub>INH<v<sub>OUT</v<sub></v<sub>	i stetiše istetovana.	0	±10	иA

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PDIP Narrow 1 2 1 V _{IN} Supply voltage to IC, usually direct from the battery. 2 1 1 14 ENABLE CMOS compatible logical input, V _{DNT} is disabled i.e. placed in a high impedance state when ENABLE is high. 3 7 12 Gnd Ground connection. 41 6 10 RESET CMOS compatible output pin. RESET goes low whenever V _{OUT} falls; out of regulation. The RESET delay is externally programmed. 5 4 5 V _{OUT} Regulated output voltage, 5V (typ). N/A 8 25 Vout Regulation which allows remote sensing of output voltage age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} age for improved regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation was obtained to the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation of the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation of the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation of the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation of the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation of the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and the removed regulation. If remote sensing is not desired. Connect to V _{OUT} and	PA	CKAGE PI	IN#	PIN SYMBOL		FUI	NCTION	
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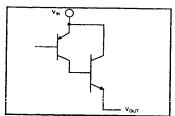
Voltage Reference and Output Circuitry

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within $\pm 4\%$ over temperature and supply variation.

Output Stage

The composite PNP-NPN output structure (Figure 1) provides 300mA (tpy) of output current while maintaining a low drop out voltage (1.25V) and drawing little quiescent current (2.5mA).



The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

Figure 1: Composite Output Stage of the CS-8120

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).

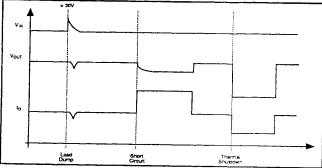


Figure 2: Typical Circuit Waveforms for Output Stage Protection.

If the input voltage rises above 30V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

Regulator Control Functions

The CS-8120 contains two microprocessor compatible control functions: ENABLE and RESET.

ENABLE Function

The ENABLE function switches the output transistor ON and OFF. When the voltage on the ENABLE pin exceeds 2.9V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only $250\mu A$, until the voltage on the pin drops below 2.1V typ. Hysteresis (800mV) is built into the ENABLE function to provide good noise immunity.

RESET Function

A RESET signal (low voltage) is generated as the IC powers up (V_{OUT} - V_{OUT} -100mV) or when V_{OUT} drops out of regulation (V_{OUT} < V_{OUT} -140mV,typ). 40mV of hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1V.

An external RC network on the RESET pin (Figure 3) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT}C_{RST} = \left\lfloor \frac{t_{Delay}}{\ln \left(\frac{V_{T} - V_{OUT}}{V_{RST} - V_{OUT}} \right)} \right\rfloor$$

where: $R_{TOT} = R_{RST}$ in parallel with R_{IN}

 $R_{IN} = \mu P$ port impedance

 $C_{RST} = \overline{RESET}$ Delay capacitor

t_{Delay} = desired delay time

 $V_{RST} = V_{SAT}$ of RESET pin (0.7V @ turn - ON)

 $V_T = \mu P \text{ logic threshold voltage}$

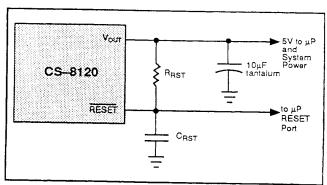


Figure 3: RC Network for RESET Delay

Circuit Description: continued FOR 7V < VIN < 26V (1) - NO RESET DELAY CARACITOR (2) - WITH RESET DELAY CARACITOR

Figure 4: Circuit Waveform

Package Considerations

The CS-8120 is available in 3 packages: a 5 lead TO-220, a 14 lead narrow surface mount, and an 8 lead plastic DIP. The IC operates up to a junction temperature (T_J) of 150°C. However the IC's package and the circuit's worst case power dissipation determine the maximum ambient temperature of the packaged IC. The TO-220 operates at a higher temperature than the other two packages because it dissipates heat more rapidly than the other two packages under comparable power dissipation conditions. The maximum ambient temperature for each package type is calculated from the equation:

$$T_{\mathbf{A}} = T_{\mathbf{J}} \cdot \left(\frac{\mathbf{V}_{\mathbf{IN}} \cdot \mathbf{V}_{\mathbf{OCT}}}{I_{\mathbf{OCT}}} + \frac{\mathbf{V}_{\mathbf{N}}}{I_{\mathbf{Q}}} \right) R_{\mathbf{\Theta}_{\mathbf{J}}\mathbf{A}}$$

where T_J

 v_{IN} = Supply voltage to the IC

 $V_{OUT} = 5V$

LOUT = output current

= IC's quiescent current

The thermal resistances for the three packages are listed here. They are also included in the package specification section under the package thermal data heading. When usines the TO-220 package with heat sink:

$$R_{\Theta_{JA}} = R_{\Theta_{JC}} + R_{CA}$$
 (Heat Sink Thermal Resistance)
= 3.5°C/W + R_{CA}

Package	R _{OCA}	
TO220	50	°C/W
14 SO N	125	°C/W
8 PDIP	100	°C/W

Applications Notes

The circuit depicted in the application diagram lets the microprocessor control its power source, the CS-8120 regulator. An I/O port on the µP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the ENABLE pin falls below its lower threshold. The regulator's output is ENABLED. When the drive current is removed, the voltage on the ENABLE pin rises, the output is switched off and the IC moves into Sleep mode where it draws 250µA.

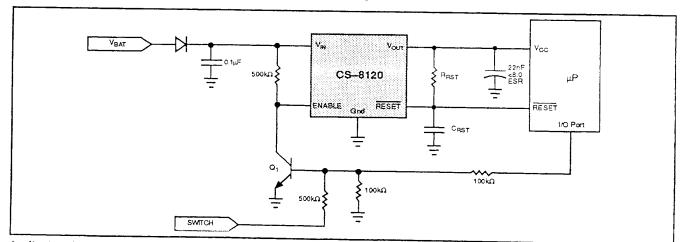
By coupling these two controls with the ENABLE pin, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The μ P can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the

 μP to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1 below

Table 1: Logic Control of CS-8120 Output				
μΡ I/O drive	Switch	ENABLE	Output	
ON	Closed	LOW	ON	
	Open	LOW	ON	
OFF	Closed	LOW	ON	
	Open	HIGH	OFF	

The I/O port of the μP typically provides 50 μA to Q1. In automotive applications the SWITCH is connected to the ignition switch.



Applications diagram - µP Control of CS-8120 using external switching transistor Q1.

Package Specification

ROJC

ROJA

typ

50

PACKAGE DIMENSIONS IN mm(INCHES)

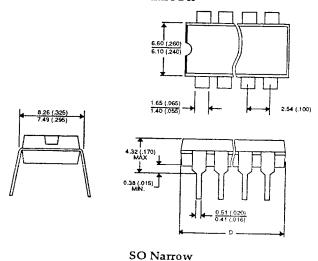
	D				
Lead Count	Metric		English		
	Max	Min	Max	Min	
14 SO NARROW	8.74	8.53	.344	.336	
8 Lead PDIP	9.40	9.14	.370	.360	

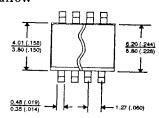
PACKAGE THERMAL DATA Thermal Data TO-220 8L **14L SO** PDIP NARROW 3.5 typ 52 30 'C/W

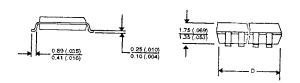
125

*C/W

300 mil PDIP





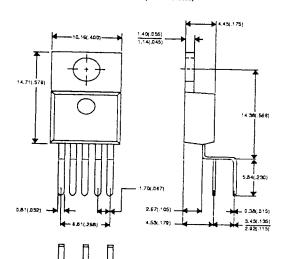


Ordering Information

Part Number CS-8120T	Description TO-220 Straight
CS-8120TV	TO-220 Vertical
CS-8120TH	TO-200 Horizontal
CS-8120N8	8L PDIP
CS-8120D14	14L SO Narrow

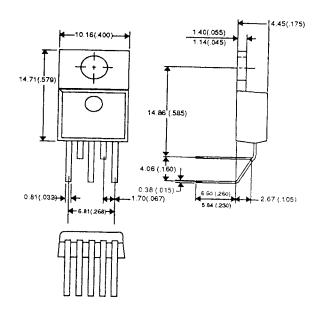
TO-220 (Vertical)

100





TO-220 (Horizontal)





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