# GaAs IC 5 Bit Digital Attenuator With Serial-to-Parallel Driver DC–2 GHz

SKYWORKS

**AA107-310**

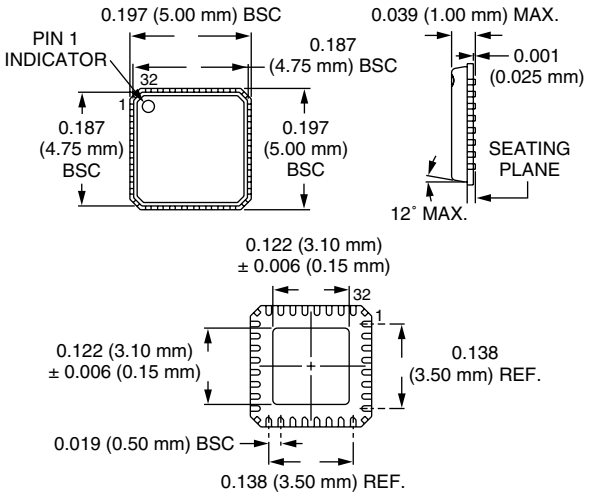
## Features

- Positive Voltage Operation (+5 V)
- QFN 5 x 5 mm Leadless Package
- Integrated Silicon Serial-to-Parallel Driver
- Attenuation 0.5 dB Steps to 15.5 dB

## Description

The AA107-310 is a GaAs FET IC 5 bit digital attenuator with a serial-to-parallel driver packaged in a 32 leadless exposed pad plastic package. It is particularly suited at IF frequencies where high attenuation accuracy, low insertion loss and low intermodulation products are required. Typical applications include base station, wireless and RF data and wireless local loop gain control circuits.

## QFN 5 x 5 (-310)




## Electrical Specifications at 25°C ($V_{CC}$ = +5 V)

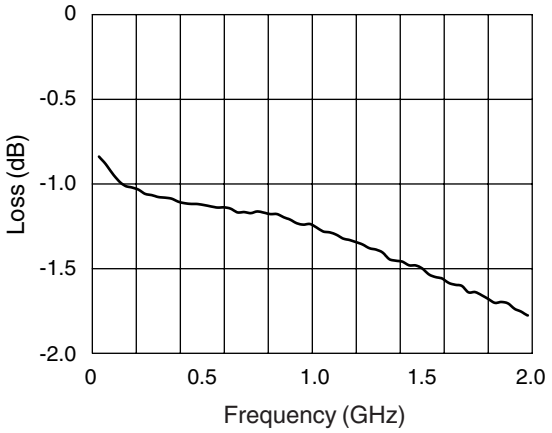
| Parameter[1] | Condition | Frequency[2] | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Insertion Loss[3] | | DC–1.0 GHz<br>DC–2.0 GHz | | 1.4<br>1.7 | 1.7<br>2.2 | dB<br>dB |
| Attenuation Range[4, 5] | | | | 15.5 | | dB |
| Attenuation Accuracy[4, 5] | | DC–1.0 GHz<br><br>DC–2.0 GHz | | ± (0.2 + 3% of Attenuation Setting in dB)<br>± (0.4 + 3% of Attenuation Setting in dB) | | dB<br><br>dB |
| VSWR (I/O) | | DC–2.0 GHz | | 1.4:1 | 1.8:1 | |
| Switching Characteristics[6] | Rise, Fall (10/90% or 90/10% RF)<br>On, Off (50% CTL to 90/10% RF)<br>Video Feedthru | | | 50<br>100<br>50 | | ns<br>ns<br>mV |
| Input Power for 1 dB Compression | | 0.50–2.0 GHz<br>0.05 GHz | +24<br>+17 | +29<br>+22 | | dBm<br>dBm |
| Intermodulation Intercept Point (IP3) | For Two-tone Input Power +5 dBm | 0.50–2.0 GHz<br>0.05 GHz | +44<br>+35 | +50<br>+40 | | dBm<br>dBm |
| Control Voltages | $V_{Low}$ = 0 to 0.2 V @ 20 µA Max.<br>$V_{High}$ = -5 V @ 300 µA Max. | | | | | |

## DC Electrical Characteristics at 25°C ($V_{CC}$ = +5 V)

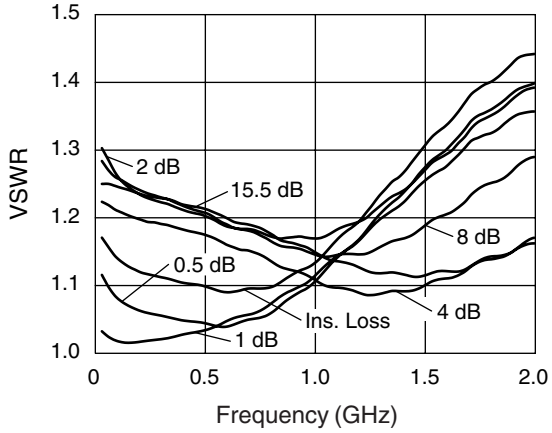
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Voltage High | $V_{IH}$ (1) | | 3.5 | 5.0 | V |
| Input Voltage Low | $V_{IL}$ (0) | 0 | 0.5 | | V |
| Input Leakage Current | $I_L$ | | ±0.5 | | µA |
| Quiescent Current | $I_{CC}$ | | 500 | | µA |
| Supply Voltages | $V_{CC}$ | | 5.0 | | V |

1. All measurements made in a 50 Ω system, unless otherwise specified.
2. DC = 300 kHz.
3. Insertion loss changes by 0.003 dB/°C.
4. Attenuation value referenced above insertion loss.
5. Exposed pad must be connected to RF ground to obtain specified attenuation.
6. Video feedthru measured with 1 ns risetime pulse and 500 MHz bandwidth.

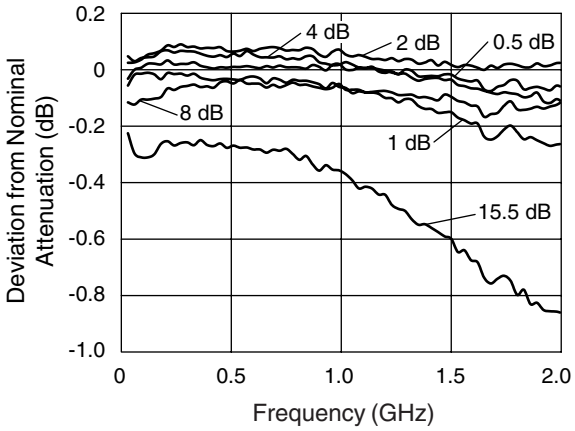
## Typical Performance Data ($V_{CC}$ = +5 V)




**Insertion Loss vs. Frequency**




**VSWR vs. Frequency**




**Attenuation Accuracy vs. Frequency**

## Absolute Maximum Ratings

| Characteristic | Value |
|---|---|
| Supply Voltage ($V_{CC}$) | -0.5 to +6 V |
| Input Voltage ($V_I$) | -0.5 – $V_{CC}$ + 0.5 V |
| Power Dissipation ($P_D$) | 500 mW |
| Storage Temperature ($T_{ST}$) | -65°C to +125°C |
| Operating Temperature ($T_{OP}$) | -40°C to +85°C |

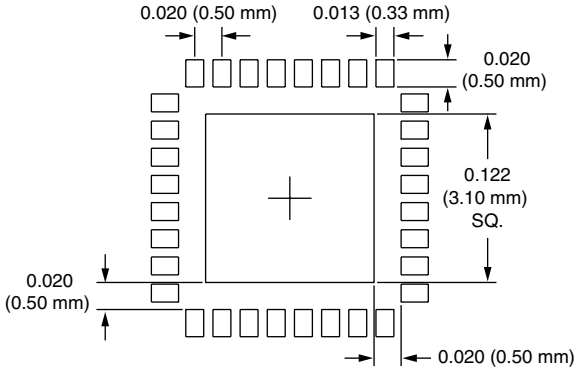
## Truth Table

| | Serial Data Input | | | | | $J_1$–$J_2$ |
|---|---|---|---|---|---|---|
| Reset | 0.5 dB | 1 dB | 2 dB | 4 dB | 8 dB | Attenuation |
| 1 | 0 | 0 | 0 | 0 | 0 | Insertion Loss |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.5 dB |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 dB |
| 1 | 0 | 0 | 1 | 0 | 0 | 2 dB |
| 1 | 0 | 0 | 0 | 1 | 0 | 4 dB |
| 1 | 0 | 0 | 0 | 0 | 1 | 8 dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 15.5 dB |
| 0 | X | X | X | X | X | Insertion Loss |

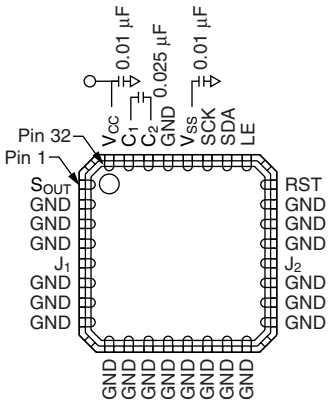
$V_{IL}$ (0) = 0 to 0.5 V.
$V_{IH}$ (1) = 3.5 to 5 V.
X = Don't Care.

## Surface Mount Land Pattern

**5 x 5 mm QFN 32 Lead**

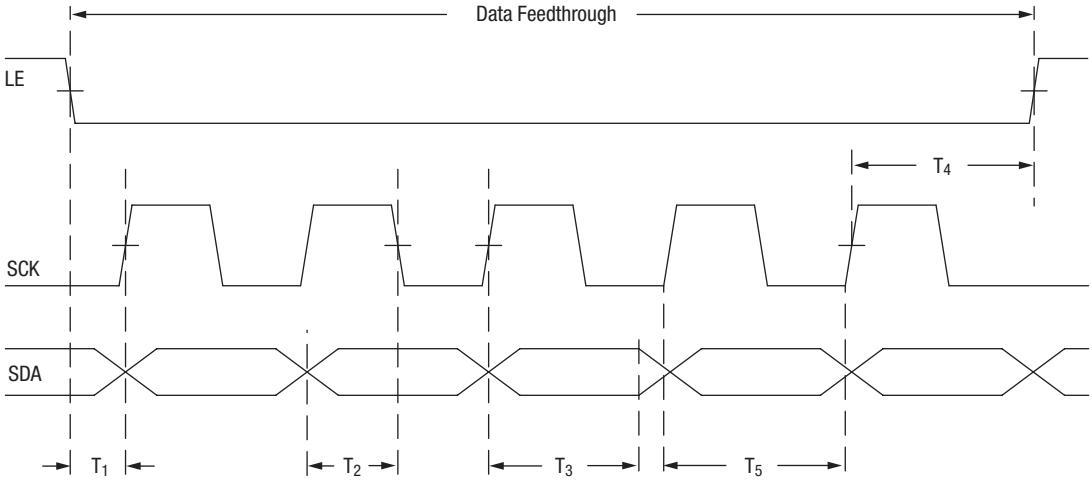



Dimensions in inches (mm).




| Pin | Symbol | Function |
|---|---|---|
| 1 | $S_{OUT}$ | Serial Data Output |
| 2–4 | GND | Ground |
| 5 | $J_1$ | RF Input/Output |
| 6–19 | GND | Ground |
| 20 | $J_2$ | RF Input/Output |
| 21–23 | GND | Ground |
| 24 | RST | Reset |
| 25 | LE | Latch Enable |
| 26 | SDA | Serial Data Input |
| 27 | SCK | Serial Clock Input |
| 28 | $V_{SS}$ | Low Output Voltage Level |
| 29 | GND | Ground |
| 30 | $C_2$ | Charge Pump Capacitor |
| 31 | $C_1$ | Charge Pump Capacitor |
| 32 | $V_{CC}$ | Supply Voltage |

## Timing Diagram




| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| LE Setup Time | $T_1$ | 5 | 15 | | ns |
| SDA Setup Time | $T_2$ | 5 | 15 | | ns |
| SDA Hold Time | $T_3$ | 5 | 10 | | ns |
| LE Hold Time | $T_4$ | 5 | 10 | | ns |
| Clock Frequency | $f_{CLK}$ | | 16 | 100 | MHz |
| Clock Period | $T_5$ | | $1/f_{CLK}$ | | |

Serial data is shifted into the register on the rising edge of the clock (SCK), MSB first. The rising edge of the LE signal will be the clock for the transfer of shifted data, causing the attenuator to change states.

Power-up sequence:

1. Connect ground
2. Apply $V_{CC}$
3. Set all inputs (SCK, SDA, LE)

Power-down sequence should be the reverse of above.