NEC

MOS INTEGRATED CIRCUIT

μPD461016L

1M-BIT BiCMOS FAST STATIC RAM
64K-WORD BY 16-BIT

Description

The μPD461016L is 1,048,576 bits (65,536 words by 16 bits), BiCMOS static RAMs. Operating supply voltage is 3.3 V $^{+0.3\ V}_{-0.15V}$ or 3.3 V ± 0.3 V.

The μPD461016L is packaged in a 44-pin plastic SOJ.

Features

- 65,536 words by 16 bits organization
- Output Enable input for easy application
- Byte data control
  $\overline{LB}$: I/O1 to I/O8, $\overline{UB}$: I/O9 to I/O16
- Fast access time

Ordering Information

Part number	Package	Word organization	Access time ns (MAX.)	Supply Voltage	Supply current mA (MAX.)	
					Operation	Standby
μPD461016LLE-A10	44-pin plastic SOJ (400 mil)	64K × 16 bits	10	3.3 V $^{+0.3\ V}_{-0.15\ V}$	260	70
μPD461016LLE-A11			11	3.3 V ± 0.3 V		
μPD461016LLE-A12			12			

Quality grade

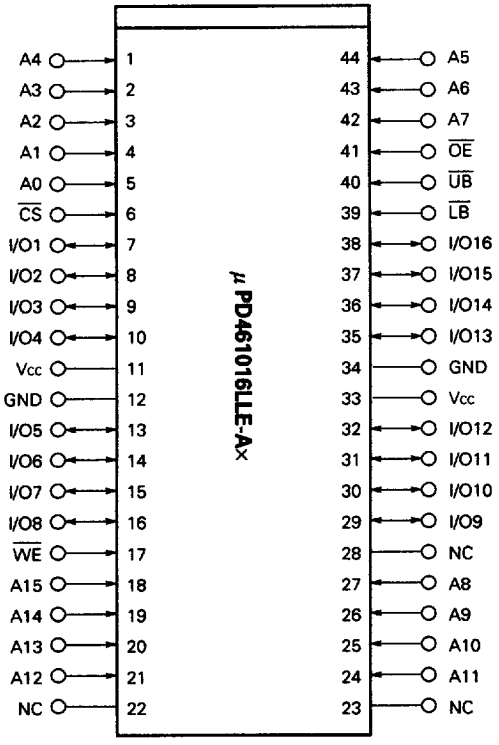
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration (Marking Side)

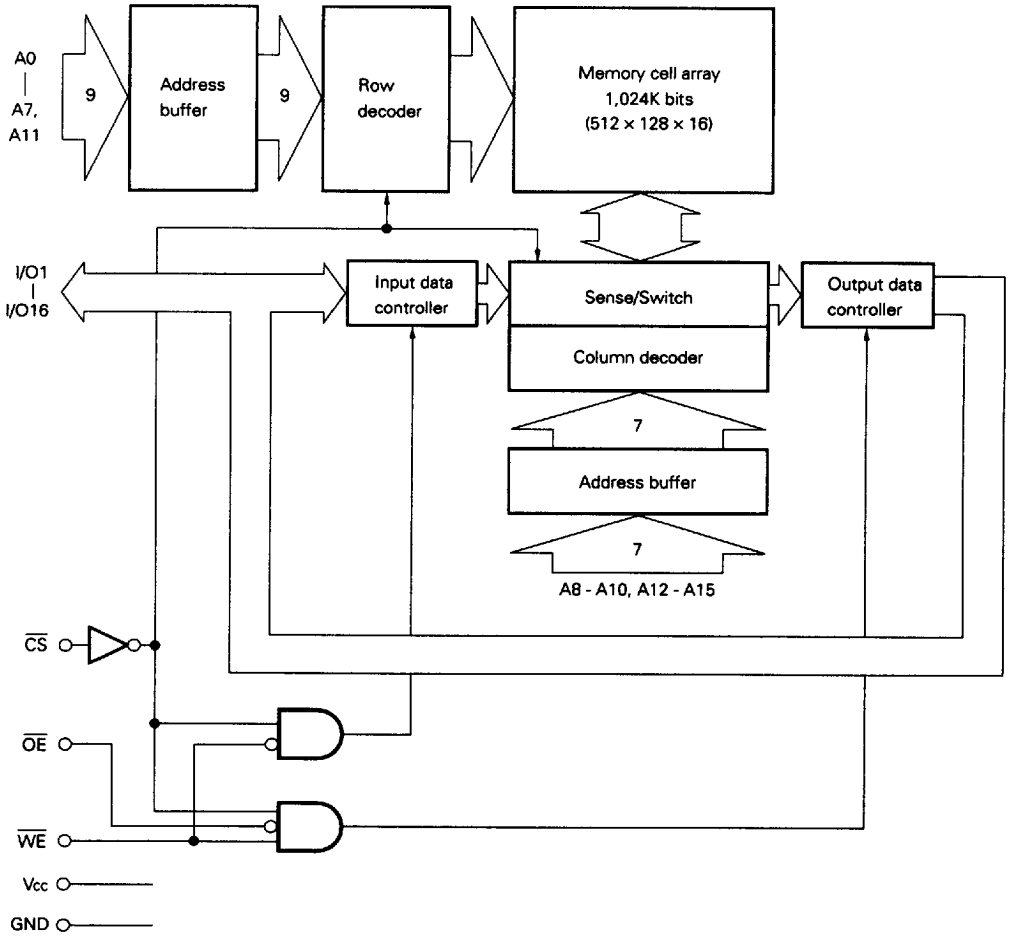
- **μPD461016L**

44-Pin Plastic SOJ (400 mil)



A0 to A15	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{CS}$	:	Chip Select
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
$\overline{LB}$, $\overline{UB}$	:	Byte data select
Vcc	:	Power supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Note		Supply current
						Lower I/O	Upper I/O	
H	×	×	×	×	Not selected	High impedance	High impedance	I_{SB}
L	L	H	L	L	Read	D_{OUT}	D_{OUT}	I_{CC}
			L	H		D_{OUT}	High impedance	
			H	L		High impedance	D_{OUT}	
L	×	L	L	L	Write	D_{IN}	D_{IN}	
			L	H		D_{IN}	High impedance	
			H	L		High impedance	D_{IN}	
L	H	H	×	×	Output disable	High impedance	High impedance	
L	×	×	H	H		High impedance	High impedance	

Note

Part number	Lower I/O	Upper I/O
μPD461016L	I/O1 - I/O8	I/O9 - I/O16

Remark ×: Don't care

Electrical Specifications

The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the following tables.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5[Note] to +4.6	V
Input voltage	V_{IN}	−0.5[Note] to V_{CC} +0.3	V
Input/Output voltage	$V_{I/O}$	−0.5[Note] to V_{CC}	V
Operating temperature	T_{opt}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note −1.0 V (MIN.) (Pulse width: 3 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μPD461016L-A10			μPD461016L-A11, 461016L-A12			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	3.15	3.3	3.6	3.0	3.3	3.6	V
High level input voltage	V_{IH}	2.0		V_{CC} + 0.3	2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}	− 0.5[Note]		+0.8	−0.5[Note]		+0.8	°C
Ambient temperature	T_a	0		70	0		70	°C

Note −1.0 V (MIN.) (Pulse width: 3 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		−10		+10	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{LB}$ = V_{IH} or $\overline{UB}$ = V_{IH}		−10		+10	μA
Operating supply current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	Cycle frequency ≤ 100 MHz			260	mA
			Cycle frequency = 0 MHz			220	
Standby supply current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}				100	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V				70	
High level output voltage	V_{OH}	I_{OH} = −2.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 4 mA				0.4	V

Remark V_{IN}: Input voltage

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF

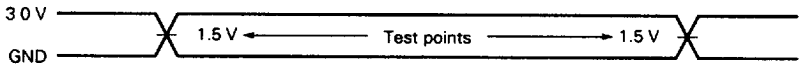
Remark 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

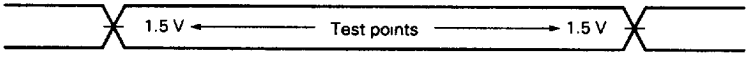
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/Fall Time: 2 ns)



Output waveform



Output load

AC characteristics directed with the **Note** should be measured with the following output load shown in **Fig. 1** and **Fig. 2.**

t_{AA}, t_{ACS}, t_{OE}, t_{ABD} and t_{OH} are measured with the output load shown in **Fig. 1.**

t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ} and t_{OW} are measured with the output load shown in **Fig. 2.**

Fig. 1 Output load

(For t_{AA}, t_{ACS}, t_{OE}, t_{ABD}, t_{OH})

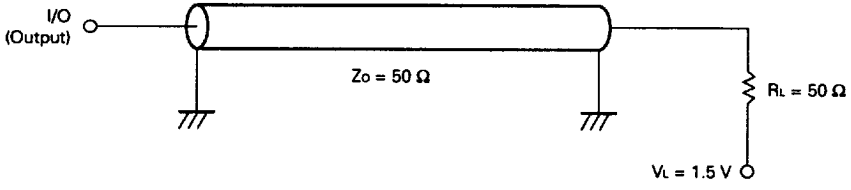
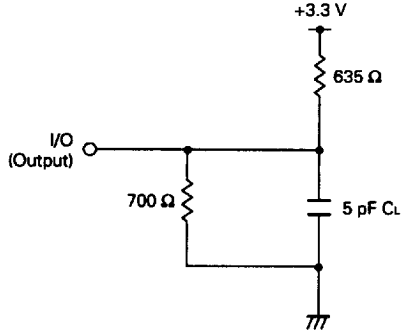


Fig. 2 Output load

(For t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ} and t_{OW})



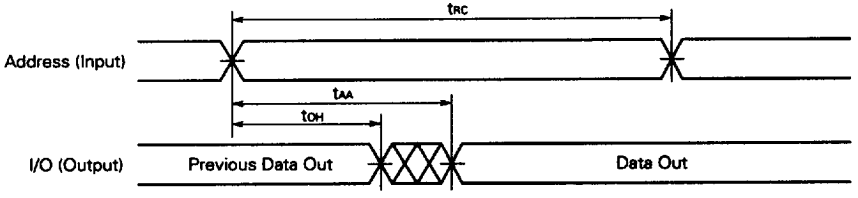
Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

Parameter	Symbol	μPD461016L-A10		μPD461016L-A11		μPD461016L-A12		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	10		11		12		ns	
Address access time	t_{AA}		10		11		12	ns	Note 1.
$\overline{CS}$ access time	t_{ACS}		10		11		12	ns	
$\overline{OE}$ access time	t_{OE}		5		5		6	ns	
$\overline{LB}$, $\overline{UB}$ access time	t_{ABD}		5		5		6	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
$\overline{CS}$ to output in low impedance	t_{CLZ}	3		3		3		ns	Note 2.
$\overline{OE}$ to output in low impedance	t_{OLZ}	1		1		1		ns	
$\overline{LB}$, $\overline{UB}$ to output in low impedance	t_{BLZ}	1		1		1		ns	
$\overline{CS}$ to output in high impedance	t_{CHZ}		5		5		6	ns	
$\overline{OE}$ to output hold in high impedance	t_{OHZ}		5		5		6	ns	
$\overline{LB}$, $\overline{UB}$ to output hold in high impedance	t_{BHZ}		5		5		6	ns	

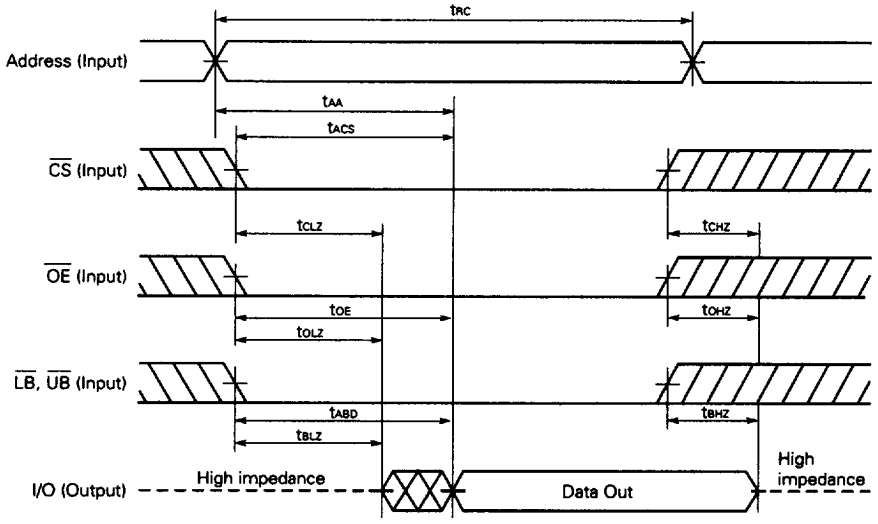
Note 1. See the output load shown in **Fig. 1.**
2. See the output load shown in **Fig. 2.**

Read Cycle Timing Chart 1 (Address Access)



Remark 1. In read cycle, $\overline{WE}$ should be fixed to high level.
2. $\overline{CS}$ = $\overline{OE}$ = $\overline{LB}$ (or $\overline{UB}$) = V_{IL}

Read Cycle Timing Chart 2 ($\overline{CS}$ Access)



Caution Address valid prior to or coincident with $\overline{CS}$ low level input.

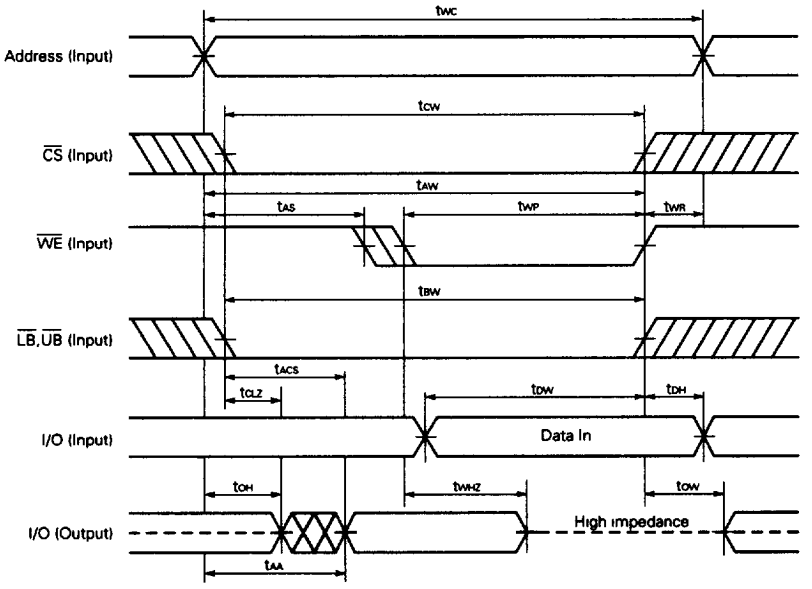
Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle

Parameter	Symbol	μPD461016L-A10		μPD461016L-A11		μPD461016L-A12		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	10		11		12		ns	
$\overline{CS}$ to end of write	t_{CW}	8		9		10		ns	
Address valid to end of wirte	t_{AW}	8		9		10		ns	
Write pulse width	t_{WP}	8		9		10		ns	
$\overline{LB}$, $\overline{UB}$ to end of write	t_{BW}	8		9		10		ns	
Data valid to end of write	t_{DW}	6		7		8		ns	
Data hold time	t_{DH}	0		0		0		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		5		5		6	ns	**Note**
Output active from end of write	t_{OW}	3		3		3		ns	

Note See the output load shown in **Fig. 2.**

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



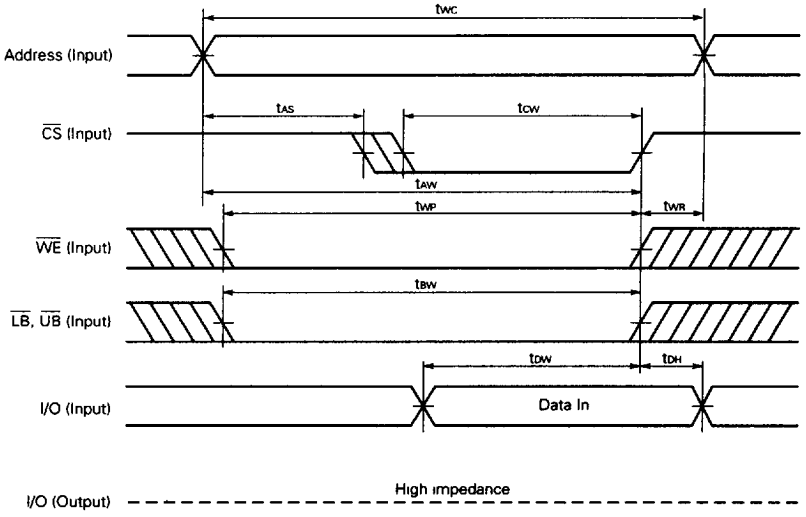
Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark 1. Write operation is done during the overlap time of low level $\overline{CS}$, low level $\overline{WE}$ and low level $\overline{LB}$ (or low level $\overline{UB}$).

2. During t_{WHZ}, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

3. When $\overline{WE}$ is at low level, the I/O pins are always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.

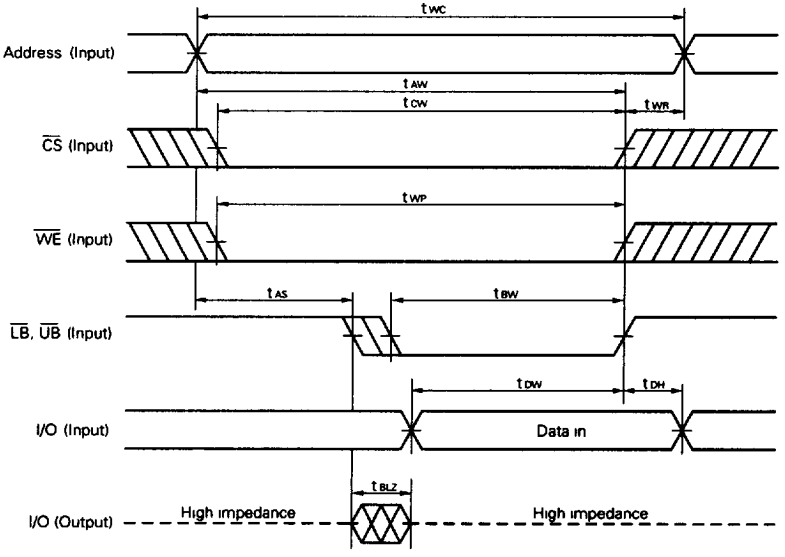
Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)



Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$, low level $\overline{WE}$ and low level $\overline{LB}$ (or low level $\overline{UB}$).

Write Cycle Timing Chart 3 ($\overline{LB}$, $\overline{UB}$ Controlled)

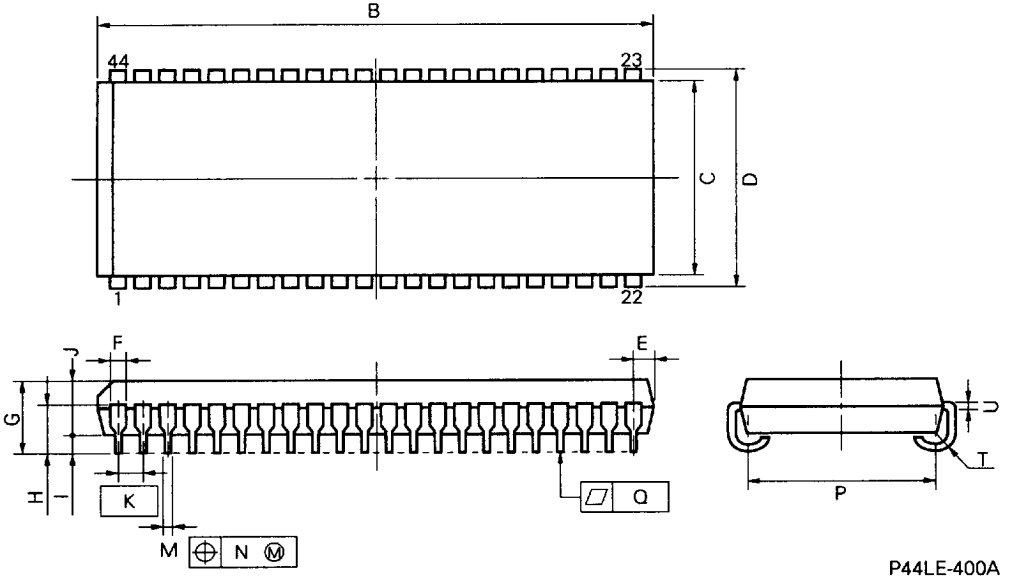


Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$, low level $\overline{WE}$ and low level $\overline{LB}$ (or low level $\overline{UB}$).

Package Drawings

44 PIN PLASTIC SOJ (400 mil)



P44LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$28.73^{+0.2}_{-0.35}$	$1.131^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.20	0.440±0.008
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.3±0.2	$0.091^{+0.008}_{-0.009}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD461016L.

Types of Surface Mount Device

μPD461016LLE : 44-pin plastic SOJ (400 mil)