

Description

The μPD431004 is a 262,144-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431004 a high-speed device that requires very low power and no clock or refreshing.

The μPD431004 is available in standard 28-pin plastic SOJ packaging.

Features

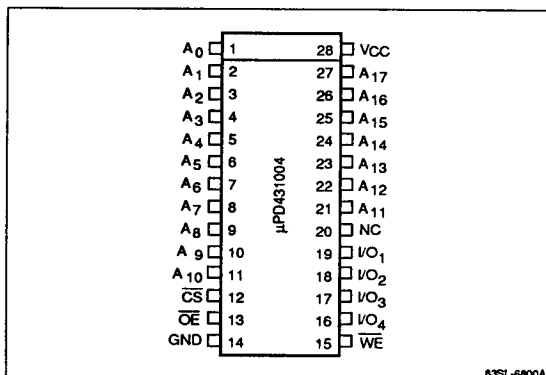
- 262,144-word x 4-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
 - 150 mA max (active)
 - 2 mA max (standby)
- Standard 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD431004LE-20	20 ns	28-pin plastic SOJ
LE-25	25 ns	
LE-35	35 ns	

Pin Configuration

28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A ₀ - A ₁₇	Address inputs
I/O ₁ - I/O ₄	Data inputs and outputs
CS	Chip select
WE	Write enable
GND	Ground
V _{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{CC}	- 0.5 to + 7.0 V
Input and output voltages, V_{IN} (Note 1)	- 0.5 to V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to + 70°C
Storage temperature, T_{STG}	- 55 to + 125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = -3.0 V minimum for 10 ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz (Note 1)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	I_{CC}
Not selected	H	X	X	High-Z	Standby
Output disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Notes:

(1) X = don't care.

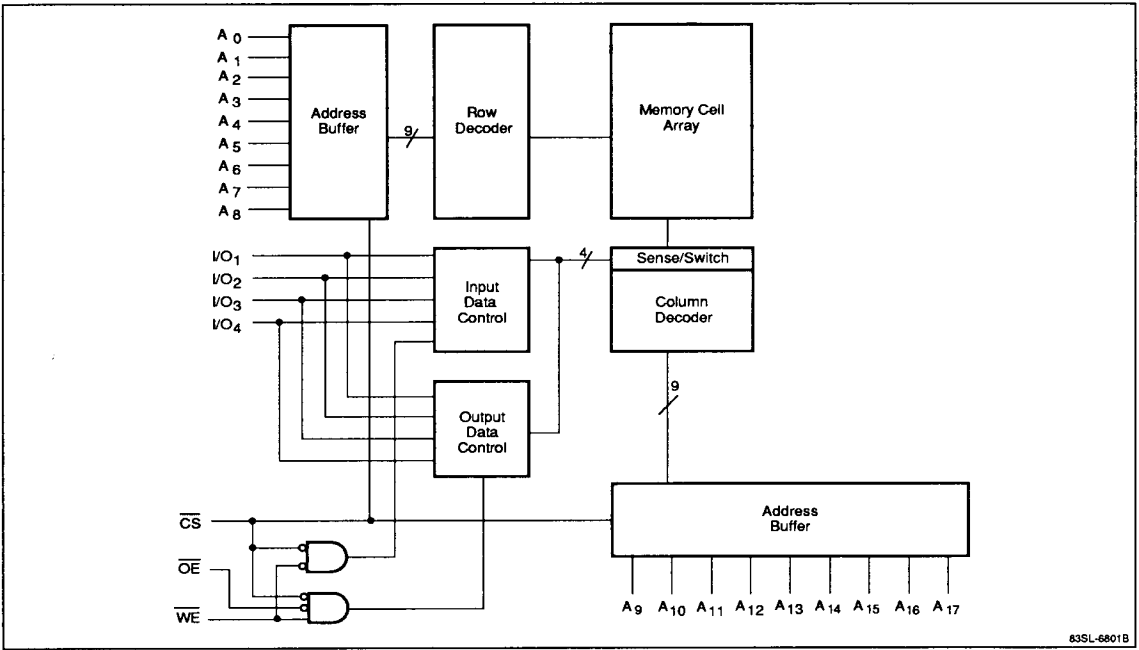
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	- 0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = -3.0 V minimum for 10 ns pulse.

Block Diagram



DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	-2		2	μA	$V_{IN} = 0 \text{ V to } V_{CC}$
Output leakage current	I_{LO}	-2		2	μA	$V_{OUT} = 0 \text{ V to } V_{CC}$; $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$
Standby supply current	I_{SB}			30	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$; $V_{IN} \leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0 \text{ mA}$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0 \text{ mA}$

AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	μPD431004-20		μPD431004-25		μPD431004-35		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Read Operation									
Operating supply current	I _{CC}		150		140		120	mA	$\overline{CS} = V_{IL}; t_{RC} = t_{RC}(\text{min}); I_{DOUT} = 0 \text{ mA}$
Read cycle time	t _{RC}	20		25		35		ns	(Note 2)
Address access time	t _{AA}		20		25		35	ns	
Chip select access time	t _{ACS}		20		25		35	ns	
Output hold from address change	t _{OH}	5		5		5		ns	
Output enable access time	t _{OE}		10		10		15	ns	
Output enable to output in low-Z	t _{OLZ}	0		0		0		ns	(Note 3)
Output disable to output in high-Z	t _{OHZ}	0	8	0	10	0	15	ns	(Note 4)
Chip selection to output in low-Z	t _{CLZ}	5		5		5		ns	(Note 3)
Chip selection to output in high-Z	t _{CHZ}	0	8	0	10	0	15	ns	(Note 4)
Write Operation									
Write cycle time	t _{WC}	20		25		35		ns	(Note 2)
Chip select to end of write	t _{CW}	15		20		30		ns	
Address valid to end of write	t _{AW}	15		20		30		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	15		20		30		ns	
Write recovery time	t _{WR}	3		3		3		ns	
Data valid to end of write	t _{DW}	12		12		20		ns	
Data hold time	t _{DH}	0		0		0		ns	
Write enable to output in high-Z	t _{WHZ}	0	8	0	8	0	10	ns	(Note 4)
Output active from end of write	t _{OW}	0		0		0		ns	(Note 3)

Notes:

- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.
- (2) All read cycle timings are referenced from the last valid address to the first transitioning address.
- (3) Transition is measured at $\pm 200 \text{ mV}$ from steady-state voltage with the load shown in figure 2.
- (4) Transition is measured at $V_{OL} + 200 \text{ mV}$ and $V_{OH} - 200 \text{ mV}$ with the load shown in figure 2.

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Figure 1. Output Load

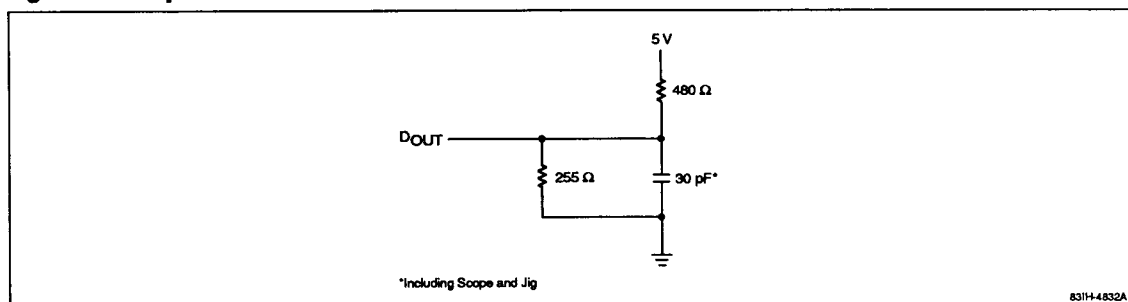
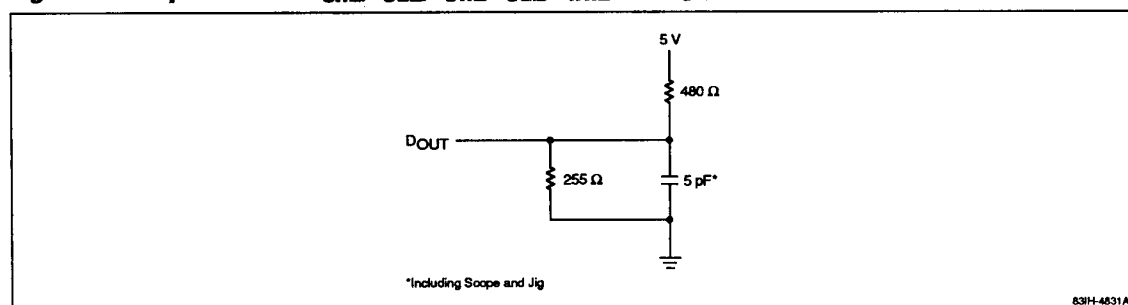
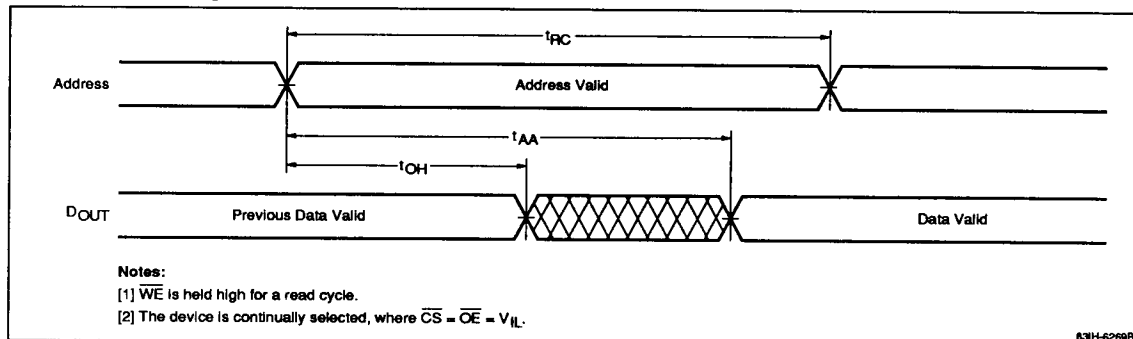


Figure 2. Output Load for t_{CHZ} , t_{CLZ} , t_{OHZ} , t_{OLZ} , t_{WHZ} , and t_{OW}

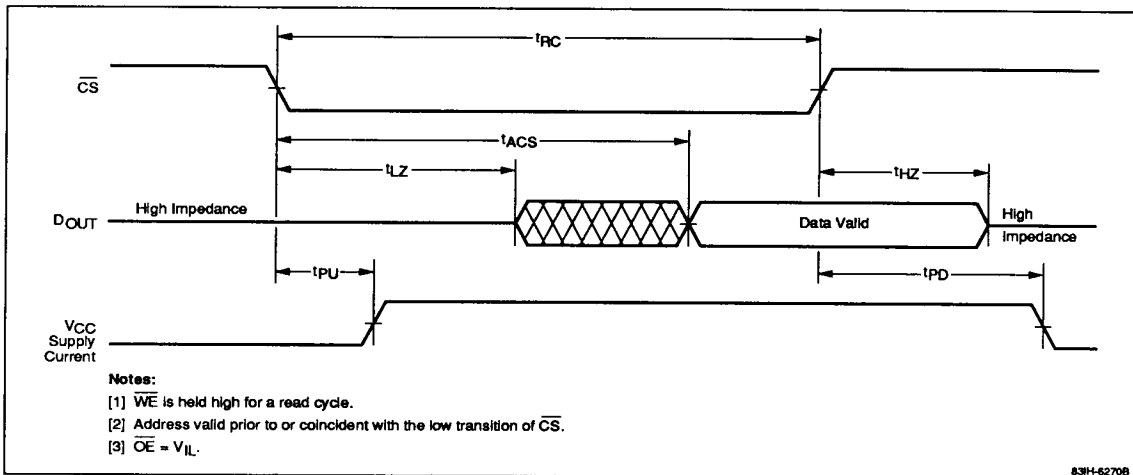


Timing Waveforms

Address Access Cycle



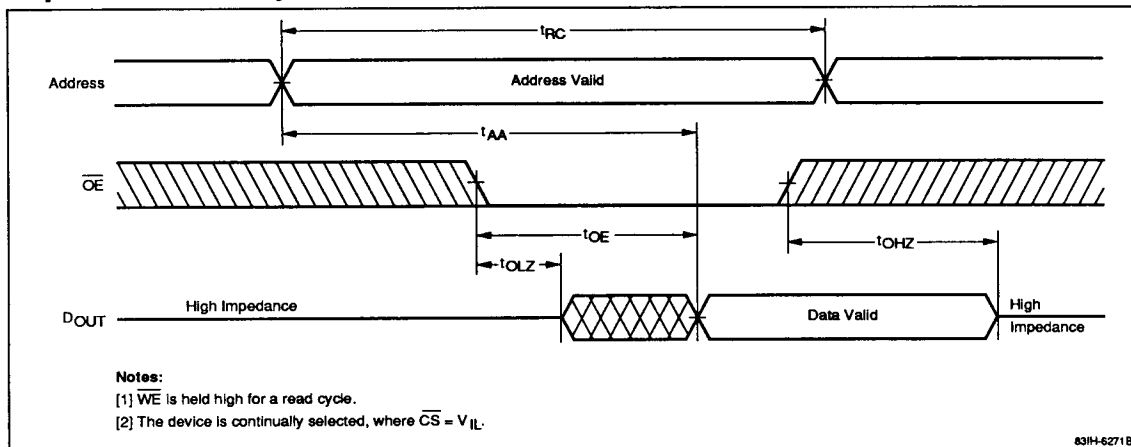
Chip Select Access Cycle



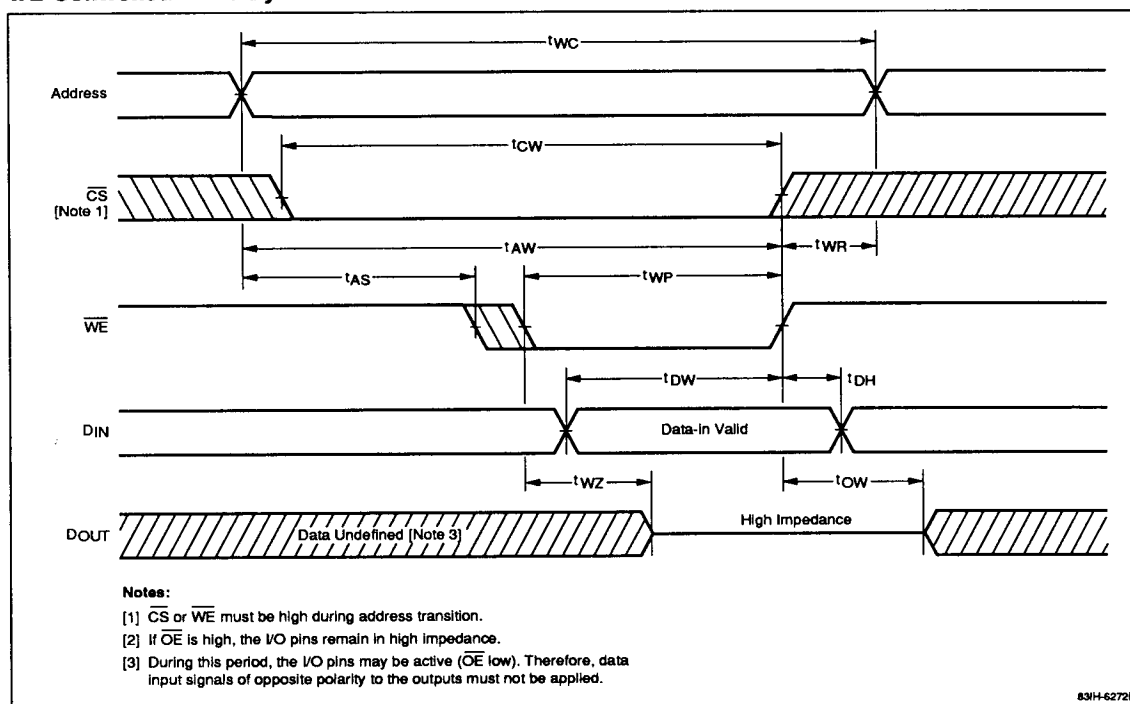
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Timing Waveforms (cont)

Output Enable Access Cycle

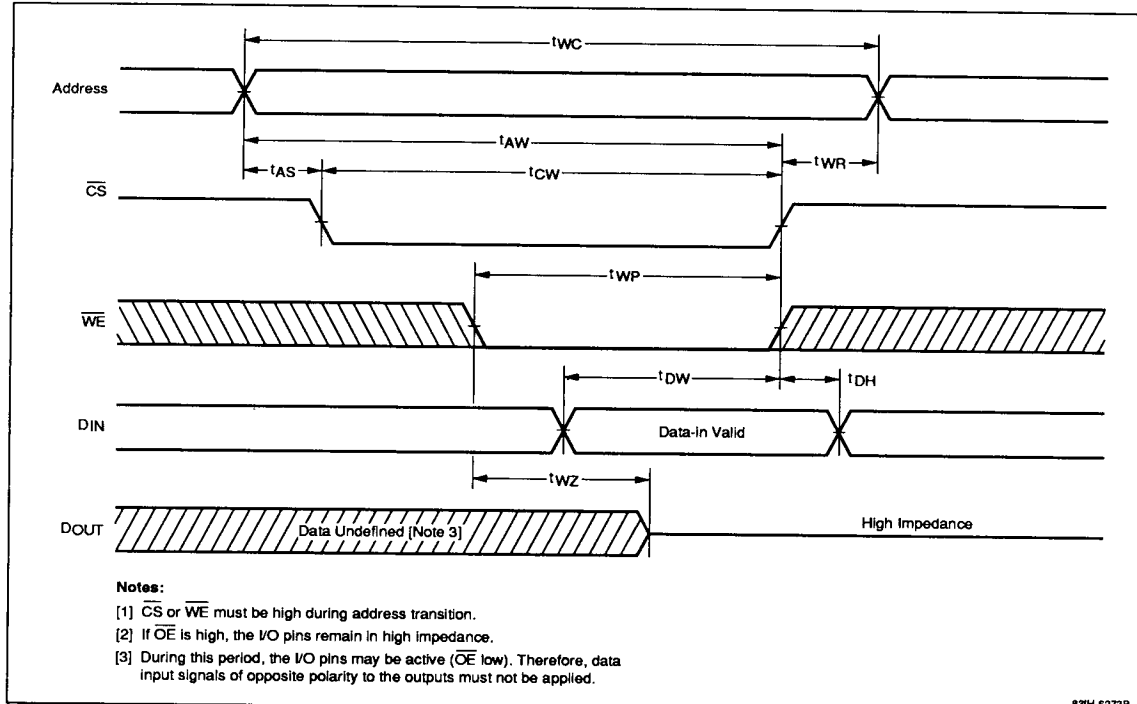


$\overline{WE}$ -Controlled Write Cycle



Timing Waveforms (cont)

$\overline{CS}$ -Controlled Write Cycle



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