NEC Electronics Inc.

μPD424440/L, 42S4440/L
1,048,576 x 4-Bit Dynamic CMOS RAM With Four $\overline{CAS}$ controls

Description

The μPD424440/L and μPD42S4440/L are fast-page dynamic RAMs organized as 1,048,576 words by 4 bits and designed to operate from a single power supply. The four $\overline{CAS}$ controls, $\overline{CAS}_1$ - $\overline{CAS}_4$, are paired with I/O_1 - I/O_4

Optional features are power supply voltage (+5 V or +3.3 V) and a new refresh mode called "self-refresh."

μPD	Options
424440	+5 V
424440L	+3.3 V
42S4440	+5 V; self-refresh mode
42S4440L	+3.3 V; self-refresh mode

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O_{1-4} pins are controlled by $\overline{CAS}_{1-4}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by maintaining $\overline{CAS}$ low. The output returns to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RAS}$-only refresh cycles will also refresh all memory locations.

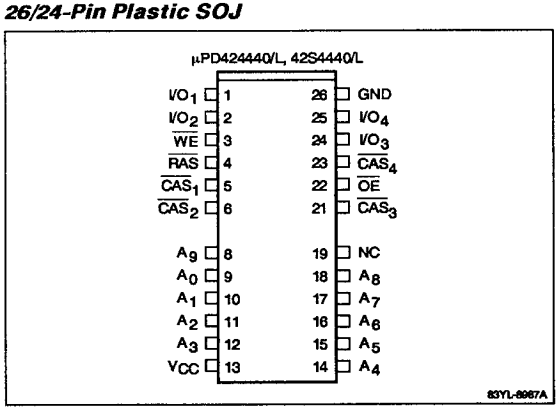
The self-refresh mode is entered by holding $\overline{RAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 microamperes. Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Features

- 1,048,576 by 4-bit organization
- Single power supply (+5-volt or +3.3-volt)
- Self-refresh option (slow internal automatic refresh)
- Fast-page option
- Low power dissipation
- Four I/O and $\overline{CAS}$ pairs
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/24-pin (350-mil) plastic SOJ package

Pin Configuration

26/24-Pin Plastic SOJ



Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}_1$ - $\overline{CAS}_4$	Column address strobes
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt or +3.3-volt power supply
NC	No connection

5h

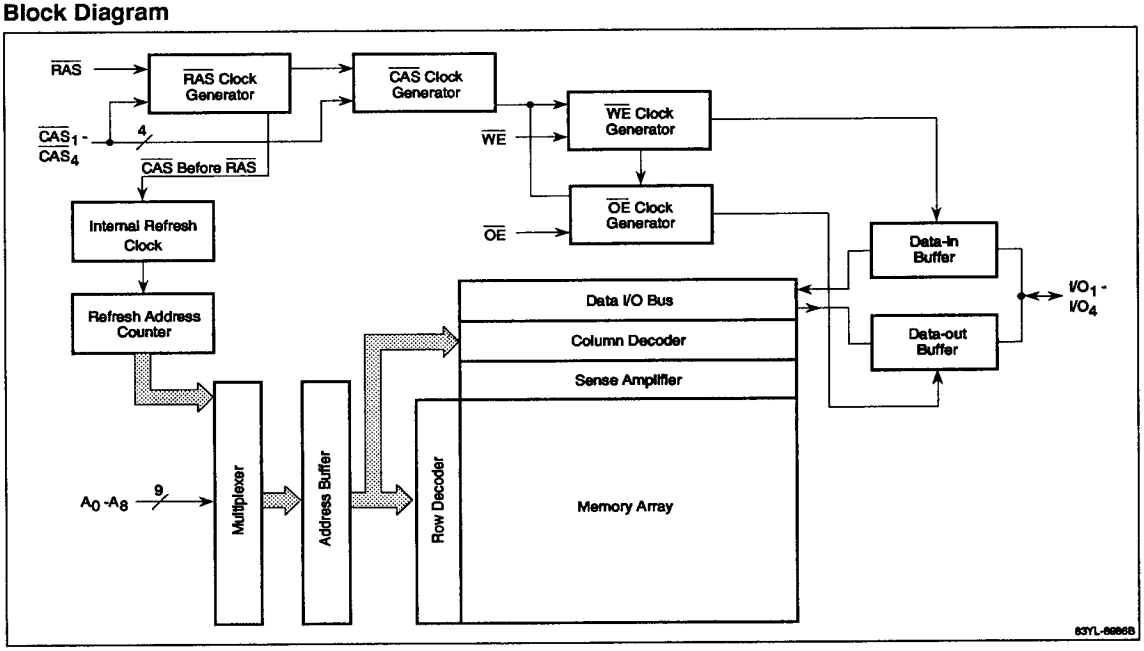
Ordering Information, Standard Devices

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	Power Supply	$\overline{CAS}$ Access Time (max)	Package
μPD424440LE-60	60 ns	40 ns	+5 V	20 ns	26/24-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD424440LLE-60	60 ns	40 ns	+3.3 V		
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			

Ordering Information, Self-Refresh Devices

Part Number	$\overline{RAS}$ Access Time (max)	Fast-Page Cycle Time (max)	Power Supply	$\overline{CAS}$ Access Time (max)	Package
μPD42S4440LE-60	60 ns	40 ns	+5 V	20 ns	26/24-pin plastic SOJ
LE-70	70 ns	45 ns			
LE-80	80 ns	50 ns			
μPD42S4440LLE-A60	60 ns	40 ns	+3.3 V		
LE-A70	70 ns	45 ns			
LE-A80	80 ns	50 ns			

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	
+5-volt devices	−1.0 to +7.0 V
+3.3-volt devices	−0.5 to +4.6 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	
+5-volt devices	50 mA
+3.3-volt devices	20 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{CAS}_1$ - $\overline{CAS}_4$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

Recommended Operating Conditions

		+5-Volt Devices			+3.3-Volt Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	2.0		V_{CC} +0.3	V
Input voltage, low	V_{IL}	−1.0		0.8	−0.5		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	3.0	3.3	3.6	V
Ambient temperature	T_A	0		+70	0		+70	°C

Self-Refresh Current

T_A = 0 to +70°C; V_{CC} = +5 V ±10% (42S4440) or +3.3 V ±0.3 V (42S4440L)

Symbol	42S4440	42S4440L	Conditions
I_{CC7}	300 μA max	100 μA max	I/O pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. Other input pins: $V_{IH} \geq V_{CC} - 0.2$ V; $V_{IL} \leq 0.2$ V or open. $t_{RAS} \geq 100$ μs

5h

DC Characteristics; +5-Volt Devices

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				300	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

DC Characteristics; +3.3-Volt Devices

T_A = 0 to +70°C; V_{CC} = +3.3 V ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			500	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				100	μA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–5		5	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–5		5	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.0 mA

AC Characteristics

T_A = 0 to +70°C

V_{CC} = +5.0 V ±10% or +3.3 V ±0.3 V

		-60		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1} (+5)		90		80		70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 3)
	I_{CC1} (+3.3)		80		70		60		
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (+5)		90		80		70	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 3)
	I_{CC3} (+3.3)		80		70		60		
Operating current, fast-page cycle, average	I_{CC4} (+5)		80		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 3)
	I_{CC4} (+3.3)		70		60		50		
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (+5)		90		80		70	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 3)
	I_{CC5} (+3.3)		80		70		60		
Access time from column address	t_{AA}		30		35		40	ns	(Notes 4, 5, 7)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45	ns	(Notes 4, 5, 7)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		20		20	ns	(Notes 4, 5, 7)
Column address hold time	t_{CAH}	15		15		15		ns	
Delay time, column address to $\overline{CAS}$ high	t_{CAL}	30		35		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		15		ns	
$\overline{CAS}$ hold time (CBR self-refresh mode)	t_{CHS}	–35		–40		–50		ns	Self-refresh devices
Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	t_{CLCH}	5		5		5		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		12		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55		60		75		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		ns	
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in hold time	t_{DH}	15		15		15		ns	
Data-in setup time	t_{DS}	0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		20	ns	(Notes 4, 5, 7)
$\overline{OE}$ data delay time	t_{OED}	15		15		15		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	(Note 8)
Output disable from $\overline{CAS}$ high	t_{OFF}	0	15	0	15	0	20	ns	(Note 8)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 5)
Fast-page read or write cycle time	t_{PC}	40		45		50		ns	(Note 6)
Fast-page read-modify-write cycle time with exended data output	t_{PRWC}	85		90		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	(Notes 4, 5, 7)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	(Note 7)
Row address hold time	t_{RAH}	10		10		10		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ pulse width (CBR self-refresh mode)	t_{RASS}	100		100		100		μs	Self-refresh devices
Random read or write cycle time	t_{RC}	120		130		150		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	ns	(Note 7)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_8
			128		128		128	ms	Self-refresh devices

5h

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ precharge time (CBR self-refresh mode)	t_{RPS}	120		130		150		ns	Self-refresh devices
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		25		ns	
Read-modify-write cycle time	t_{RWC}	165		175		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		ns	
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		ns	
Rise and fall times	t_T	3	50	3	50	3	50	ns	
Write command hold time	t_{WCH}	15		15		15		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
Write command pulse width	t_{WP}	15		15		15		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume t_T = 5 ns.

(5) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max); if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(8) t_{OFF} (max) defines the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) Parameter t_{WP} is applicable for late-write or read-modify-write cycles. In early-write cycles, t_{WCH} (min) should be satisfied.

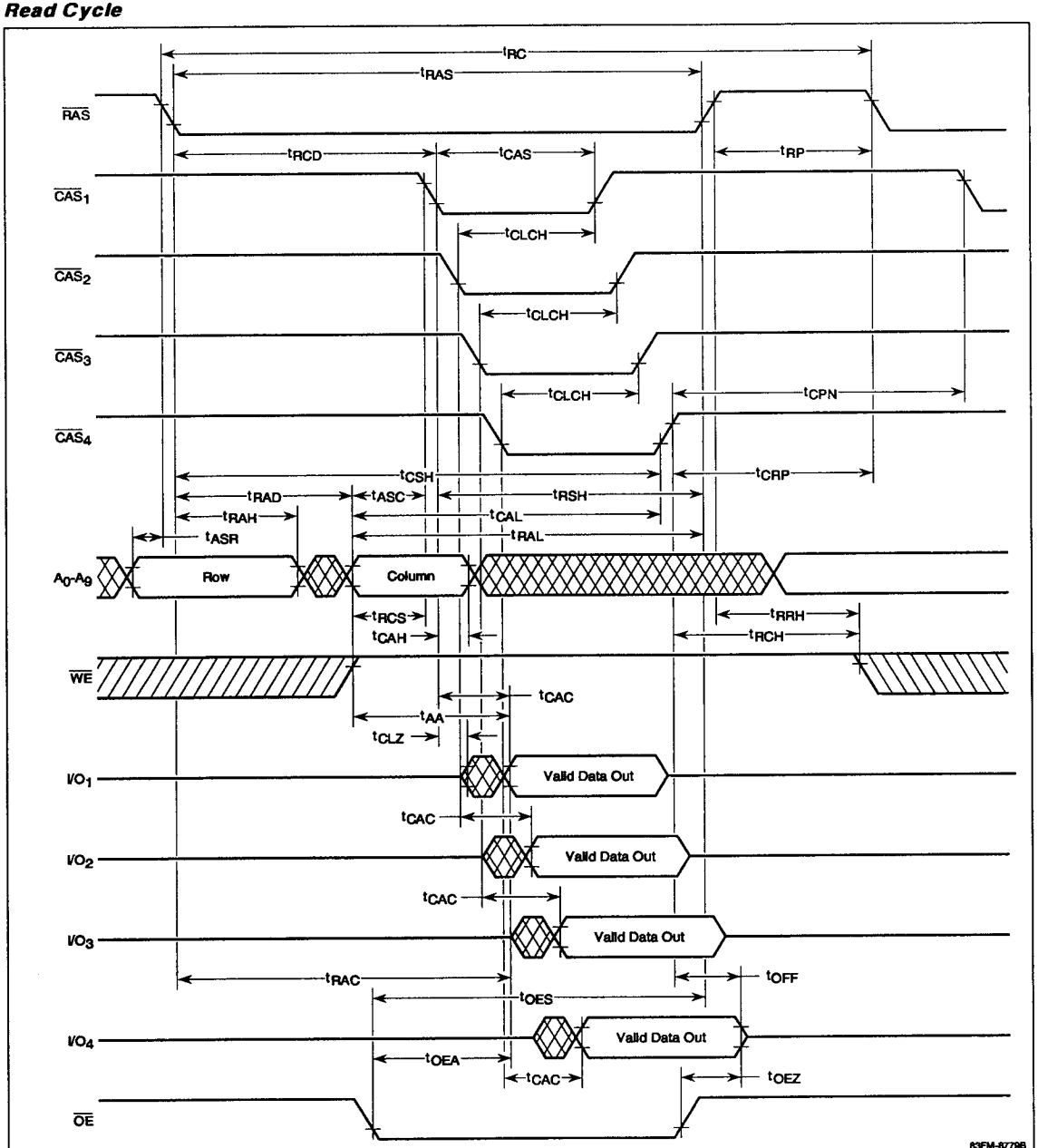
(11) These parameters are referenced to the leading edge of one of the $\overline{CAS}$ signals in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(12) These parameters are the conditions defining read-modify-write cycles.

(13) Load = 2 TTl (−1 mA, +4 mA) loads and 100 pF. For 3.3-volt devices, V_{OH} = 2.0 V and V_{OL} = 0.8 V (ac reference levels).

Timing Waveforms

Read Cycle



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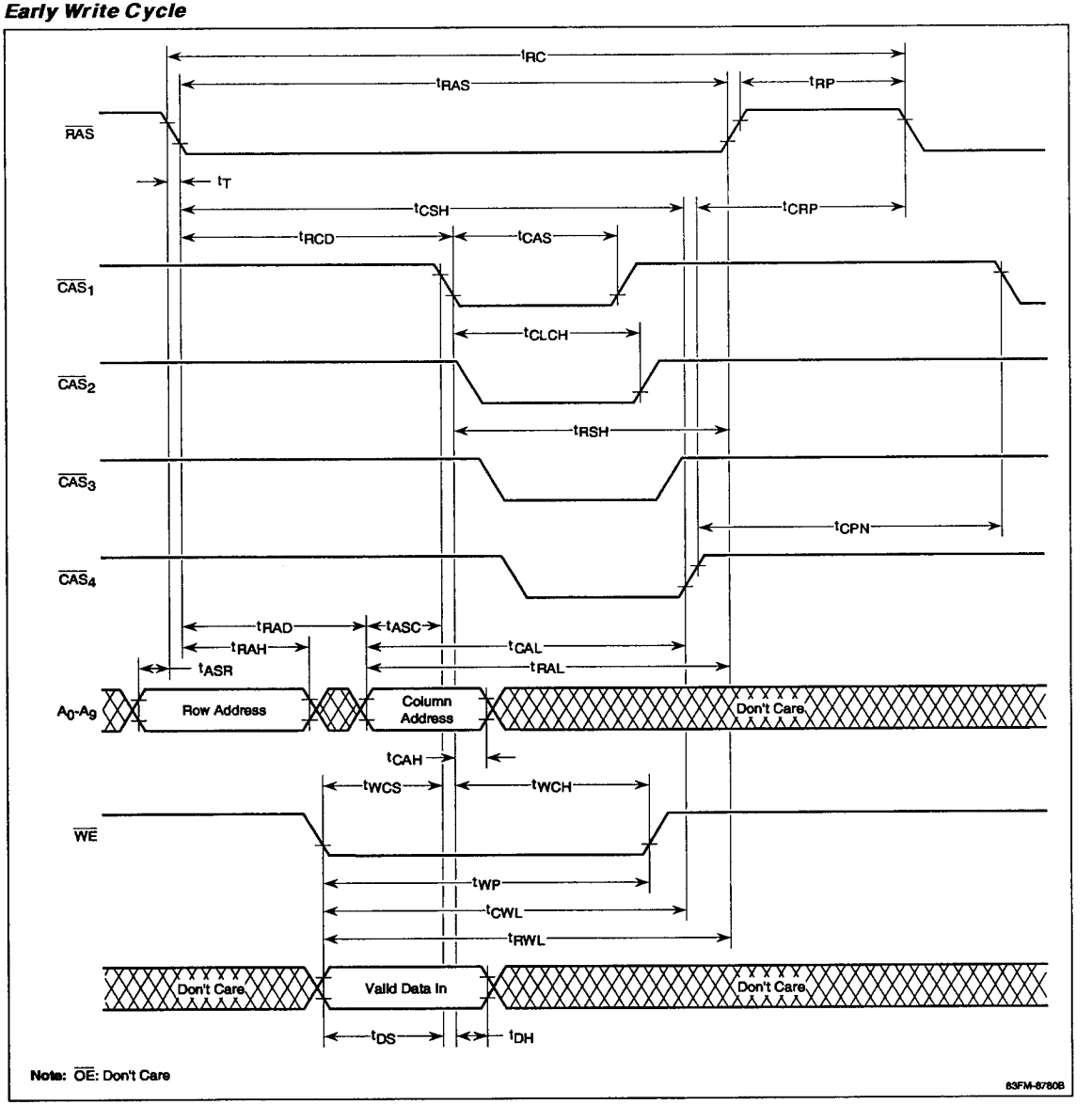
Timing Waveforms (cont)

Early Write Cycle



Note: $\overline{OE}$: Don't Care

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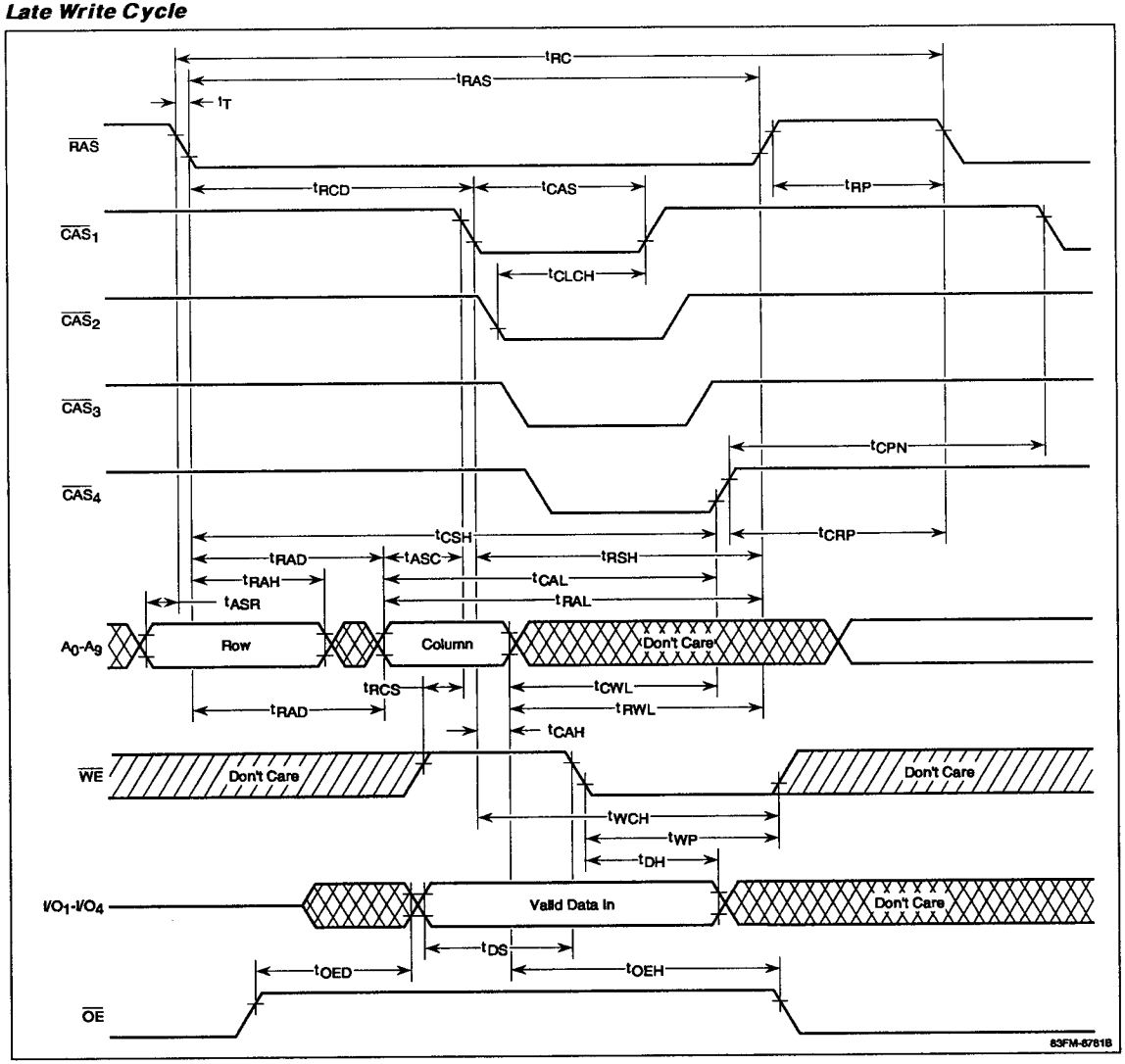
Timing Waveforms (cont)

Late Write Cycle



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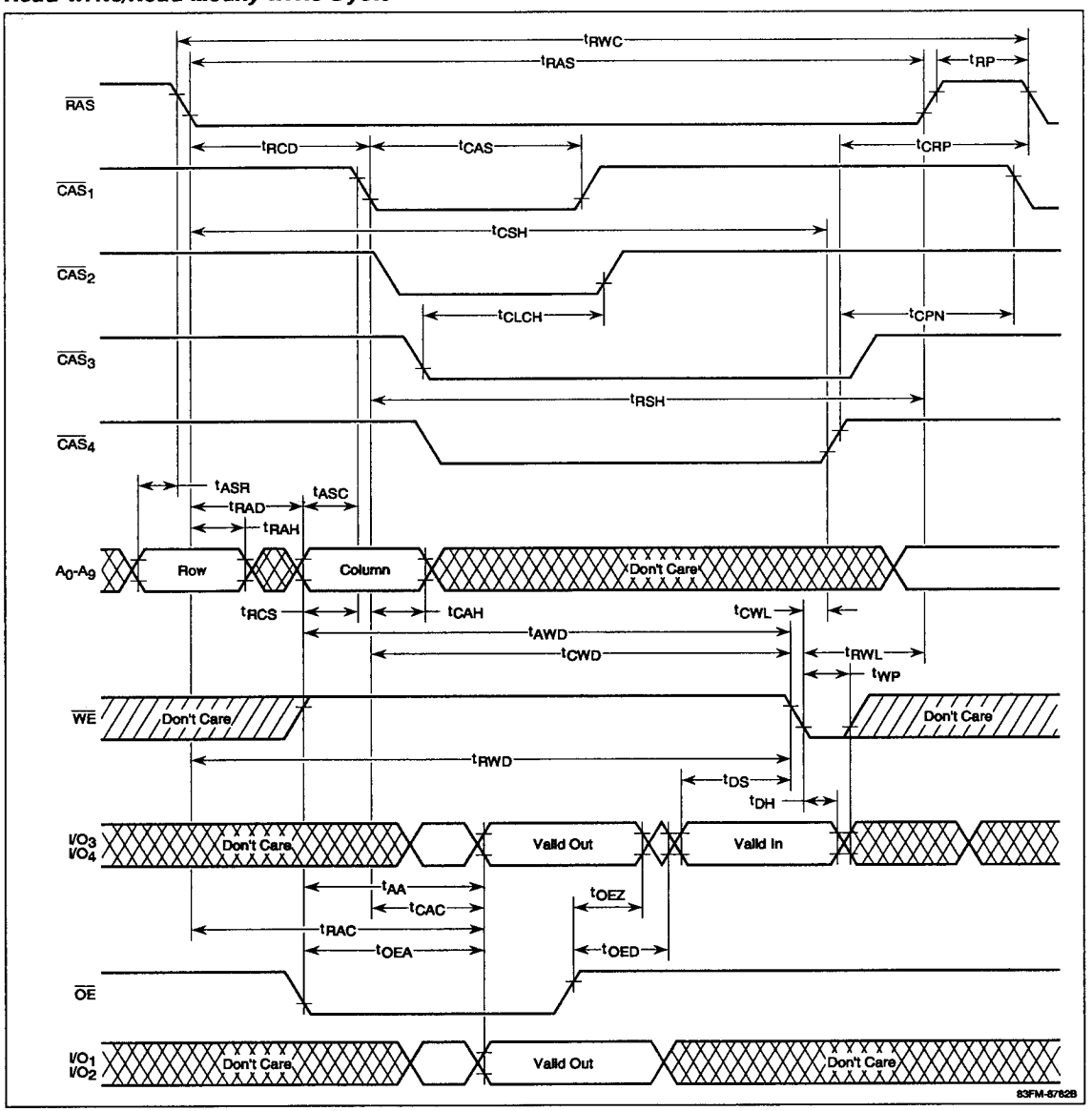
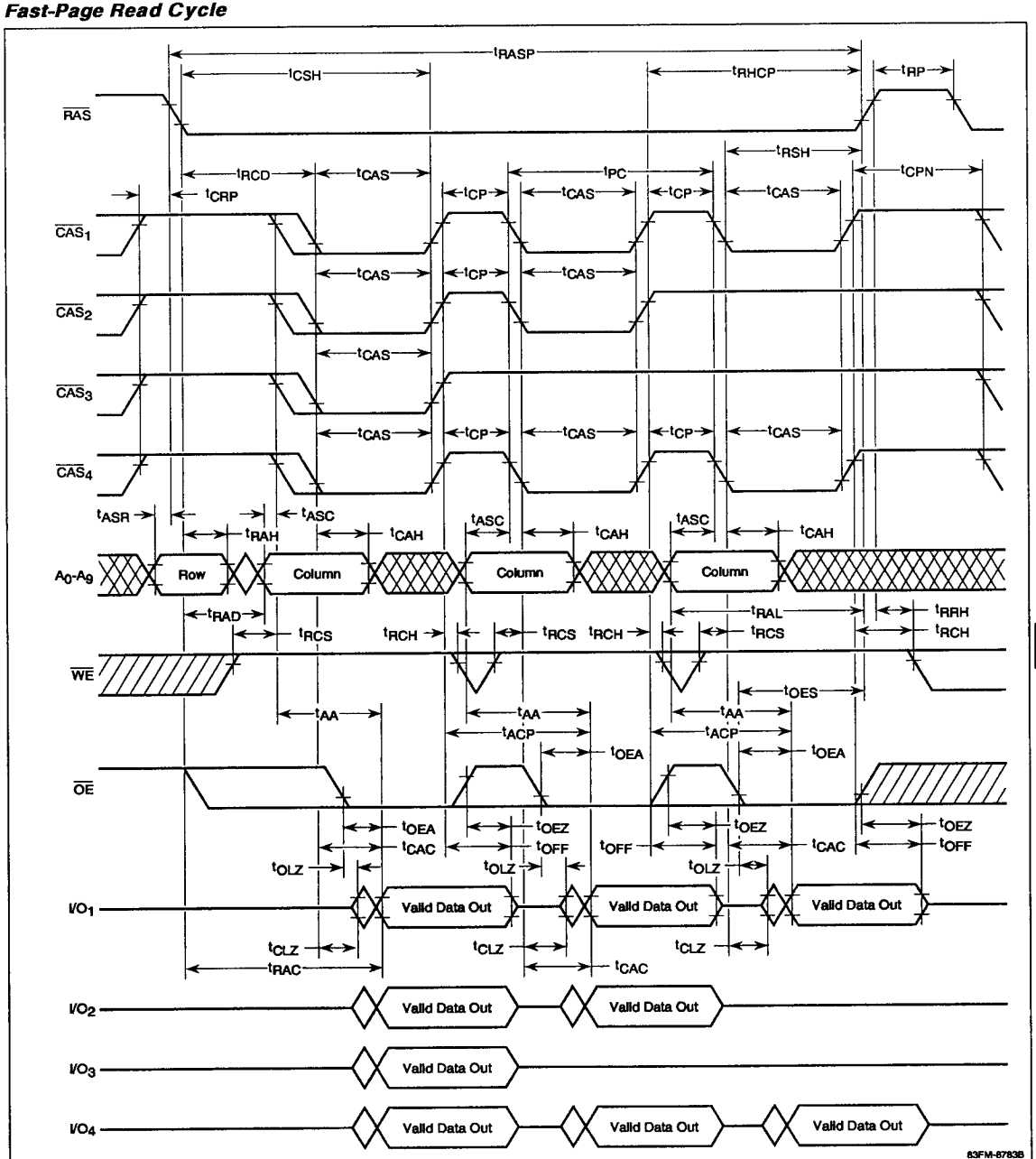
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Fast-Page Read Cycle



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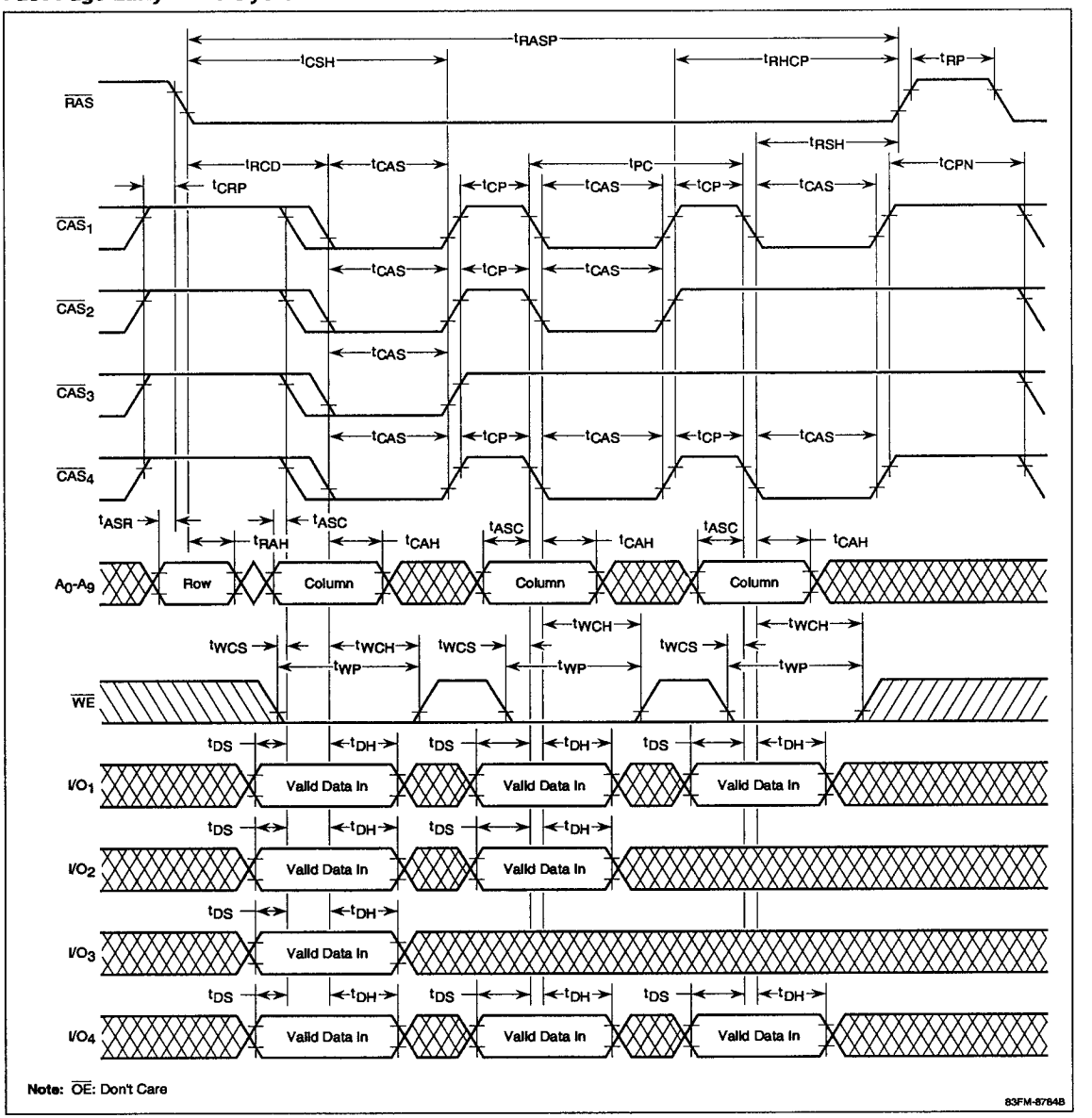
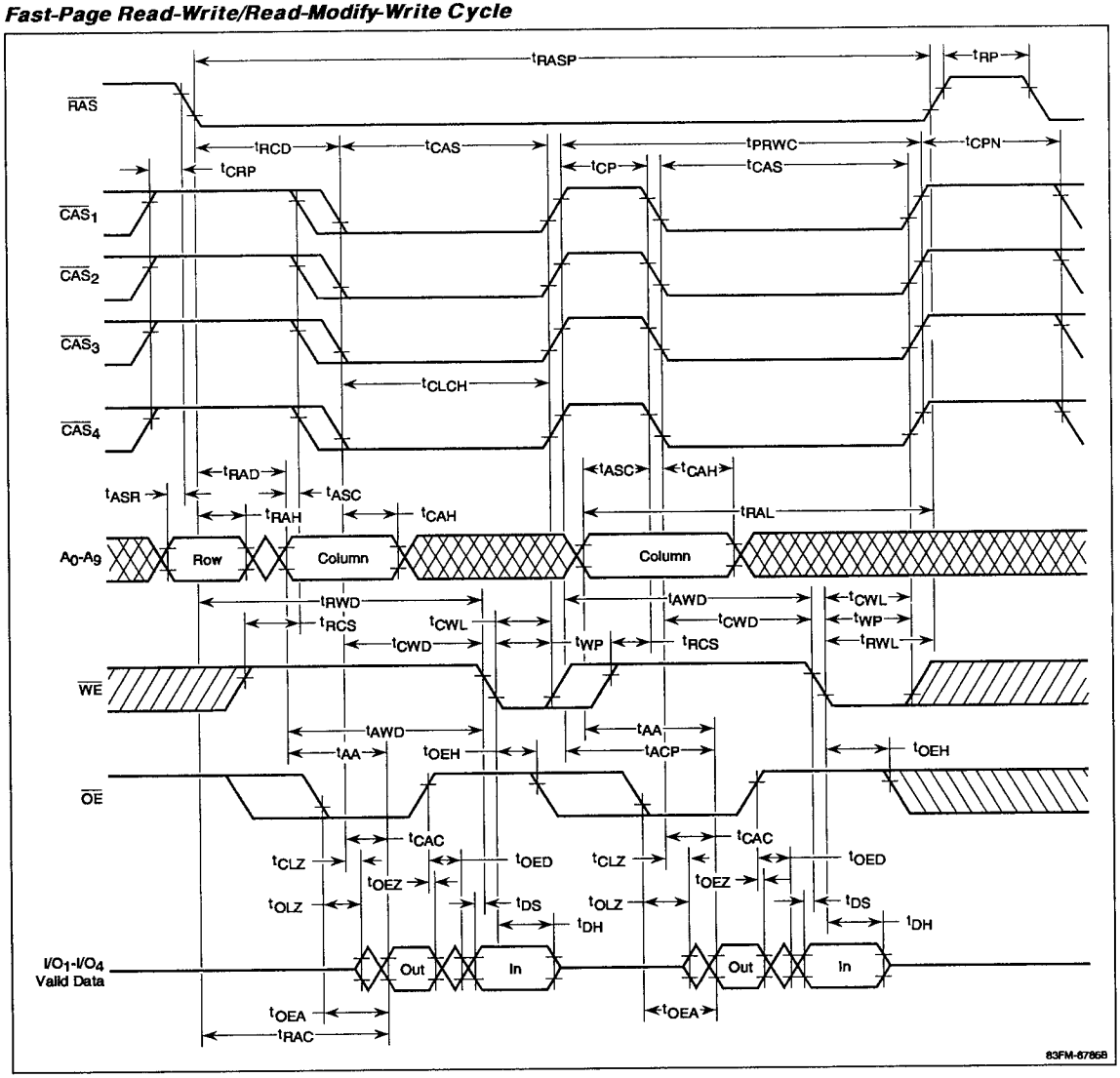
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



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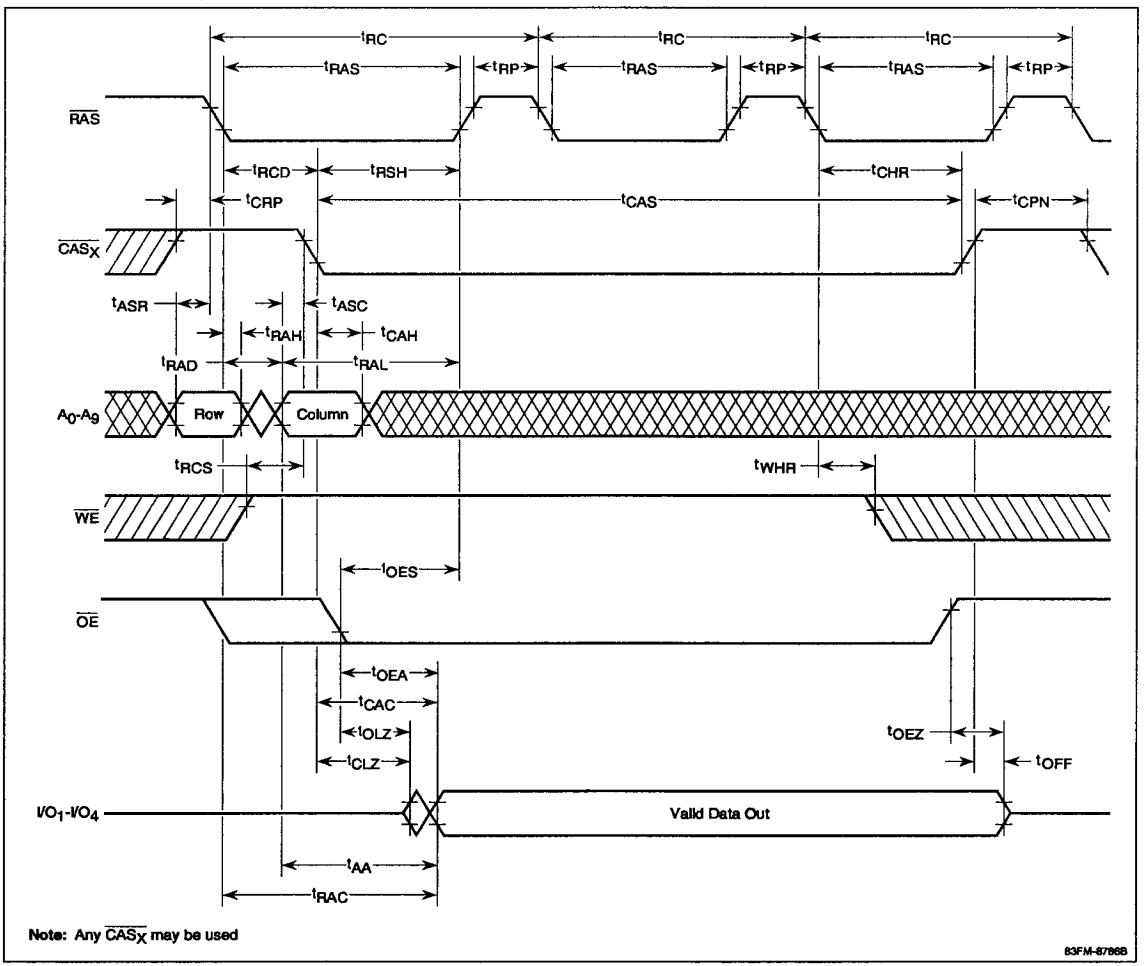
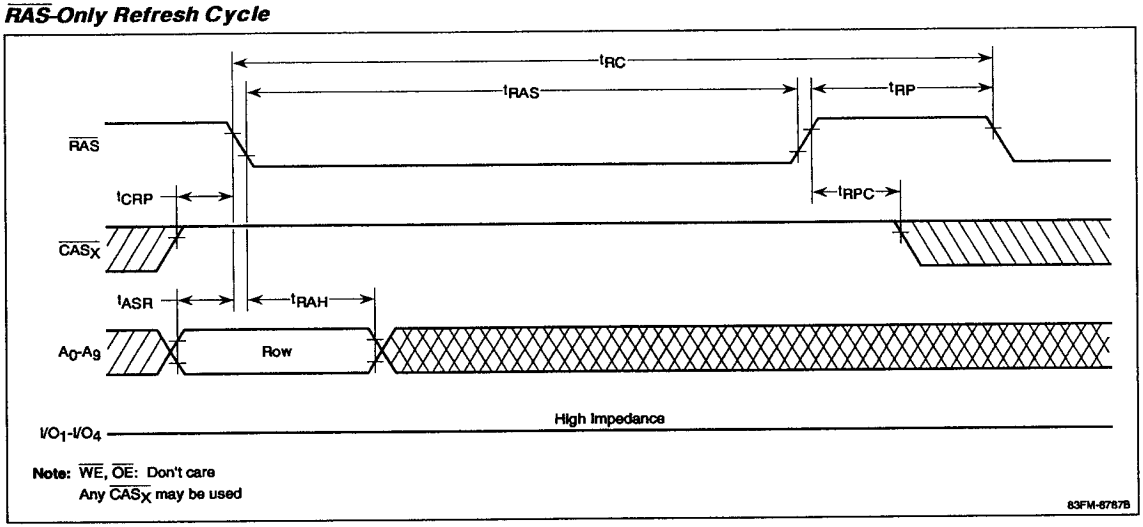
Timing Waveforms (cont)

Hidden Refresh Cycle

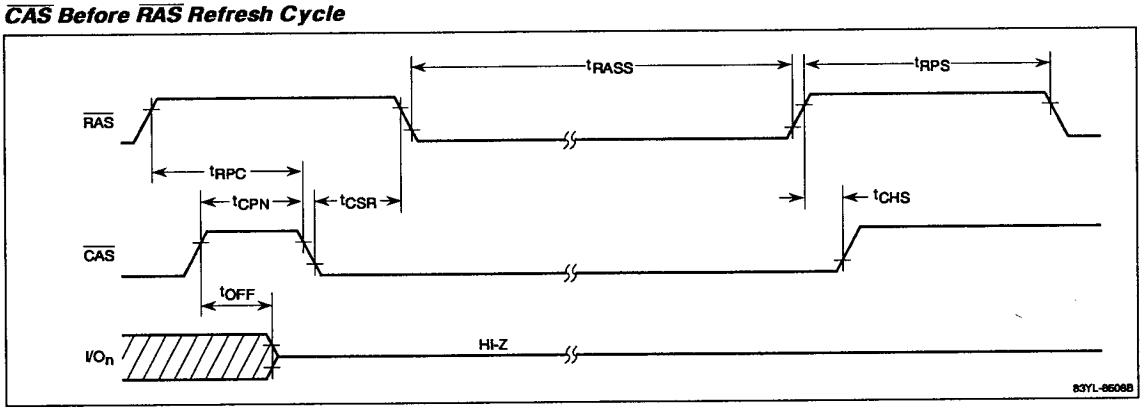


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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Timing Waveforms (cont)

CBR Self-Refresh Cycle