# μPD421x160/L, 42S1x160/L (x = 6, 7, 8) 1,048,576 x 16-Bit Dynamic CMOS RAM

T-46-23-18

## Description

The devices listed below are fast-page dynamic RAMs organized as 1M words by 16 bits and designed to operate from a single power supply. Optional features are power supply voltage (+5 V or +3.3 V), a new refresh mode called "self-refresh," and the number of cycles in a refresh period.

| μPD | Power | Self-Refresh | Refresh Cycles |
|---|---|---|---|
| 4216160 | +5 V | — | 4096 in 64 ms |
| 160L | +3.3 V | — | |
| 42S16160 | +5 V | √ | 4096 in 256 ms |
| 160L | +3.3 V | √ | |
| 4217160 | +5 V | — | 2048 in 32 ms |
| 160L | +3.3 V | — | |
| 42S17160 | +5 V | √ | 2048 in 256 ms |
| 160L | +3.3 V | √ | |
| 4218160 | +5 V | — | 1024 in 16 ms |
| 160L | +3.3 V | — | |
| 42S18160 | +5 V | √ | 1024 in 256 ms |
| 160L | +3.3 V | √ | |

**Note:** Letters L and S denote 3.3-volt and self-refresh devices, respectively.

Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{UCAS}$ and $\overline{LCAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, upper or lower byte data is held on the outputs by maintaining $\overline{UCAS}$ or $\overline{LCAS}$ low. Data outputs return to high impedance when $\overline{UCAS}$ or $\overline{LCAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{UCAS}$ or $\overline{LCAS}$.

Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh addresses.

For the 4216/42S16, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 4096 address combinations of $A_0$ - $A_{11}$ will refresh all memory locations. Bits $A_0$ - $A_{11}$ are used for row and refresh addresses, $A_0$ - $A_7$ for column addresses.

For the 4217/42S17, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 2048 address combinations of $A_0$ - $A_{10}$ will refresh all memory locations. Bits $A_0$ - $A_{10}$ are used for row and refresh addresses, $A_0$ - $A_8$ for column addresses.

For the 4218/42S18, $\overline{RAS}$ only refresh cycles and normal read or write cycles on the 1024 address combinations of $A_0$ - $A_9$ will refresh all memory locations. Bits $A_0$ - $A_9$ are used for row, refresh, and column addresses.

The self-refresh mode is entered by holding $\overline{RAS}$ and $\overline{CAS}$ low for longer than 100 μs during a CBR cycle. Detection of this long $\overline{RAS}$ time starts an internal oscillator that maintains data integrity without external clocking. The slow refresh reduces the data hold current to less than 200 μA (+5 V) or 80 μA (+3.3 V). Self-refresh mode is used with microprocessors that have a "sleep mode" for low-power applications such as notebook PCs.

Battery backup current $I_{CC6}$ is defined as the current consumption when the device is in standby mode ($\overline{RAS} \geq V_{CC} - 0.2$ V) and very-slow (extended) CBR cycles are being performed.

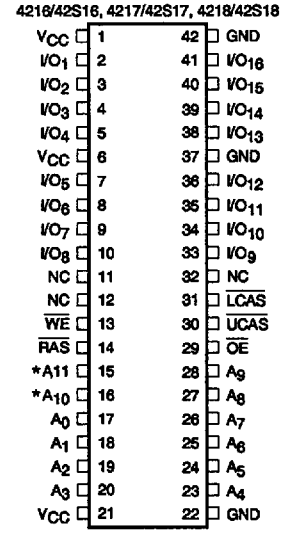
## Features

- 1,048,576 by 16-bit organization
- Single power supply: +5-volt or +3.3-volt
- Fast-page option
- Low-power operation
- Byte read/write control with $\overline{UCAS}$ and $\overline{LCAS}$
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Self-refresh option (slow internal automatic refresh)
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched three-state outputs
- Low input capacitance
- Multiplexed row and column addresses
- 42-pin SOJ and 50/44-pin TSOP plastic packages

## Pin Configurations

### *42-Pin Plastic SOJ*

4216/42S16, 4217/42S17, 4218/42S18




* Pin 15 is NC for 4217/42S17 and 4218/42S18
Pin 16 is NC for 4218/42S18.

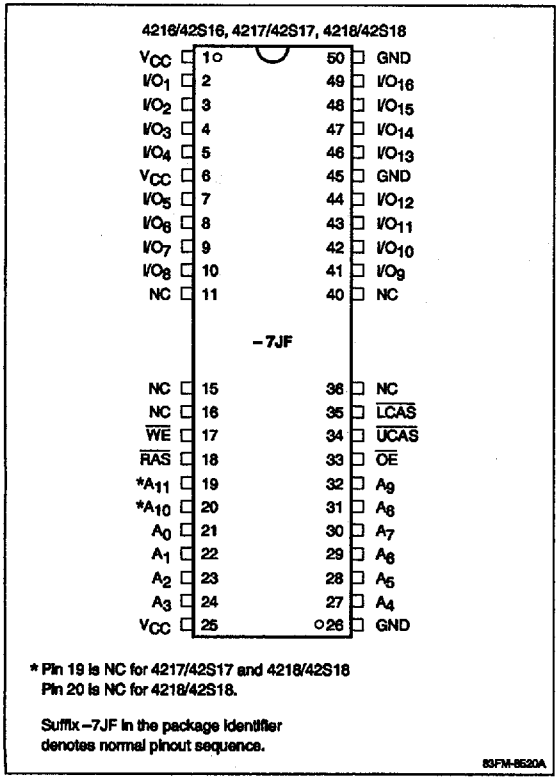
83FM-0524A

## Pin Identification

| Name | Function |
|---|---|
| $A_0$ - $A_{11}$ | Address inputs |
| $I/O_1$ - $I/O_{16}$ | Data inputs and outputs |
| $\overline{LCAS}$, $\overline{UCAS}$ | Column address strobes |
| $\overline{OE}$ | Output enable |
| $\overline{RAS}$ | Row address strobe |
| $\overline{WE}$ | Write enable |
| GND | Ground |
| $V_{CC}$ | +5-volt or +3.3-volt power supply |
| NC | No connection |

## Pin Configurations (cont)

### 50/44-Pin Plastic TSOP (Normal Pinouts)




* Pin 19 is NC for 4217/42S17 and 4218/42S18
Pin 20 is NC for 4218/42S18.

Suffix –7JF in the package identifier denotes normal pinout sequence.

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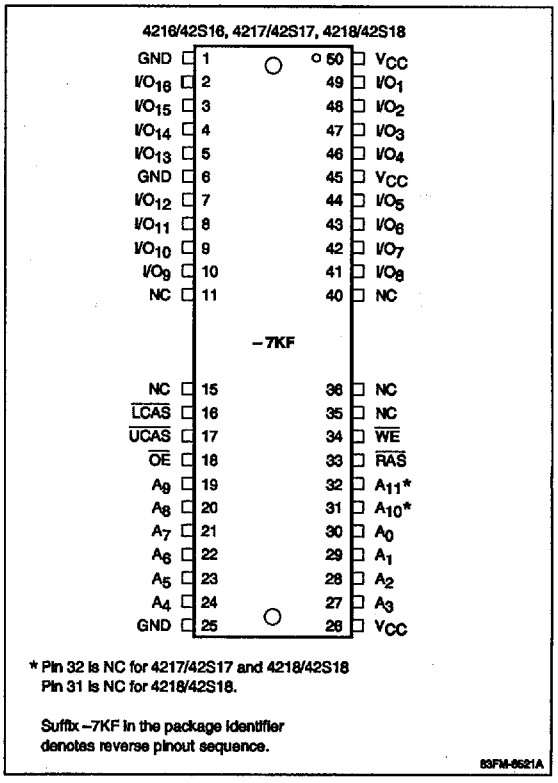
### 50/44-Pin Plastic TSOP (Reverse Pinouts)

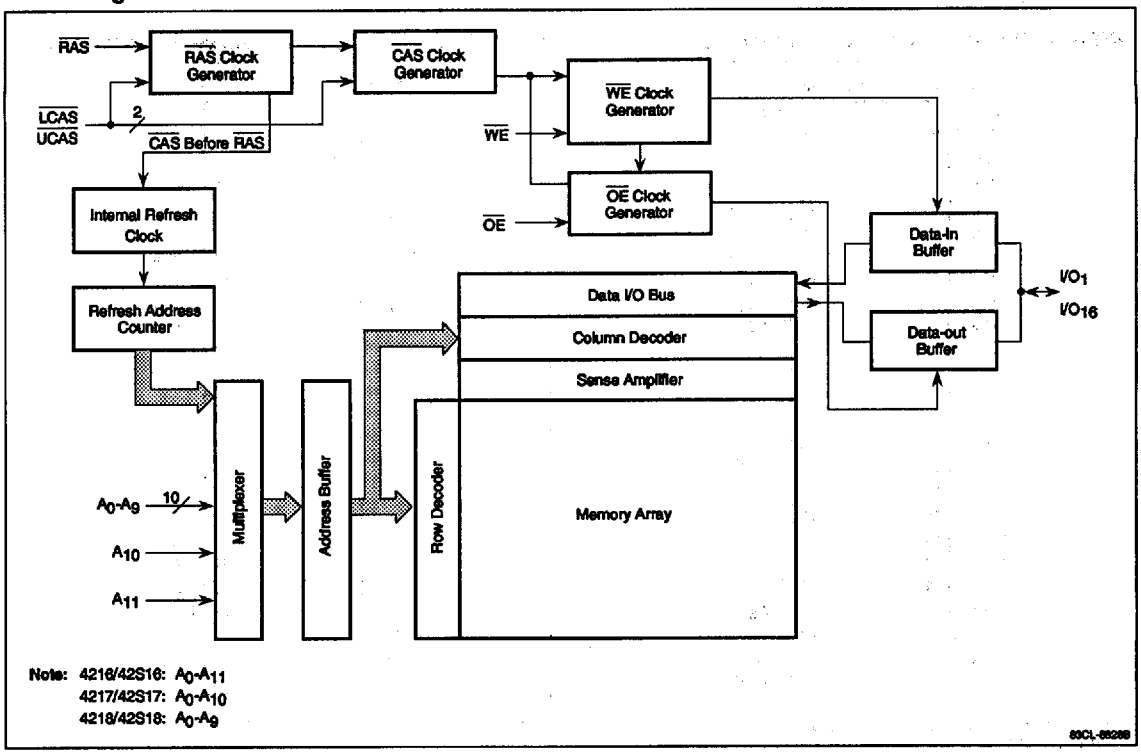



* Pin 32 is NC for 4217/42S17 and 4218/42S18
Pin 31 is NC for 4218/42S18.

Suffix –7KF in the package identifier denotes reverse pinout sequence.

83FM-8521A

## Block Diagram




Note: 4216/42S16: $A_0$-$A_{11}$
4217/42S17: $A_0$-$A_{10}$
4218/42S18: $A_0$-$A_9$

## Truth Table

| Function | RAS | LCAS | UCAS | WE | OE | $I/O_1$ - $I/O_8$ | $I/O_9$ - $I/O_{16}$ |
|---|---|---|---|---|---|---|---|
| Standby | H | X | X | X | X | High-Z | High-Z |
| Refresh cycle | L | H | H | X | X | High-Z | High-Z |
| Byte read cycle | L | L | H | H | L | Data output | High-Z |
| | L | H | L | H | L | High-Z | Data output |
| Word read cycle | L | L | L | H | L | Data output | Data output |
| Byte write cycle | L | L | H | L | H | Data input | — |
| | L | H | L | L | H | — | Data input |
| Word write cycle | L | L | L | L | H | Data input | Data input |
| —— | L | L | L | H | H | High-Z | High-Z |

X = don't care.

## Ordering Information, μPD4216160 (+5-volt power; 4096 refresh cycles)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD4216160LE-50 | 50 ns | 35 ns | 350 μA | 42-pin plastic SOJ |
| LE-60 | 60 ns | 40 ns | | |
| LE-70 | 70 ns | 45 ns | | |
| LE-80 | 80 ns | 50 ns | | |
| μPD4216160G5-50 | 50 ns | 35 ns | 350 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-60 | 60 ns | 40 ns | | |
| G5-70 | 70 ns | 45 ns | | |
| G5-80 | 80 ns | 50 ns | | |
| μPD4216160G5M-50 | 50 ns | 35 ns | 350 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-60 | 60 ns | 40 ns | | |
| G5M-70 | 70 ns | 45 ns | | |
| G5M-80 | 80 ns | 50 ns | | |

## Ordering Information, μPD4216160L (+3.3-volt power; 4096 refresh cycles)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD4216160LLE-A60 | 60 ns | 40 ns | 140 μA | 42-pin plastic SOJ |
| LE-A70 | 70 ns | 45 ns | | |
| LE-A80 | 80 ns | 50 ns | | |
| μPD4216160LG5-A60 | 60 ns | 40 ns | 140 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-A70 | 70 ns | 45 ns | | |
| G5-A80 | 80 ns | 50 ns | | |
| μPD4216160LG5M-A60 | 60 ns | 40 ns | 140 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-A70 | 70 ns | 45 ns | | |
| G5M-A80 | 80 ns | 50 ns | | |

## Ordering Information, μPD42S16160 (+ 5-volt power; 4096 refresh cycles; self-refresh mode)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD42S16160LE-50 | 50 ns | 35 ns | 350 μA | 42-pin plastic SOJ |
| LE-60 | 60 ns | 40 ns | | |
| LE-70 | 70 ns | 45 ns | | |
| LE-80 | 80 ns | 50 ns | | |
| μPD42S16160G5-50 | 50 ns | 35 ns | 350 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-60 | 60 ns | 40 ns | | |
| G5-70 | 70 ns | 45 ns | | |
| G5-80 | 80 ns | 50 ns | | |
| μPD42S16160G5M-50 | 50 ns | 35 ns | 350 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-60 | 60 ns | 40 ns | | |
| G5M-70 | 70 ns | 45 ns | | |
| G5M-80 | 80 ns | 50 ns | | |

## Ordering Information, μPD42S16160L (+ 3.3-volt power; 4096 refresh cycles; self-refresh mode)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD42S16160LLE-A60 | 60 ns | 40 ns | 140 μA | 42-pin plastic SOJ |
| LE-A70 | 70 ns | 45 ns | | |
| LE-A80 | 80 ns | 50 ns | | |
| μPD42S16160LG5-A60 | 60 ns | 40 ns | 140 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-A70 | 70 ns | 45 ns | | |
| G5-A80 | 80 ns | 50 ns | | |
| μPD42S16160LG5M-A60 | 60 ns | 40 ns | 140 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-A70 | 70 ns | 45 ns | | |
| G5M-A80 | 80 ns | 50 ns | | |

## Ordering Information, μPD4217160 (+ 5-volt power; 2048 refresh cycles)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD4217160LE-50 | 50 ns | 35 ns | 300 μA | 42-pin plastic SOJ |
| LE-60 | 60 ns | 40 ns | | |
| LE-70 | 70 ns | 45 ns | | |
| LE-80 | 80 ns | 50 ns | | |
| μPD4217160G5-50 | 50 ns | 35 ns | 300 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-60 | 60 ns | 40 ns | | |
| G5-70 | 70 ns | 45 ns | | |
| G5-80 | 80 ns | 50 ns | | |
| μPD4217160G5M-50 | 50 ns | 35 ns | 300 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-60 | 60 ns | 40 ns | | |
| G5M-70 | 70 ns | 45 ns | | |
| G5M-80 | 80 ns | 50 ns | | |

## Ordering Information, μPD4217160L (+ 3.3-volt power; 2048 refresh cycles)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD4217160LLE-A60 | 60 ns | 40 ns | 120 μA | 42-pin plastic SOJ |
| LE-A70 | 70 ns | 45 ns | | |
| LE-A80 | 80 ns | 50 ns | | |
| μPD4217160LG5-A60 | 60 ns | 40 ns | 120 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-A70 | 70 ns | 45 ns | | |
| G5-A80 | 80 ns | 50 ns | | |
| μPD4217160LG5M-A60 | 60 ns | 40 ns | 120 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-A70 | 70 ns | 45 ns | | |
| G5M-A80 | 80 ns | 50 ns | | |

## Ordering Information, μPD42S17160 (+5-volt power; 2048 refresh cycles; self-refresh mode)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD42S17160LE-50 | 50 ns | 35 ns | 300 μA | 42-pin plastic SOJ |
| LE-60 | 60 ns | 40 ns | | |
| LE-70 | 70 ns | 45 ns | | |
| LE-80 | 80 ns | 50 ns | | |
| μPD42S17160G5-50 | 50 ns | 35 ns | 300 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-60 | 60 ns | 40 ns | | |
| G5-70 | 70 ns | 45 ns | | |
| G5-80 | 80 ns | 50 ns | | |
| μPD42S17160G5M-50 | 50 ns | 35 ns | 300 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-60 | 60 ns | 40 ns | | |
| G5M-70 | 70 ns | 45 ns | | |
| G5M-80 | 80 ns | 50 ns | | |

## Ordering Information, μPD42S17160L (+3.3-volt power; 2048 refresh cycles; self-refresh mode)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD42S17160LLE-A60 | 60 ns | 40 ns | 120 μA | 42-pin plastic SOJ |
| LE-A70 | 70 ns | 45 ns | | |
| LE-A80 | 80 ns | 50 ns | | |
| μPD42S17160LG5-A60 | 60 ns | 40 ns | 120 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-A70 | 70 ns | 45 ns | | |
| G5-A80 | 80 ns | 50 ns | | |
| μPD42S17160LG5M-A60 | 60 ns | 40 ns | 120 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-A70 | 70 ns | 45 ns | | |
| G5M-A80 | 80 ns | 50 ns | | |

## Ordering Information, μPD4218160 (+ 5-volt power; 1024 refresh cycles)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD4218160LE-50 | 50 ns | 35 ns | 250 μA | 42-pin plastic SOJ |
| LE-60 | 60 ns | 40 ns | | |
| LE-70 | 70 ns | 45 ns | | |
| LE-80 | 80 ns | 50 ns | | |
| μPD4218160G5-50 | 50 ns | 35 ns | 250 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-60 | 60 ns | 40 ns | | |
| G5-70 | 70 ns | 45 ns | | |
| G5-80 | 80 ns | 50 ns | | |
| μPD4218160G5M-50 | 50 ns | 35 ns | 250 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-60 | 60 ns | 40 ns | | |
| G5M-70 | 70 ns | 45 ns | | |
| G5M-80 | 80 ns | 50 ns | | |

## Ordering Information, μPD4218160L (+ 3.3-volt power; 1024 refresh cycles)

| Part Number | RAS Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD4218160LLE-A60 | 60 ns | 40 ns | 110 μA | 42-pin plastic SOJ |
| LE-A70 | 70 ns | 45 ns | | |
| LE-A80 | 80 ns | 50 ns | | |
| μPD4218160LG5-A60 | 60 ns | 40 ns | 110 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-A70 | 70 ns | 45 ns | | |
| G5-A80 | 80 ns | 50 ns | | |
| μPD4218160LG5M-A60 | 60 ns | 40 ns | 110 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-A70 | 70 ns | 45 ns | | |
| G5M-A80 | 80 ns | 50 ns | | |

## Ordering Information, μPD42S18160 (+ 5-volt power; 1024 refresh cycles; self-refresh mode)

| Part Number | $\overline{RAS}$ Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD42S18160LE-50 | 50 ns | 35 ns | 250 μA | 42-pin plastic SOJ |
| LE-60 | 60 ns | 40 ns | | |
| LE-70 | 70 ns | 45 ns | | |
| LE-80 | 80 ns | 50 ns | | |
| μPD42S18160G5-50 | 50 ns | 35 ns | 250 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-60 | 60 ns | 40 ns | | |
| G5-70 | 70 ns | 45 ns | | |
| G5-80 | 80 ns | 50 ns | | |
| μPD42S18160G5M-50 | 50 ns | 35 ns | 250 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-60 | 60 ns | 40 ns | | |
| G5M-70 | 70 ns | 45 ns | | |
| G5M-80 | 80 ns | 50 ns | | |

## Ordering Information, μPD42S18160L (+ 3.3-volt power; 1024 refresh cycles; self-refresh mode)

| Part Number | $\overline{RAS}$ Access Time (max) | Fast-Page Cycle (max) | Battery Backup Current (max) | Package |
|---|---|---|---|---|
| μPD42S18160LLE-A60 | 60 ns | 40 ns | 110 μA | 42-pin plastic SOJ |
| LE-A70 | 70 ns | 45 ns | | |
| LE-A80 | 80 ns | 50 ns | | |
| μPD42S18160LG5-A60 | 60 ns | 40 ns | 110 μA | 50/44-pin plastic TSOP (normal pinouts) |
| G5-A70 | 70 ns | 45 ns | | |
| G5-A80 | 80 ns | 50 ns | | |
| μPD42S18160LG5M-A60 | 60 ns | 40 ns | 110 μA | 50/44-pin plastic TSOP (reverse pinouts) |
| G5M-A70 | 70 ns | 45 ns | | |
| G5M-A80 | 80 ns | 50 ns | | |

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage on any pin relative to GND | |
| 5-volt devices | −1.0 to +7.0 V |
| 3.3-volt devices | −0.5 to + 4.6 V |
| Operating temperature, $T_{OPR}$ | 0 to +70°C |
| Storage temperature, $T_{STG}$ | −55 to +125°C |
| Short-circuit output current, $I_{OS}$ | 50 mA |
| Power dissipation, $P_D$ | 1.0 W |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

## Capacitance

$T_A$ = 25°C; f = 1 MHz

| Parameter | Symbol | Max | Unit | Pins Under Test |
|---|---|---|---|---|
| Input capacitance | $C_{I1}$ | 5 | pF | Addresses |
| | $C_{I2}$ | 7 | pF | $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$, $\overline{RAS}$ |
| Input/output capacitance | $C_O$ | 7 | pF | $I/O_1$ - $I/O_{16}$ |

## Recommended Operating Conditions

| | | 5-Volt Devices | | | 3.3-Volt Devices | | | |
|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |
| Input voltage, high | $V_{IH}$ | 2.4 | | $V_{CC}$ + 1.0 | 2.0 | | $V_{CC}$ + 0.3 | V |
| Input voltage, low | $V_{IL}$ | −1.0 | | 0.8 | −0.3 | | 0.8 | V |
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | 3.0 | 3.3 | 3.6 | V |
| Ambient temperature | $T_A$ | 0 | | 70 | 0 | | 70 | °C |

## Self-Refresh Current; 42S1x Devices

$T_A$ = 0 to +70°C; $V_{CC}$ = +5 V ±10% or +3.3 V ±0.3 V

| Symbol | 5-Volt Devices | 3.3-Volt Devices | Conditions |
|---|---|---|---|
| $I_{CC7}$ | 200 μA max | 80 μA max | I/O pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open. Other input pins: $V_{IH} \geq V_{CC}$ −0.2 V; $V_{IL} \leq$ 0.2 V or open; $t_{RAS} \geq$ 100 μs |

## DC Characteristics; 5-Volt Devices

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Standby current | $I_{CC2}$ | | | 2.0 | mA | $\overline{RAS}$ = $\overline{CAS} \geq V_{IH}$ (min); $I_O$ = 0 mA |
| | | | | 400 | μA | $\overline{RAS}$ = $\overline{CAS} \geq V_{CC}$ − 0.2 V; $I_O$ = 0 mA |
| Input leakage current | $I_{I(L)}$ | −10 | | 10 | μA | $V_{IN}$ = 0 V to $V_{CC}$; all other pins not under test = 0 V |
| Output leakage current | $I_{O(L)}$ | −10 | | 10 | μA | $D_{OUT}$ disabled; $V_{OUT}$ = 0 V to $V_{CC}$ |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 4.2 mA |
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −5 mA |

## DC Characteristics; 3.3-Volt Devices

$T_A$ = 0 to +70°C; $V_{CC}$ = +3.3 V ±0.3 V

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Standby current | $I_{CC2}$ | | | 2.0 | mA | $\overline{RAS}$ = $\overline{CAS}$ ≥ $V_{IH}$ (min); $I_O$ = 0 mA |
| | | | | 400 | μA | $\overline{RAS}$ = $\overline{CAS}$ ≥ $V_{CC}$ – 0.2 V; $I_O$ = 0 mA |
| Input leakage current | $I_{I(L)}$ | –10 | | 10 | μA | $V_{IN}$ = 0 V to $V_{CC}$; all other pins not under test = 0 V |
| Output leakage current | $I_{O(L)}$ | –10 | | 10 | μA | $D_{OUT}$ disabled; $V_{OUT}$ = 0 V to $V_{CC}$ |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = –2.0 mA |

## DC Current Requirements; 5-Volt Devices

| Parameter | Symbol | -50 | -60 | -70 | -80 | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Operating current | $I_{CC1}$ | | | | | | |
| 4216/42S16 | | 110 | 100 | 90 | 80 | mA | $\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC}$ = $t_{RC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 130 | 120 | 110 | 100 | mA | |
| 4218/42S18 | | 170 | 160 | 150 | 140 | mA | |
| Refresh current ($\overline{RAS}$ only refresh) | $I_{CC3}$ | | | | | | |
| 4216/42S16 | | 110 | 100 | 90 | 80 | mA | $\overline{RAS}$ cycling; $\overline{CAS}$ ≥ $V_{IH}$ (min); $t_{RC}$ = $t_{RC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 130 | 120 | 110 | 100 | mA | |
| 4218/42S18 | | 170 | 160 | 150 | 140 | mA | |
| Operating current (Fast-page mode) | $I_{CC4}$ | | | | | | |
| 4216/42S16 | | 100 | 90 | 80 | 70 | mA | $\overline{CAS}$ cycling; $\overline{RAS}$ ≤ $V_{IL}$ (max); $t_{PC}$ = $t_{PC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 100 | 90 | 80 | 70 | mA | |
| 4218/42S18 | | 100 | 90 | 80 | 70 | mA | |
| Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh) | $I_{CC5}$ | | | | | | |
| 4216/42S16 | | 110 | 100 | 90 | 80 | mA | $\overline{RAS}$ cycling; $t_{RC}$ = $t_{RC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 130 | 120 | 110 | 100 | mA | |
| 4218/42S18 | | 170 | 160 | 150 | 140 | mA | |
| Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh) | $I_{CC6}$ | $t_{RAS}$ ≤ 300 ns | | $t_{RAS}$ ≤ 1 μs | | | Standby: $\overline{RAS}$ ≥ $V_{CC}$ – 0.2 V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ $V_{IL}$ ≤ 0.2 V, $V_{CC}$ – 0.2 V ≤ $V_{IH}$ ≤ $V_{IH}$ (max); $\overline{WE}$, $\overline{OE}$: $V_{IH}$; Address: don't care; Output: open |
| 42S16 | | 350 | | 500 | | μA | $\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms |
| 42S17 | | 300 | | 400 | | μA | $\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms |
| 42S18 | | 250 | | 300 | | μA | $\overline{CAS}$ before $\overline{RAS}$ refresh: 1024 cycles, 256 ms |

## DC Current Requirements; 3.3-Volt Devices

| Parameter | Symbol | -A60 | -A70 | -A80 | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Operating current | $I_{CC1}$ | | | | | |
| 4216/42S16 | | 90 | 80 | 70 | mA | $\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 110 | 100 | 90 | mA | |
| 4218/42S18 | | 150 | 140 | 130 | mA | |
| Refresh current ($\overline{RAS}$ only refresh) | $I_{CC3}$ | | | | | |
| 4216/42S16 | | 90 | 80 | 70 | mA | $\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ (min); $t_{RC} = t_{RC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 110 | 100 | 90 | mA | |
| 4218/42S18 | | 150 | 140 | 130 | mA | |
| Operating current (Fast-page mode) | $I_{CC4}$ | | | | | |
| 4216/42S16 | | 80 | 70 | 60 | mA | $\overline{CAS}$ cycling; $\overline{RAS} \leq V_{IL}$ (max); $t_{PC} = t_{PC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 80 | 70 | 60 | mA | |
| 4218/42S18 | | 80 | 70 | 60 | mA | |
| Refresh current ($\overline{CAS}$ before $\overline{RAS}$ refresh) | $I_{CC5}$ | | | | | |
| 4216/42S16 | | 90 | 80 | 70 | mA | $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); $I_O$ = 0 mA |
| 4217/42S17 | | 110 | 100 | 90 | mA | |
| 4218/42S18 | | 150 | 140 | 130 | mA | |
| Battery backup current (Standby with $\overline{CAS}$ before $\overline{RAS}$ refresh) | $I_{CC6}$ | $t_{RAS} \leq 300$ ns | | $t_{RAS} \leq 1$ μs | | Standby: $\overline{RAS} \geq V_{CC} - 0.2$ V; $\overline{RAS}$, $\overline{CAS}$: 0 V ≤ $V_{IL}$ ≤ 0.2 V, $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH}$ (max); $\overline{WE}$, $\overline{OE}$: $V_{IH}$; Address: don't care; Output: open |
| 42S16 | | 140 | | 140 | μA | $\overline{CAS}$ before $\overline{RAS}$ refresh: 4096 cycles, 256 ms |
| 42S17 | | 120 | | 120 | μA | $\overline{CAS}$ before $\overline{RAS}$ refresh: 2048 cycles, 256 ms |
| 42S18 | | 110 | | 110 | μA | $\overline{CAS}$ before $\overline{RAS}$ refresh: 1024 cycles, 256 ms |

## AC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10% (-50, -60, -70, -80) or +3.3 V ±0.3 V (-A60, -A70, -A80)

| | | -50 | | -60, -A60 | | -70, -A70 | | -80, -A80 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Test Conditions** |
| Access time from column address | $t_{AA}$ | | 25 | | 30 | | 35 | | 40 | ns | (Notes 7, 8) |
| Access time from $\overline{CAS}$ precharge (rising edge) | $t_{ACP}$ | | 30 | | 35 | | 40 | | 45 | ns | (Note 7) |
| Column address setup time | $t_{ASC}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Row address setup time | $t_{ASR}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 45 | | 53 | | 60 | | 65 | | ns | (Note 15) |
| Access time from $\overline{CAS}$ (falling edge) | $t_{CAC}$ | | 13 | | 15 | | 18 | | 20 | ns | (Notes 7, 8) |
| Column address hold time | $t_{CAH}$ | 13 | | 15 | | 15 | | 15 | | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 13 | 10,000 | 15 | 10,000 | 18 | 10,000 | 20 | 10,000 | ns | |
| $\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle | $t_{CHR}$ | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{CAS}$ hold time (CBR self-refresh mode) | $t_{CHS}$ | −50 | | −50 | | −50 | | −50 | | ns | (Note 16) |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | 0 | | 0 | | 0 | | 0 | | ns | (Note 7) |
| Fast-page $\overline{CAS}$ precharge time | $t_{CP}$ | 8 | | 10 | | 10 | | 10 | | ns | |
| $\overline{CAS}$ precharge time | $t_{CPN}$ | 8 | | 10 | | 10 | | 10 | | ns | |
| Fast-page $\overline{CAS}$ precharge to $\overline{WE}$ delay time | $t_{CPWD}$ | 55 | | 60 | | 65 | | 70 | | ns | (Note 14) |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | | 5 | | 5 | | 5 | | ns | (Note 10) |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 50 | | 60 | | 70 | | 80 | | ns | |
| $\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle | $t_{CSR}$ | 5 | | 5 | | 5 | | 5 | | ns | |
| $\overline{CAS}$ to $\overline{WE}$ delay | $t_{CWD}$ | 33 | | 38 | | 43 | | 45 | | ns | (Note 15) |
| Write command referenced to $\overline{CAS}$ lead time | $t_{CWL}$ | 13 | | 15 | | 15 | | 15 | | ns | |
| Data-in hold time | $t_{DH}$ | 10 | | 10 | | 15 | | 15 | | ns | (Note 13) |
| Data-in setup time | $t_{DS}$ | 0 | | 0 | | 0 | | 0 | | ns | (Note 13) |
| Masked write hold time referenced to $\overline{RAS}$ | $t_{MRH}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Access time from $\overline{OE}$ | $t_{OEA}$ | | 13 | | 15 | | 18 | | 20 | ns | (Notes 3, 4, 7, 8) |
| $\overline{OE}$ data delay time | $t_{OED}$ | 10 | | 13 | | 15 | | 15 | | ns | |
| $\overline{OE}$ command hold time | $t_{OEH}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| $\overline{OE}$ to $\overline{RAS}$ inactive setup time | $t_{OES}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Output turnoff delay from $\overline{OE}$ | $t_{OEZ}$ | 0 | 10 | 0 | 13 | 0 | 15 | 0 | 15 | ns | (Note 9) |

## AC Characteristics (cont)

| Parameter | Symbol | -50 Min | -50 Max | -60, -A60 Min | -60, -A60 Max | -70, -A70 Min | -70, -A70 Max | -80, -A80 Min | -80, -A80 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Output disable from $\overline{CAS}$ high | $t_{OFF}$ | 0 | 10 | 0 | 13 | 0 | 15 | 0 | 15 | ns | (Note 9) |
| $\overline{OE}$ to output in low-Z | $t_{OLZ}$ | 0 | | 0 | | 0 | | 0 | | ns | (Note 7) |
| Fast-page read or write cycle time | $t_{PC}$ | 35 | | 40 | | 45 | | 50 | | ns | (Note 6) |
| Fast-page read-modify-write cycle time with extended data output | $t_{PRWC}$ | 80 | | 85 | | 90 | | 100 | | ns | (Note 6) |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | | 50 | | 60 | | 70 | | 80 | ns | (Notes 7, 8) |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 13 | 25 | 15 | 30 | 15 | 35 | 17 | 40 | ns | (Note 8) |
| Row address hold time | $t_{RAH}$ | 8 | | 10 | | 10 | | 12 | | ns | |
| Column address lead time referenced to $\overline{RAS}$ (rising edge) | $t_{RAL}$ | 25 | | 30 | | 35 | | 40 | | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 50 | 10,000 | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | ns | |
| Fast-page $\overline{RAS}$ pulse width | $t_{RASP}$ | 50 | 125,000 | 60 | 125,000 | 70 | 125,000 | 80 | 125,000 | ns | |
| $\overline{RAS}$ pulse width (CBR self-refresh mode) | $t_{RASS}$ | 100 | | 100 | | 100 | | 100 | | μs | (Note 16) |
| Random read or write cycle time | $t_{RC}$ | 90 | | 110 | | 130 | | 150 | | ns | (Note 6) |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 18 | 32 | 20 | 45 | 20 | 50 | 25 | 60 | ns | (Note 8) |
| Read command hold time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | | 0 | | 0 | | 0 | | ns | (Note 11) |
| Read command setup time | $t_{RCS}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Refresh period | $t_{REF}$ | | | | | | | | | | |
| 4216 | | | 64 | | 64 | | 64 | | 64 | ms | |
| 4217 | | | 32 | | 32 | | 32 | | 32 | ms | |
| 4218 | | | 16 | | 16 | | 16 | | 16 | ms | |
| 42S16 | | | 256 | | 256 | | 256 | | 256 | ms | |
| 42S17 | | | 256 | | 256 | | 256 | | 256 | ms | |
| 42S18 | | | 256 | | 256 | | 256 | | 256 | ms | |
| $\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge | $t_{RHCP}$ | 30 | | 35 | | 40 | | 45 | | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 30 | | 40 | | 50 | | 60 | | ns | |
| $\overline{RAS}$ precharge $\overline{CAS}$ hold time | $t_{RPC}$ | 5 | | 5 | | 5 | | 5 | | ns | |
| $\overline{RAS}$ precharge time (CBR self-refresh mode) | $t_{RPS}$ | 90 | | 110 | | 130 | | 150 | | ns | (Note 16) |
| Read command hold time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | | 0 | | 0 | | 0 | | ns | (Note 11) |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 13 | | 15 | | 18 | | 20 | | ns | |
| Read-modify-write cycle time | $t_{RWC}$ | 140 | | 160 | | 180 | | 200 | | ns | (Note 6) |

## AC Characteristics (cont)

| Parameter | Symbol | -50 Min | -50 Max | -60, -A60 Min | -60, -A60 Max | -70, -A70 Min | -70, -A70 Max | -80, -A80 Min | -80, -A80 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{RAS}$ to $\overline{WE}$ delay | $t_{RWD}$ | 70 | | 83 | | 95 | | 105 | | ns | (Note 15) |
| Write command referenced to $\overline{RAS}$ lead time | $t_{RWL}$ | 18 | | 20 | | 20 | | 20 | | ns | |
| Rise and fall transition time | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| Write command hold time | $t_{WCH}$ | 8 | | 10 | | 10 | | 15 | | ns | (Note 12) |
| Write command setup time | $t_{WCS}$ | 0 | | 0 | | 0 | | 0 | | ns | (Note 14) |
| Write command pulse width | $t_{WP}$ | 8 | | 10 | | 10 | | 15 | | ns | (Note 12) |

**Notes:**

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by eight refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is achieved.

(3) $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, and $I_{CC5}$ depend on output loading and cycle rates. Specified values are obtained with the output open. $I_{CC3}$ is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. $I_{CC4}$ is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(4) Ac measurements assume $t_T$ = 5 ns.

(5) $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring the timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A$ = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by $t_{RAC}$ (max).
If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by $t_{CAC}$ (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by $t_{AA}$ (max).

(9) $t_{OFF}$ (max) and $t_{OEZ}$ (max) define the time at which the outputs become open-circuit and are not referenced to $V_{OH}$ or $V_{OL}$.

(10) The $t_{CRP}$ requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.

(12) Parameter $t_{WP}$ is applicable for a late write cycle. For early write cycles, $t_{WCH}$ must be met.

(13) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in late write or read-modify-write cycles.

(14) If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle.

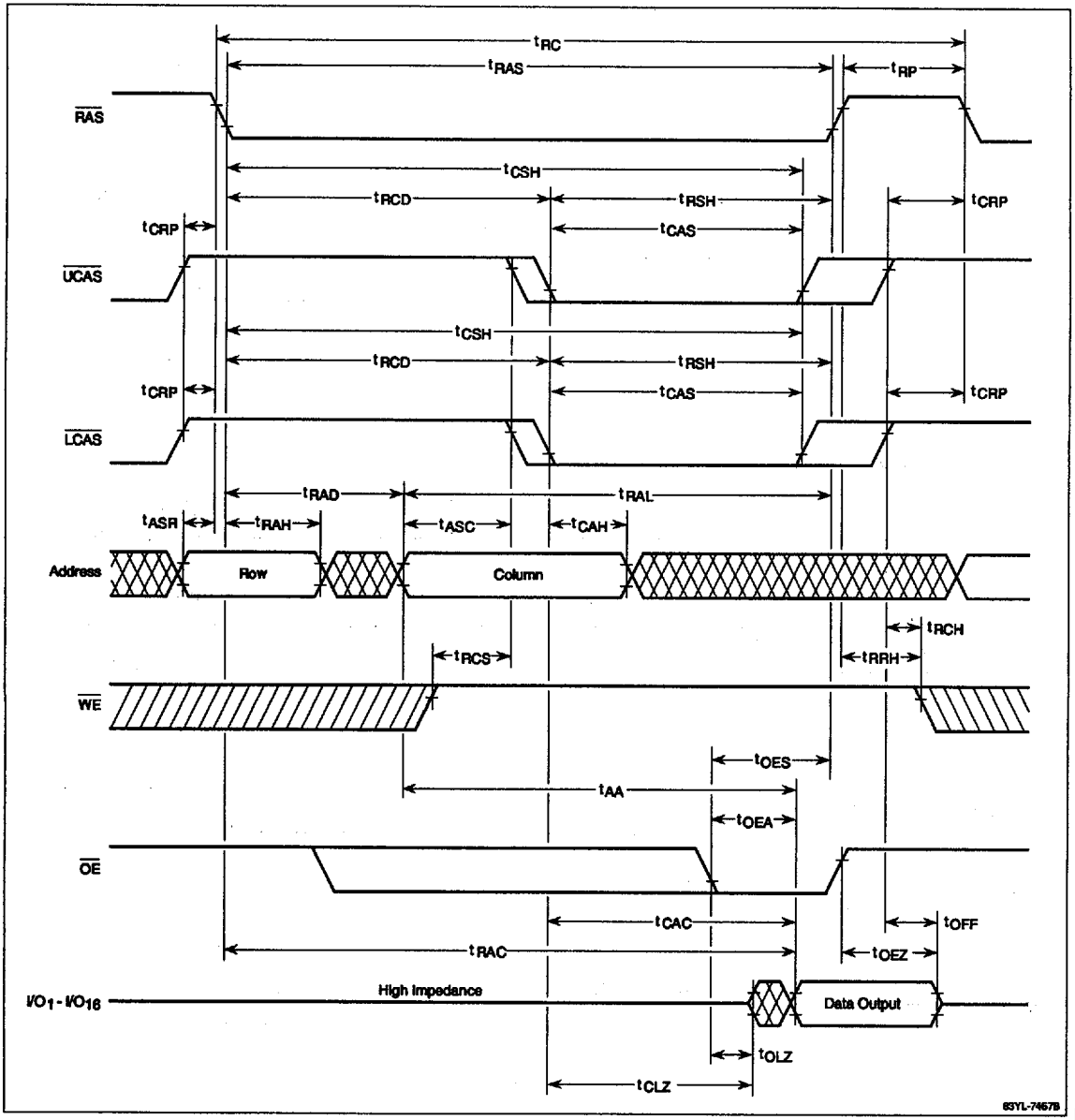
(15) If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to $V_{IH}$) is indeterminate.

(16) Parameter is applicable only to self-refresh versions.

(17) With burst CBR, $\overline{RAS}$ only, or external $\overline{RAS}$/$\overline{CAS}$, all addresses must be refreshed before entering self-refresh mode and after exiting.

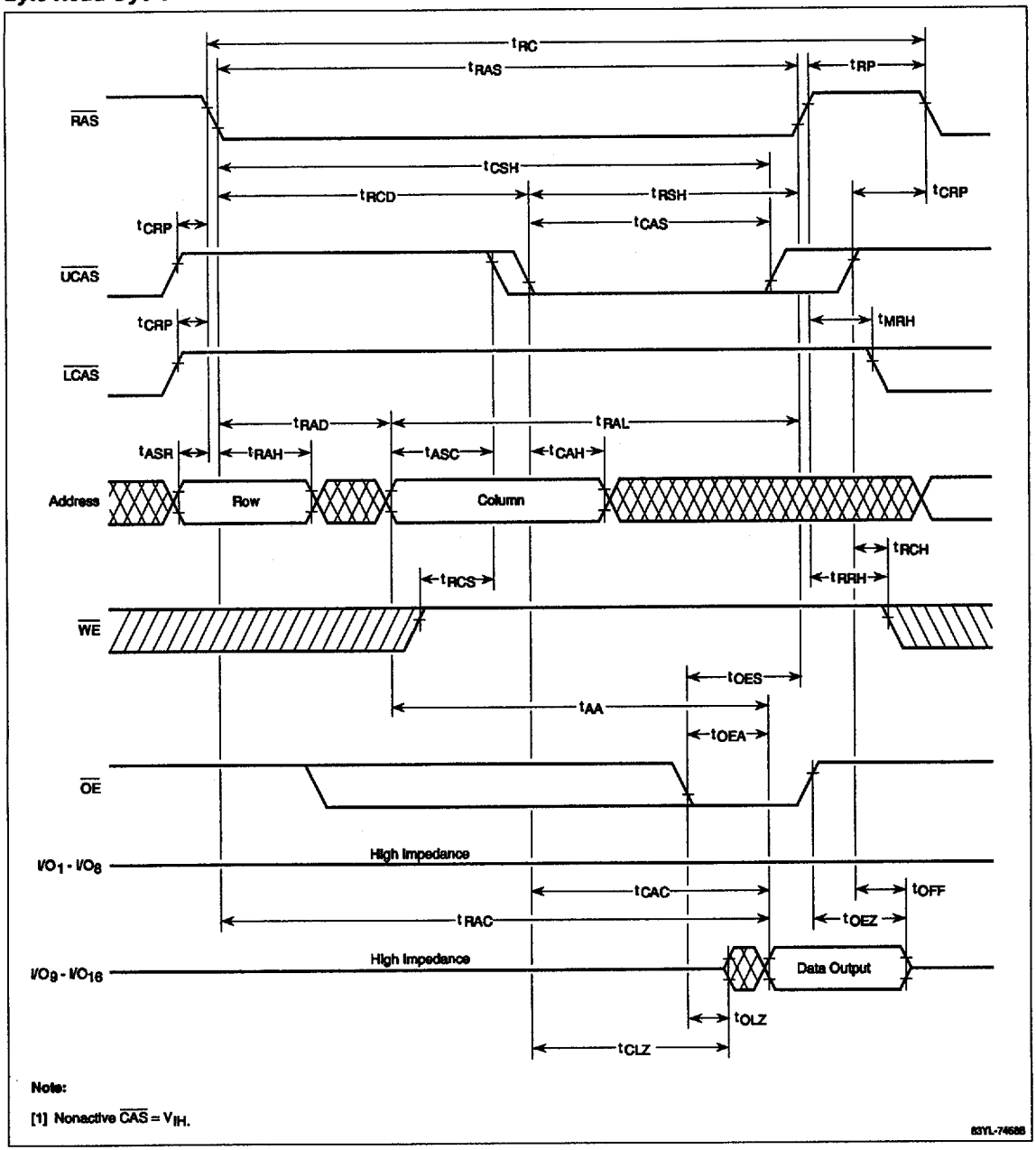
## Timing Waveforms

### *Word Read Cycle*



## Timing Waveforms (cont)

### *Byte Read Cycle*



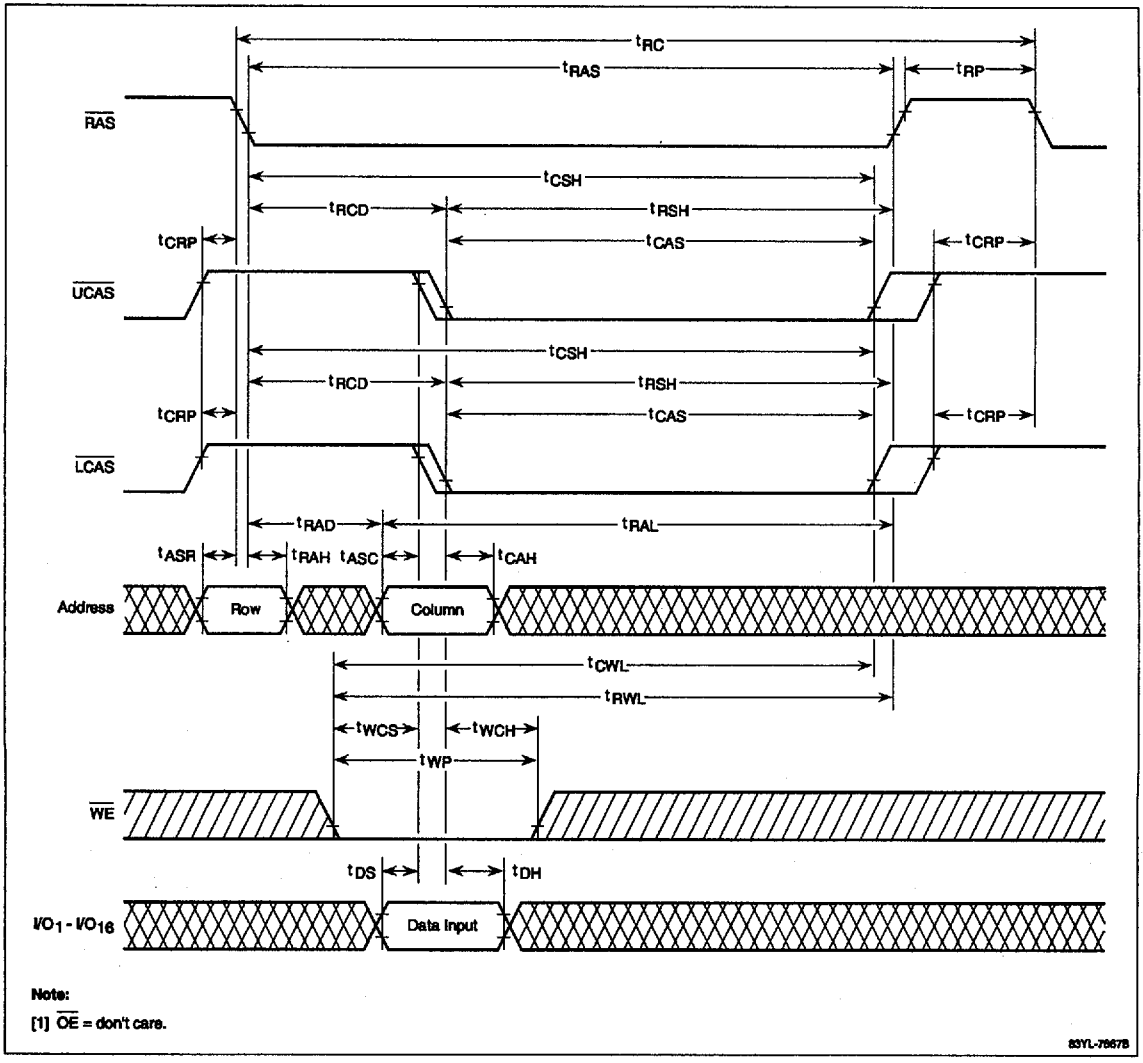

**Note:**

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-74688

## Timing Waveforms (cont)

***Word Early-Write Cycle***

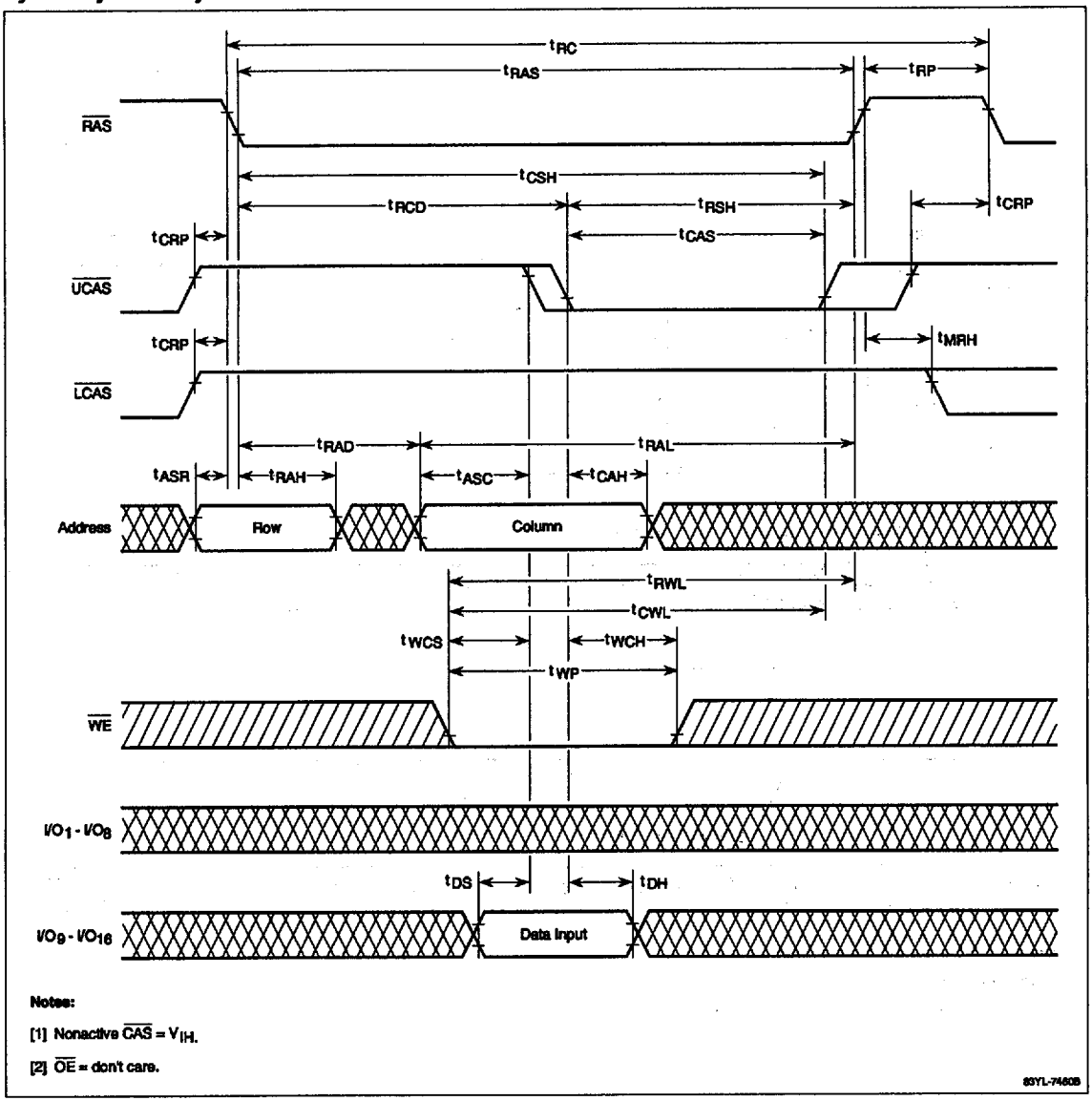



**Note:**
[1] $\overline{OE}$ = don't care.

83YL-7667B

## Timing Waveforms (cont)

### *Byte Early-Write Cycle*




**Notes:**

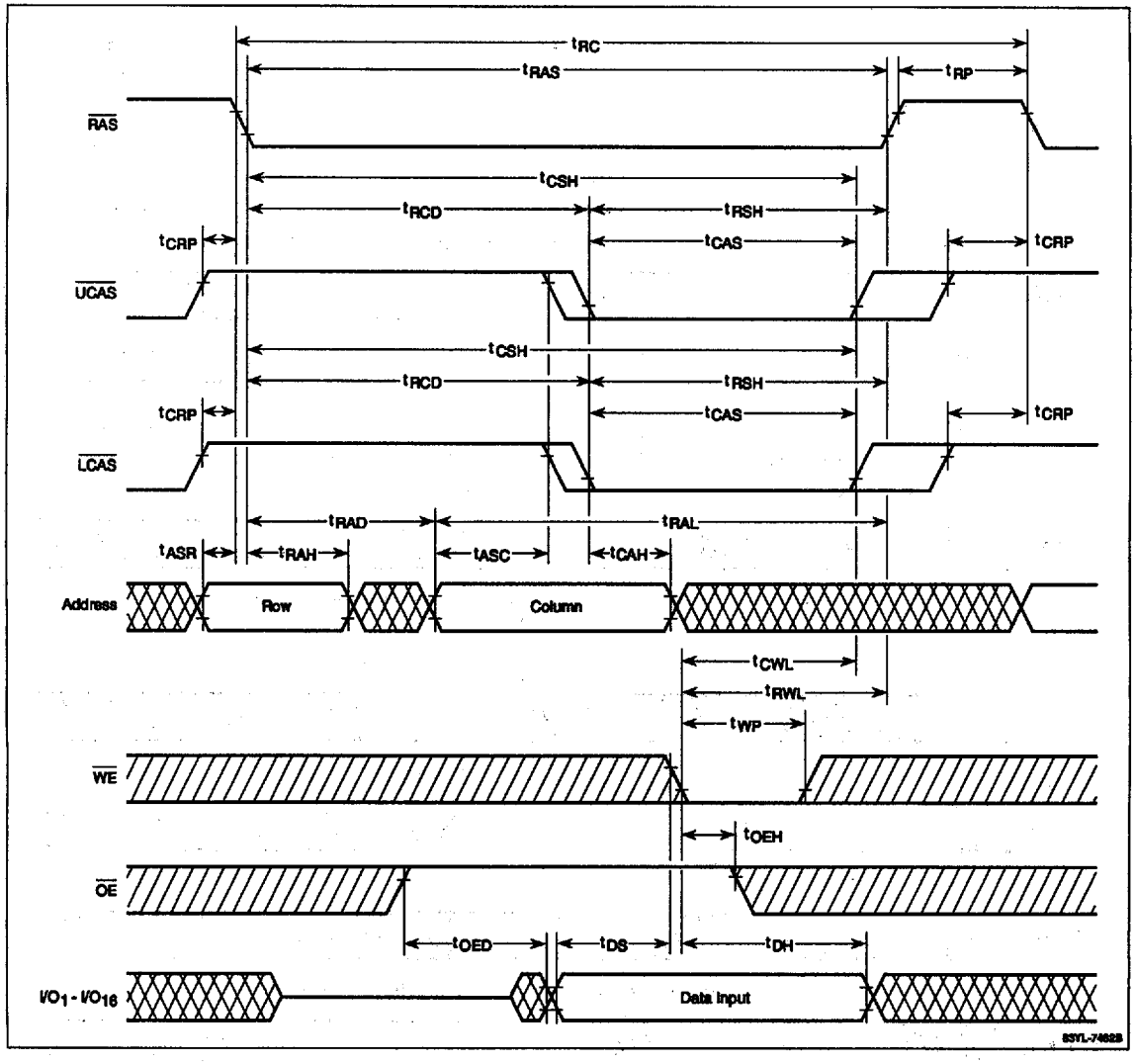
[1] Nonactive $\overline{CAS} = V_{IH}$.

[2] $\overline{OE}$ = don't care.

83YL-746OB

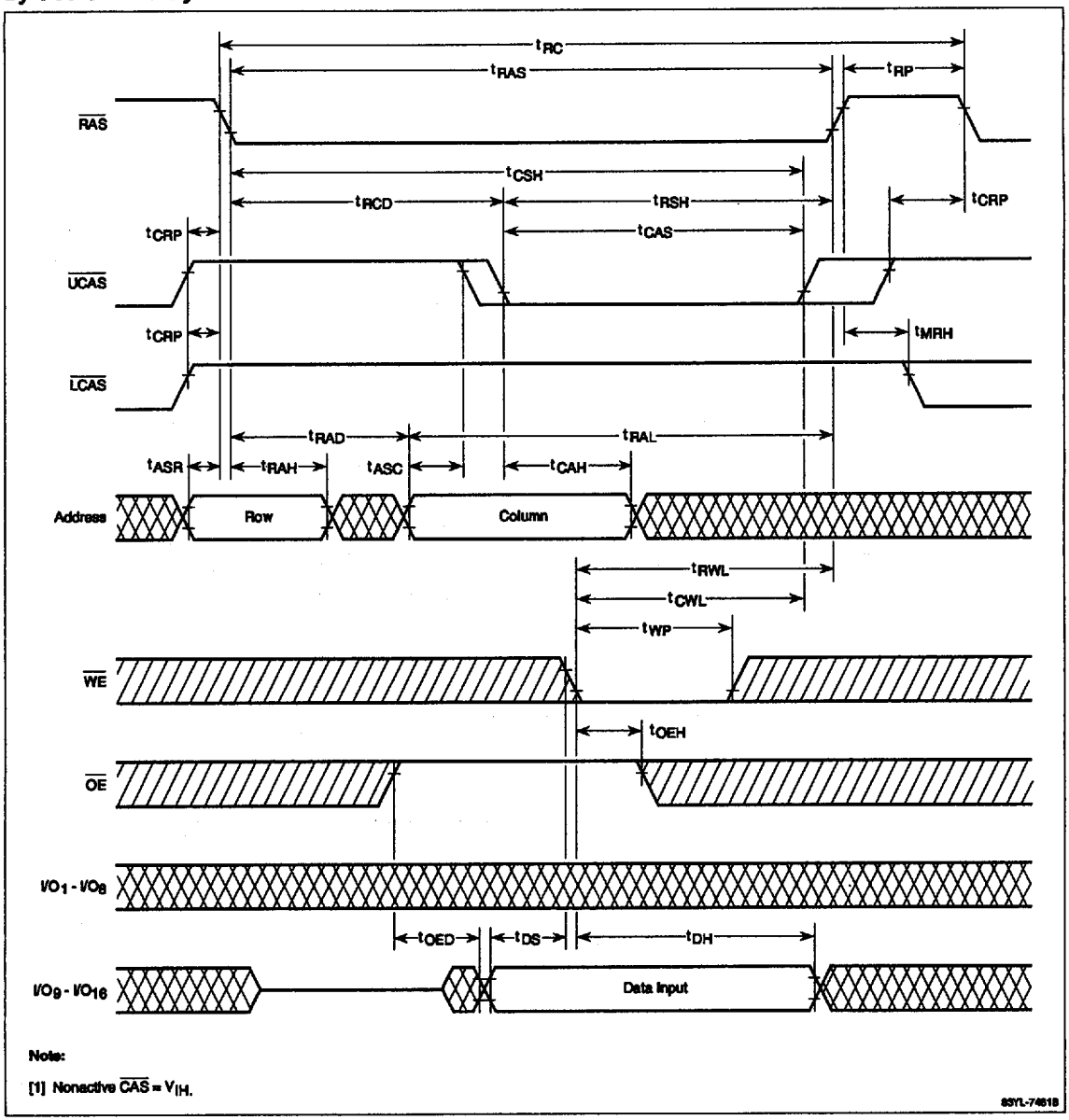
## Timing Waveforms (cont)

***Word Late-Write Cycle***



## Timing Waveforms (cont)

### *Byte Late-Write Cycle*



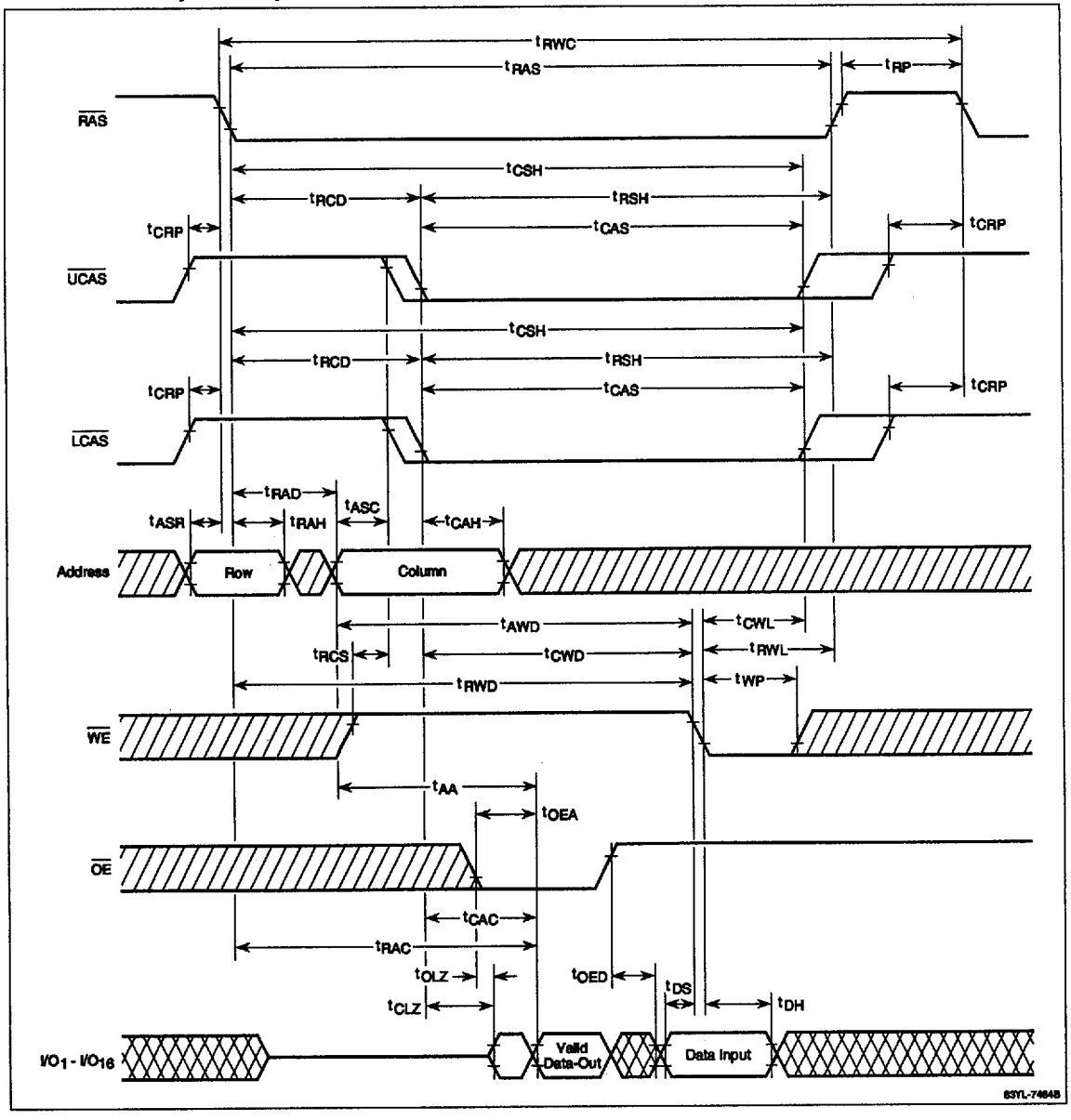

Note:

[1] Nonactive $\overline{CAS}$ = $V_{IH}$.

83YL-74818

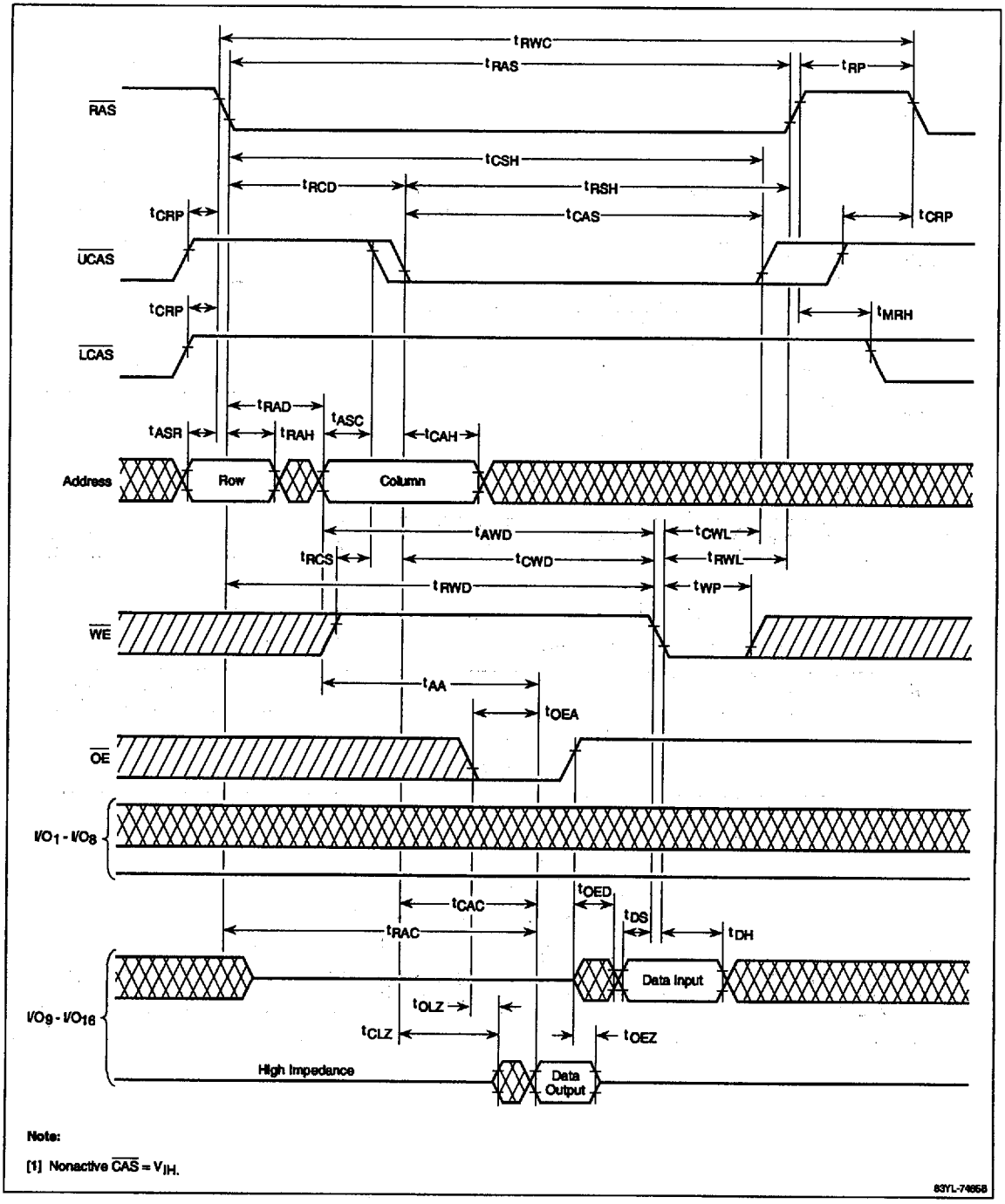
## Timing Waveforms (cont)

***Word Read-Modify-Write Cycle***



## Timing Waveforms (cont)

### *Byte Read-Modify-Write Cycle*



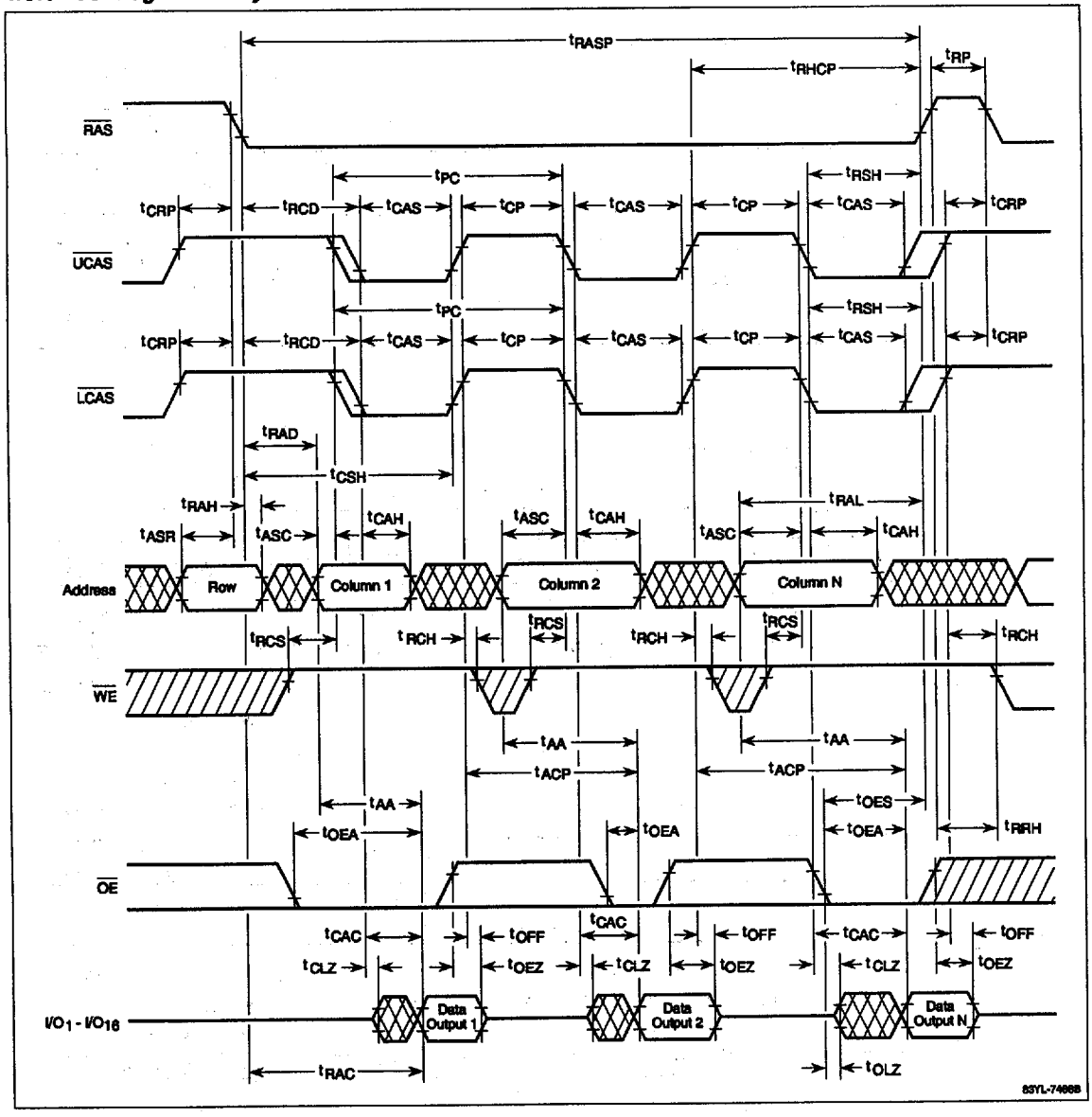

**Note:**

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-74658

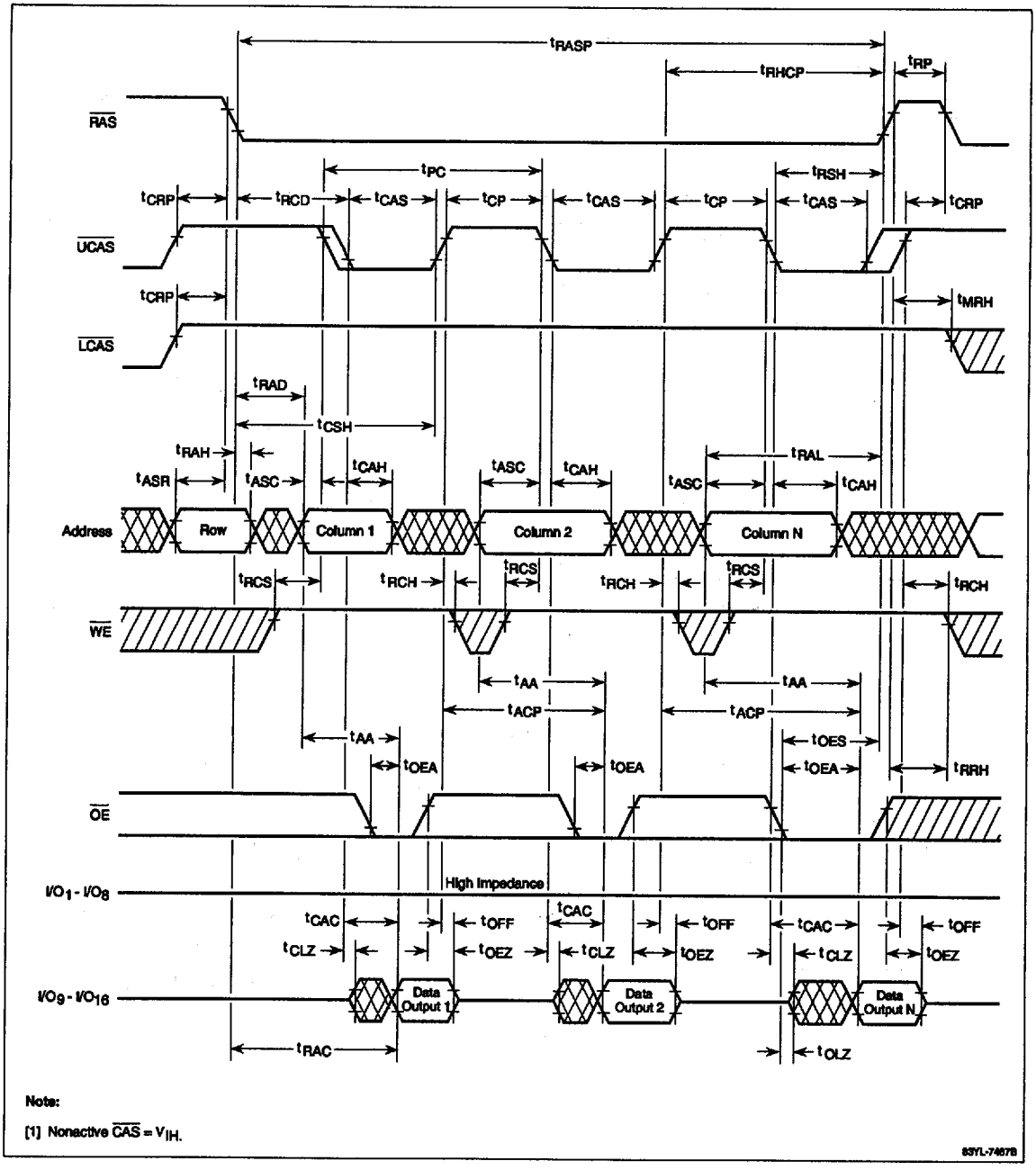
## Timing Waveforms (cont)

### *Word Fast-Page Read Cycle*



## Timing Waveforms (cont)

### *Byte Fast-Page Read Cycle*



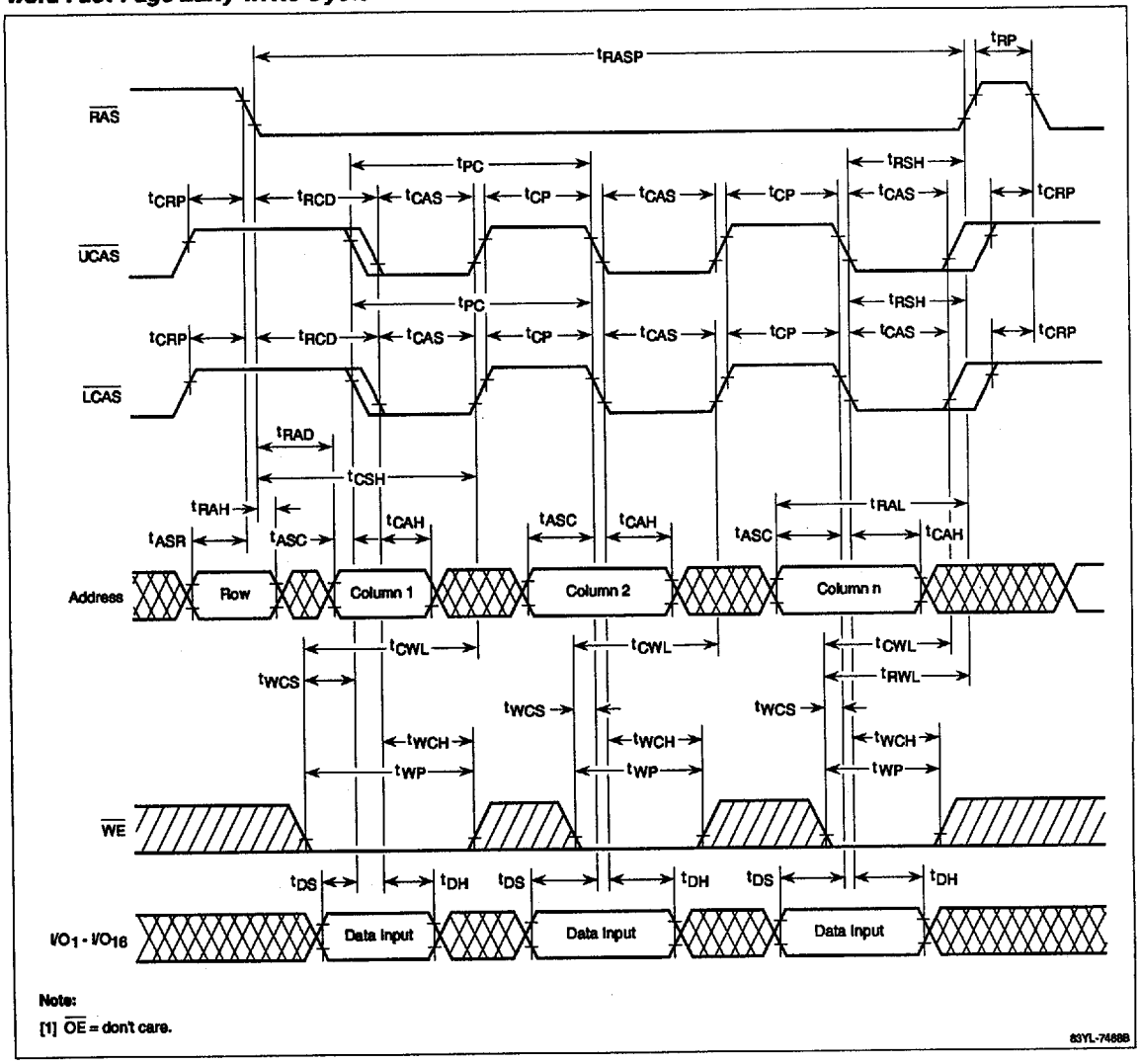

**Note:**

[1] Nonactive $\overline{CAS} = V_{IH}$.

83YL-7467B

## Timing Waveforms (cont)

### *Word Fast-Page Early-Write Cycle*



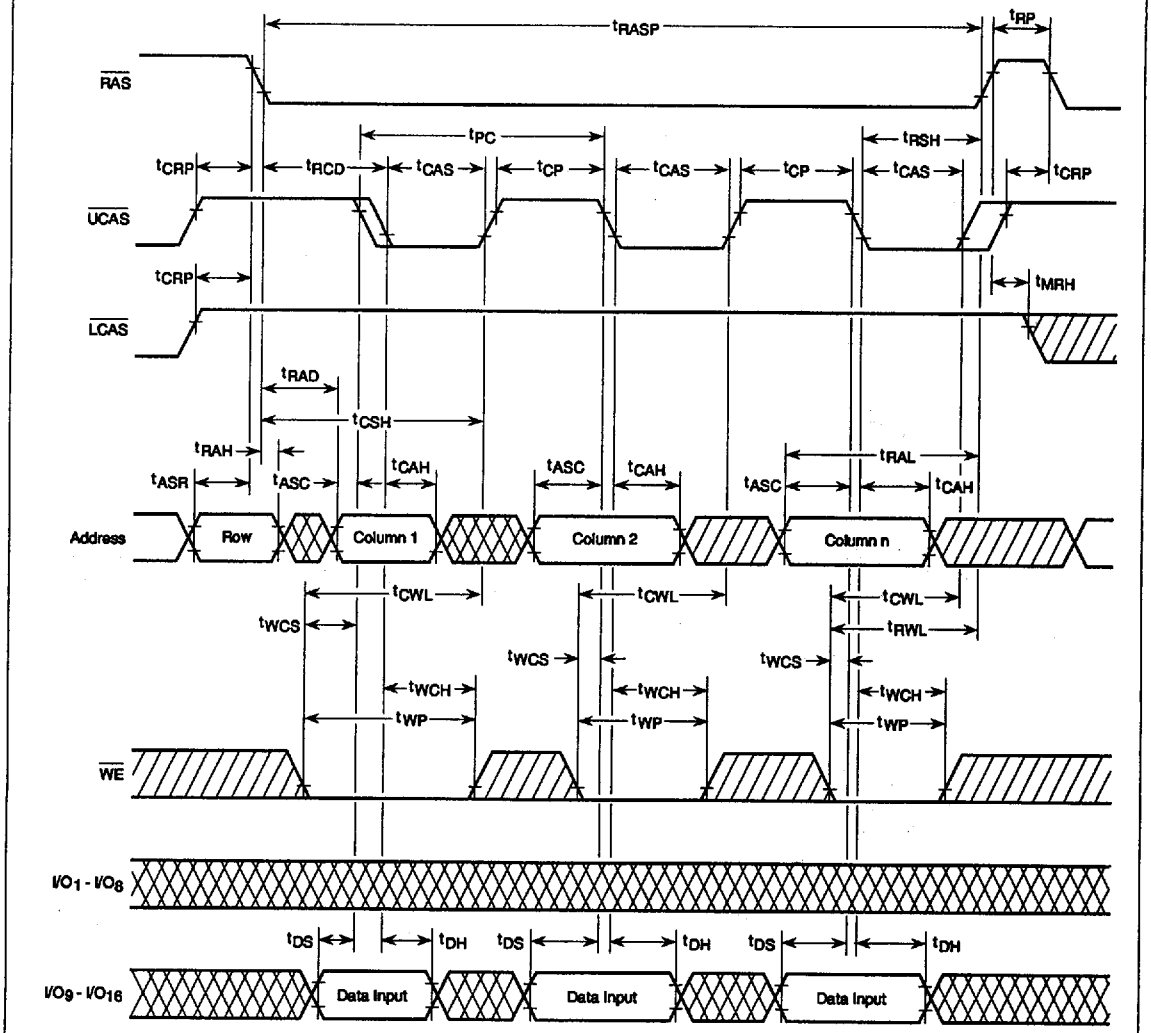

**Note:**

[1] $\overline{OE}$ = don't care.

83YL-74688

## Timing Waveforms (cont)

### *Byte Fast-Page Early-Write Cycle*




**Notes:**

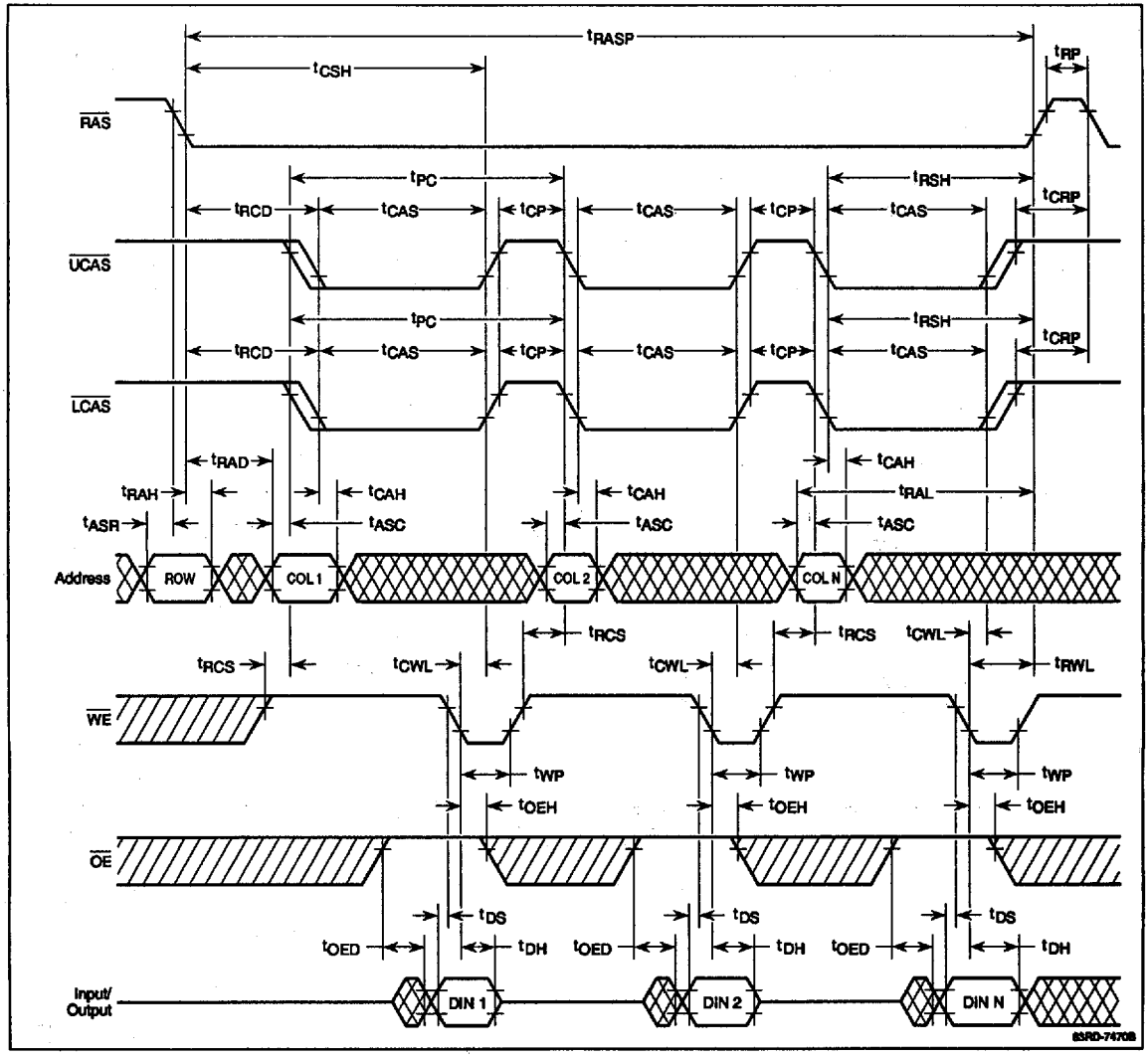
[1] Nonactive $\overline{CAS}$ = $V_{IH}$.

[2] $\overline{OE}$ = don't care.

83YL-74608

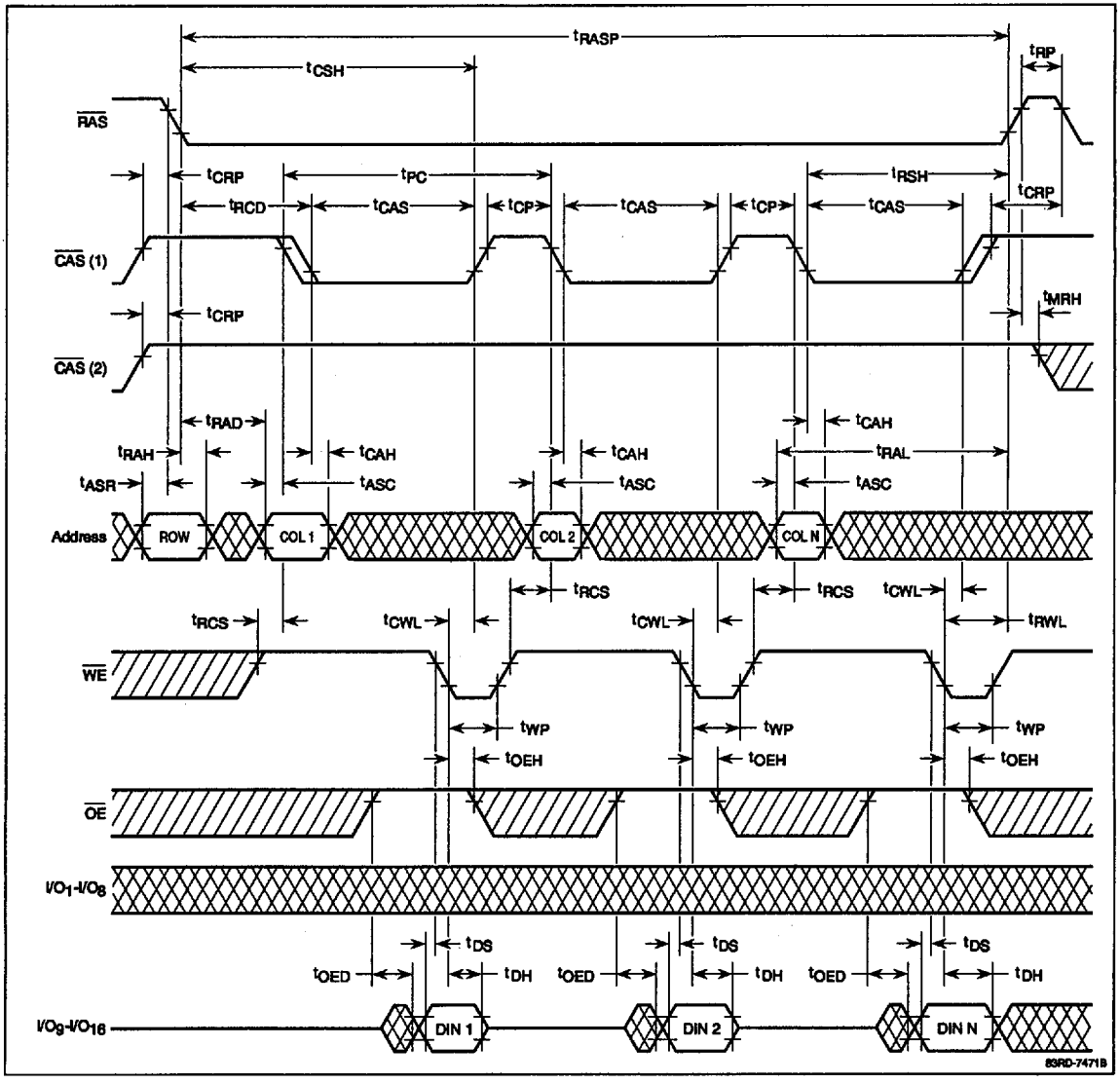
## Timing Waveforms (cont)

***Word Fast-Page Late-Write Cycle***



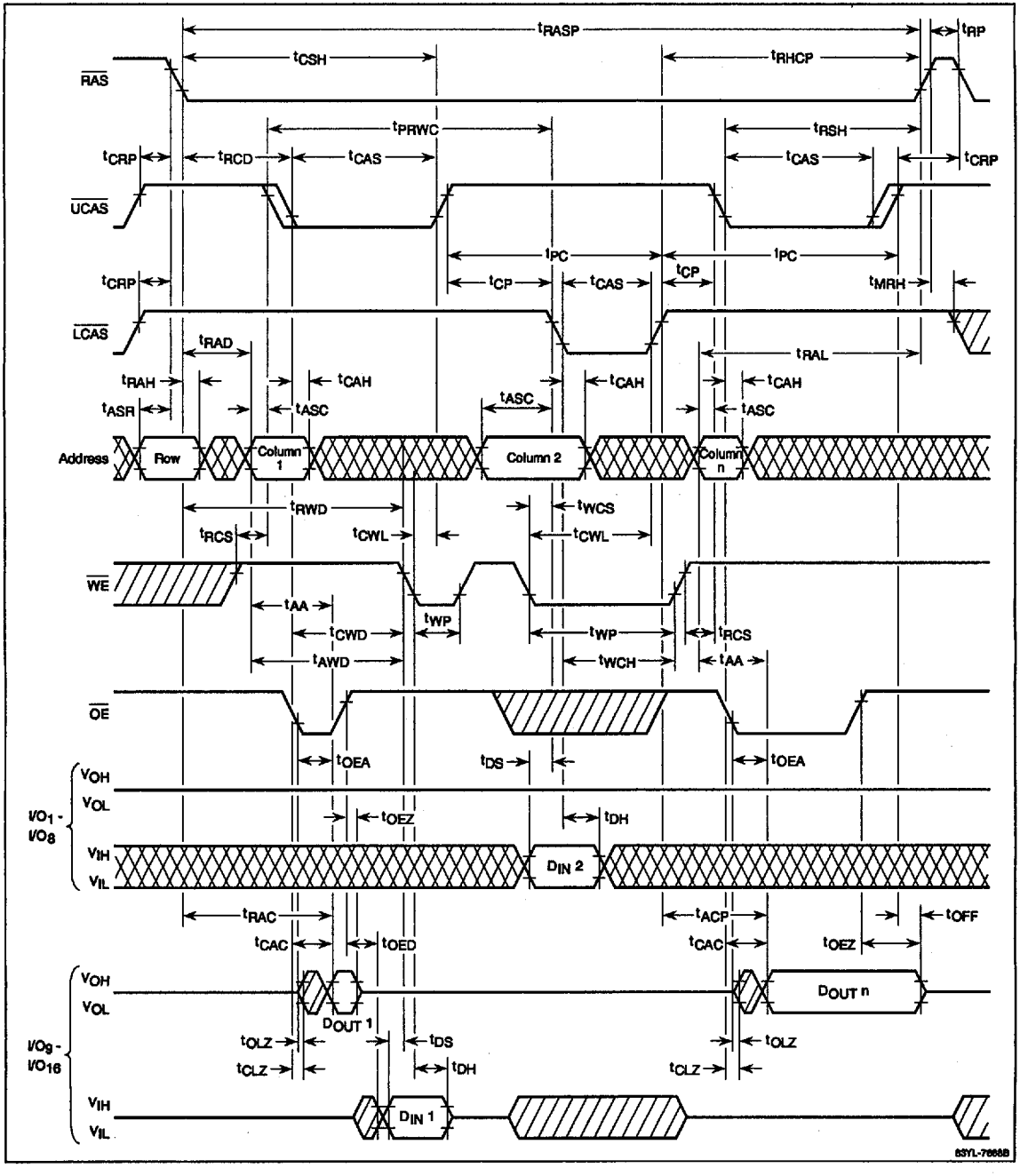
## Timing Waveforms (cont)

### *Byte Fast-Page Late-Write Cycle*



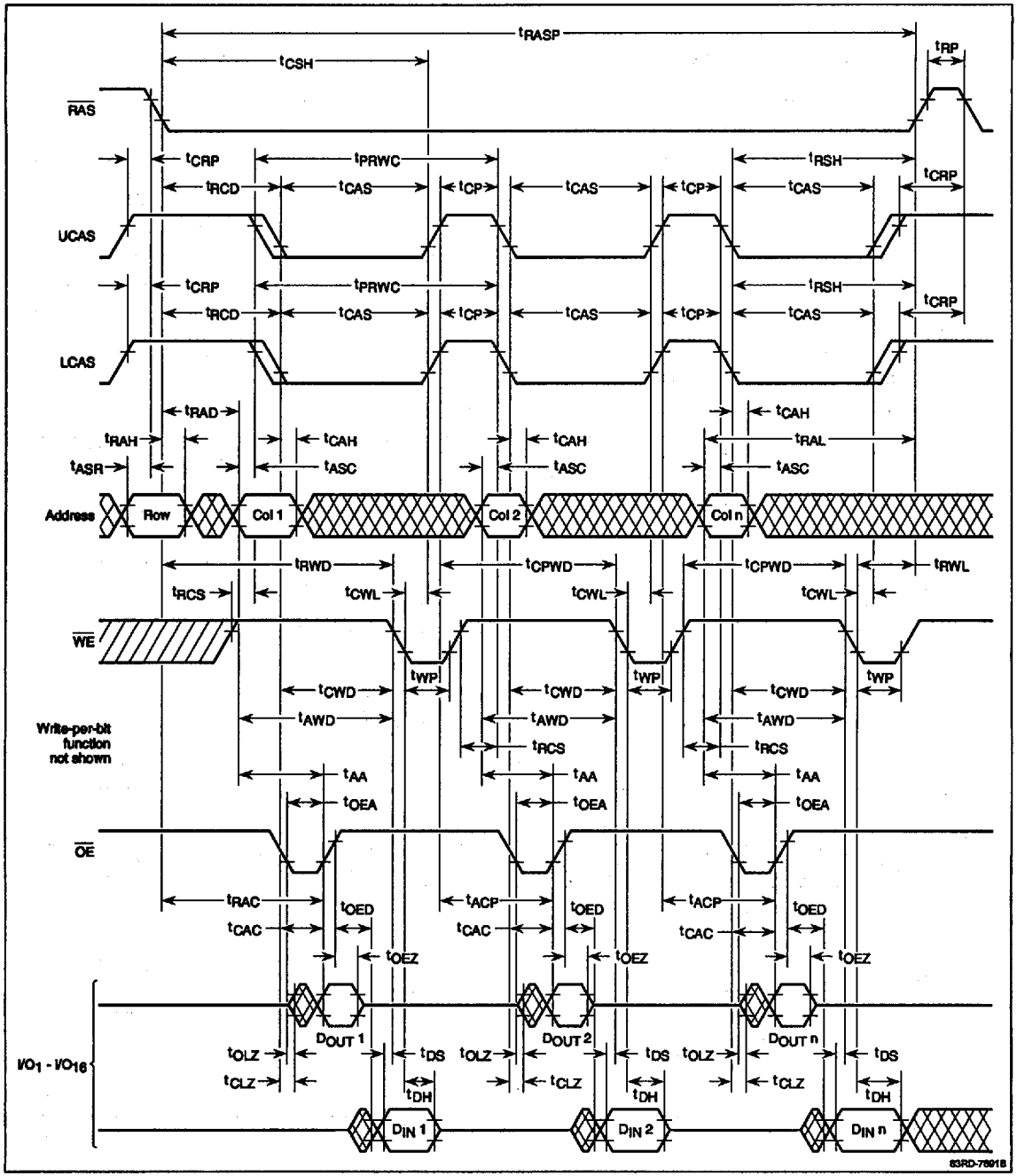
## Timing Waveforms (cont)

### *Byte Fast-Page Read/Write Cycle*



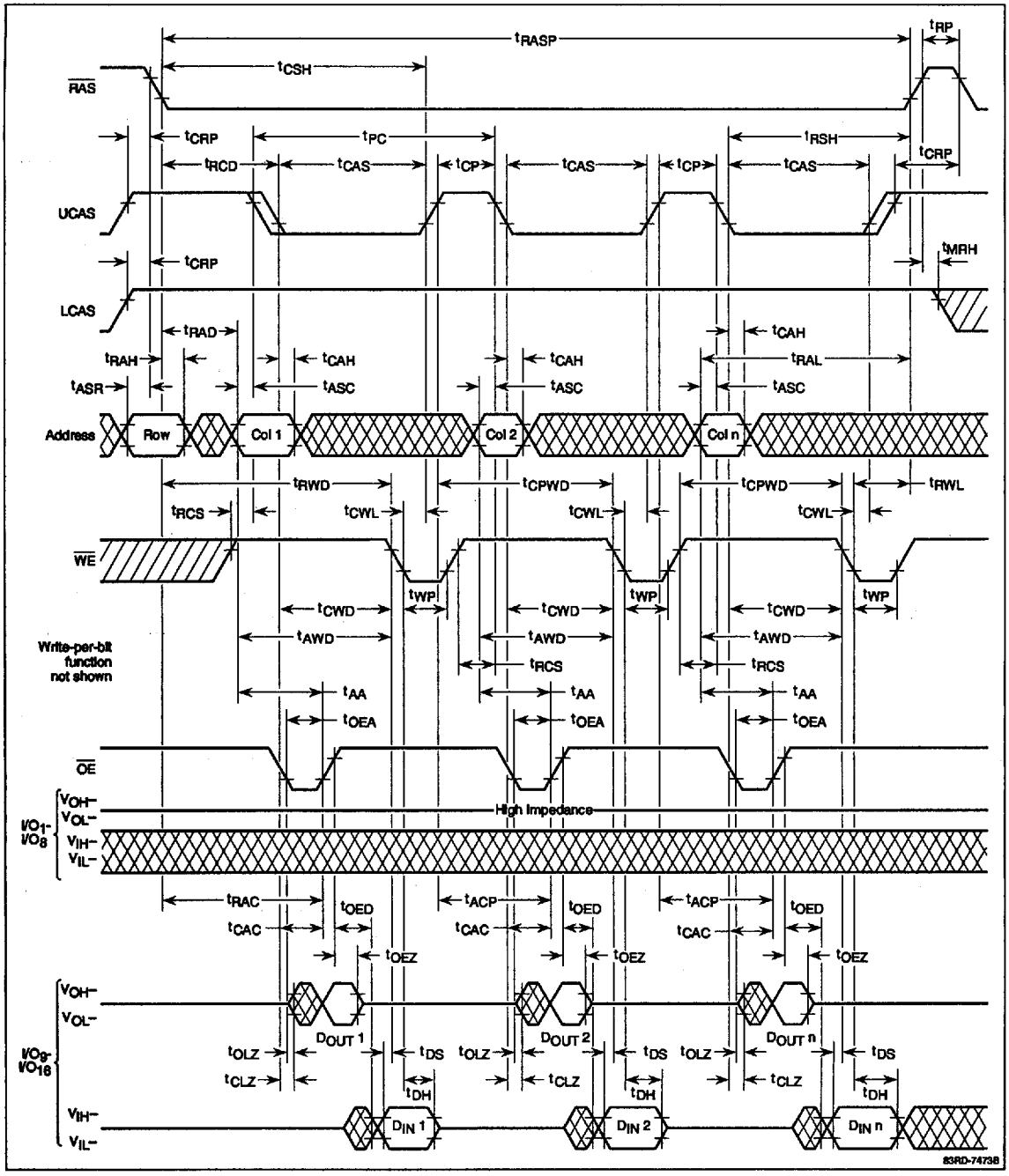
## Timing Waveforms (cont)

### *Word Fast-Page Read-Modify-Write Cycle*



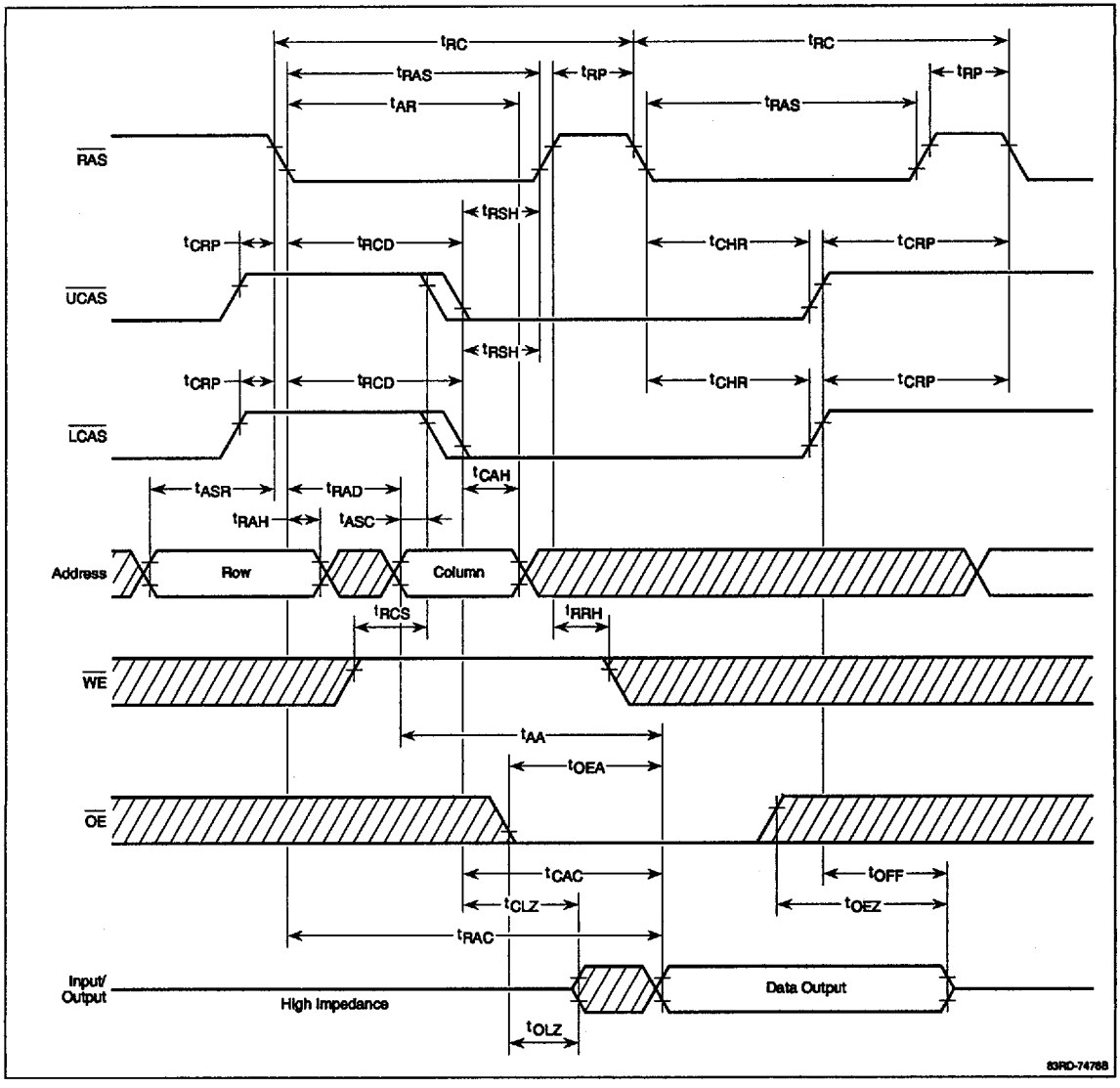
## Timing Waveforms (cont)

### *Byte Fast-Page Read-Modify-Write Cycle*



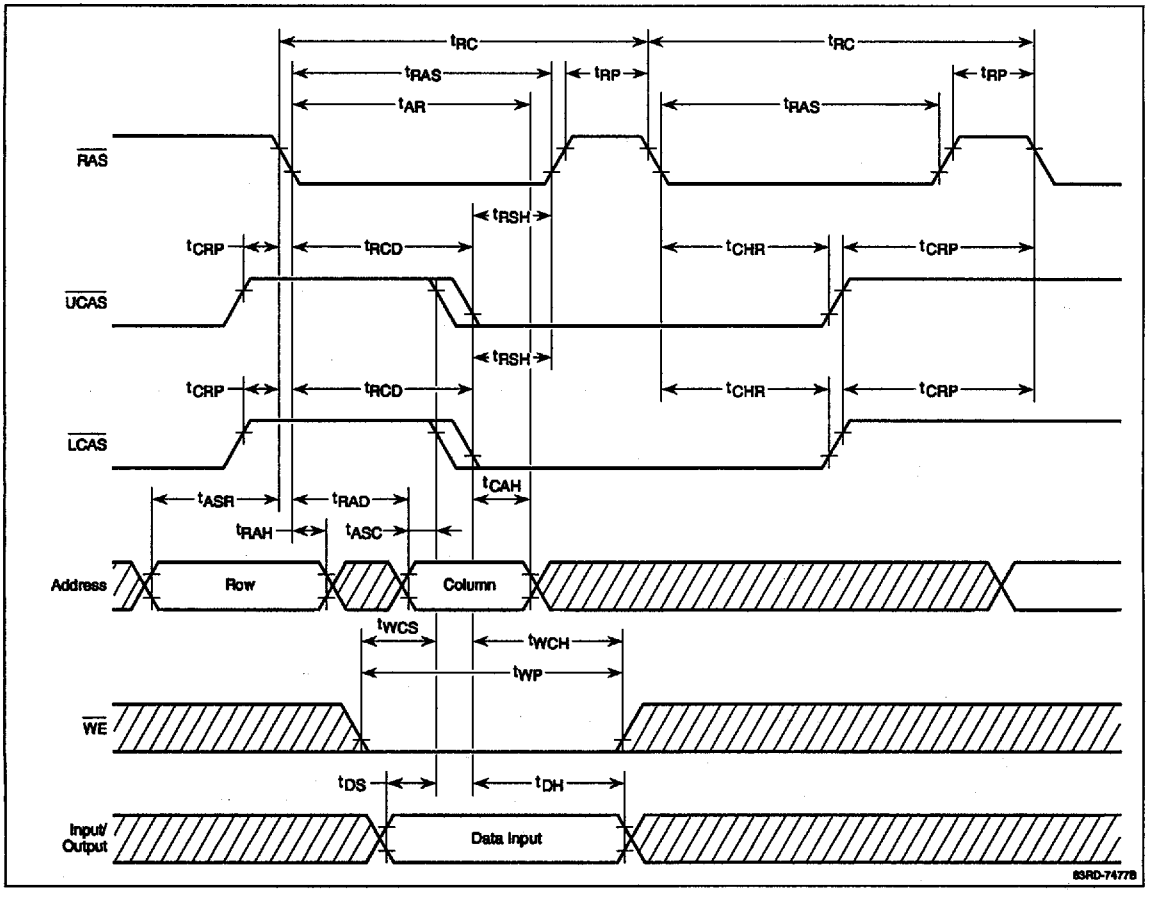
## Timing Waveforms (cont)

### *Hidden-Refresh Cycle (Word Read Cycle)*



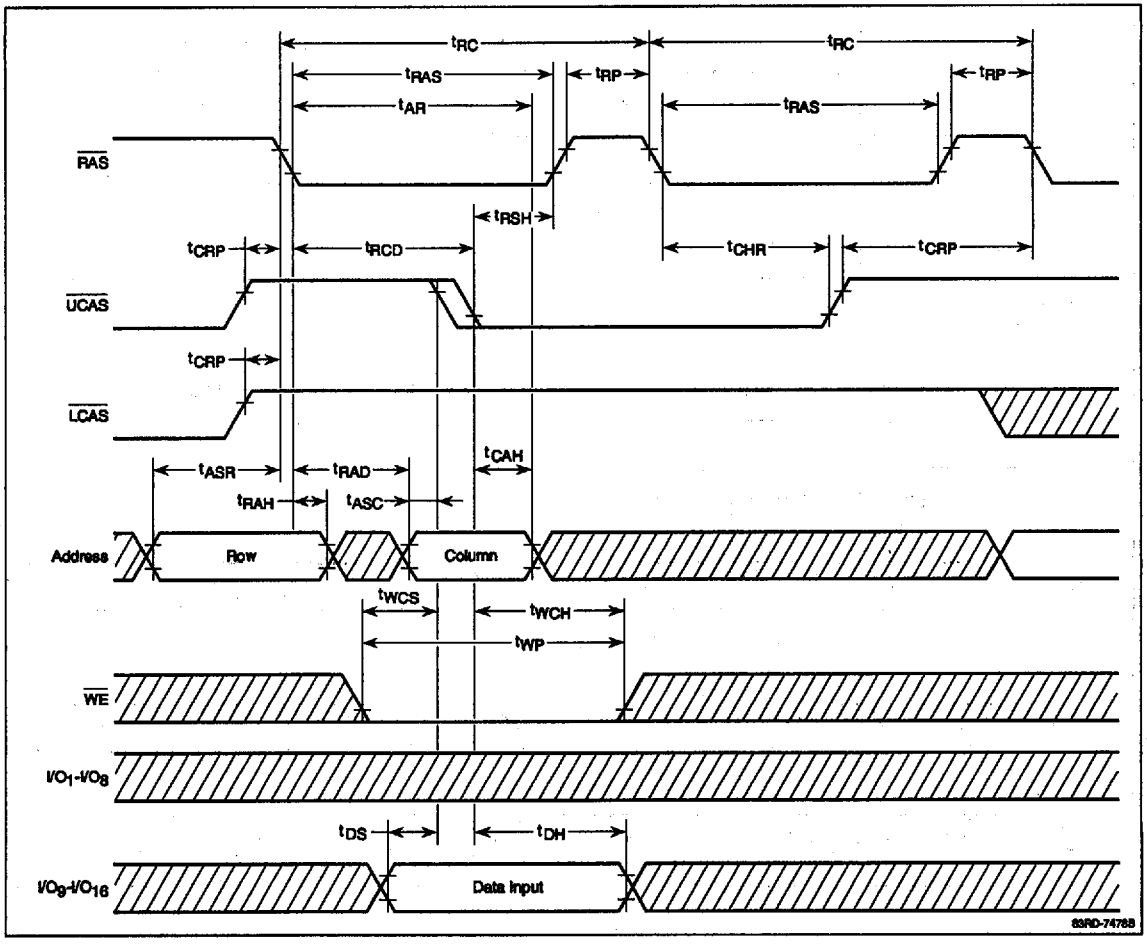
## Timing Waveforms (cont)

***Hidden-Refresh Cycle (Word Write Cycle)***



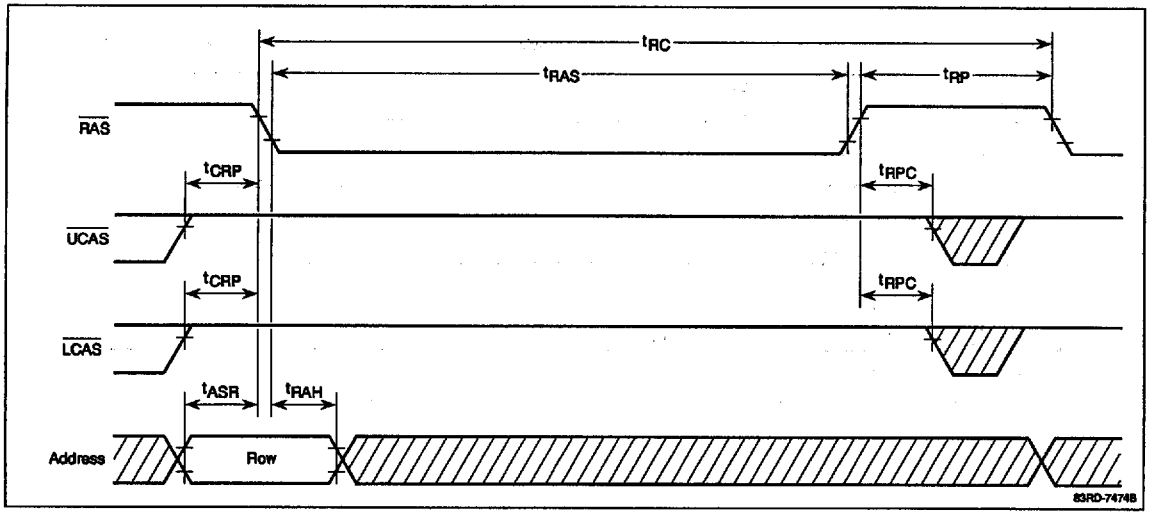
## Timing Waveforms (cont)

### *Hidden-Refresh Cycle (Byte Write Cycle)*

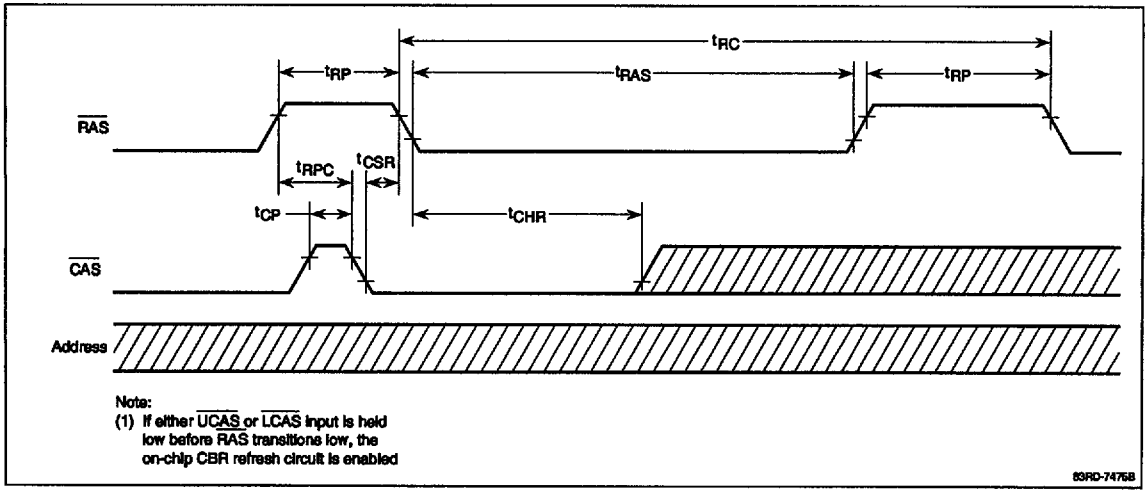


## Timing Waveforms (cont)

### *$\overline{RAS}$-Only Refresh Cycle*




### *$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle*



## Timing Waveforms (cont)

### *CBR Self-Refresh Cycle*