



NEC Electronics Inc.

**μPD431000A**  
**131,072 x 8-Bit**  
**Static CMOS RAM**

T-46-23-14

**Description**

The μPD431000A is a 131,072-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431000A a high-speed device that requires very low power and no clock or refreshing.

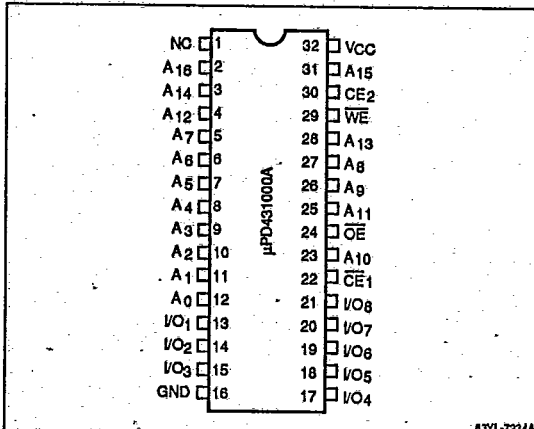
Minimum standby power is drawn when CE<sub>2</sub> is low, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 volts. The μPD431000A is available in standard 32-pin plastic DIP, 32-pin plastic miniflat, and 32-pin plastic TSOP packaging.

**Features**

- 131,072-word by 8-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Two CE pins and one OE pin for easy application
- Data retention current of 1 μA typical
- Data retention voltage of 2 V minimum
- Standard 32-pin plastic DIP, miniflat and TSOP packaging

**Pin Configurations**

**32-Pin Plastic DIP or Miniflat**



**Pin Identification**

Symbol	Function
A <sub>0</sub> - A <sub>16</sub>	Address Inputs
I/O <sub>0</sub> - I/O <sub>7</sub>	Data Inputs/outputs
OE <sub>1</sub> , CE <sub>2</sub>	Chip enables 1 and 2
OE	Output enable
WE	Write enable
GND	Ground
VCC	+5-volt power supply
NC	No connection

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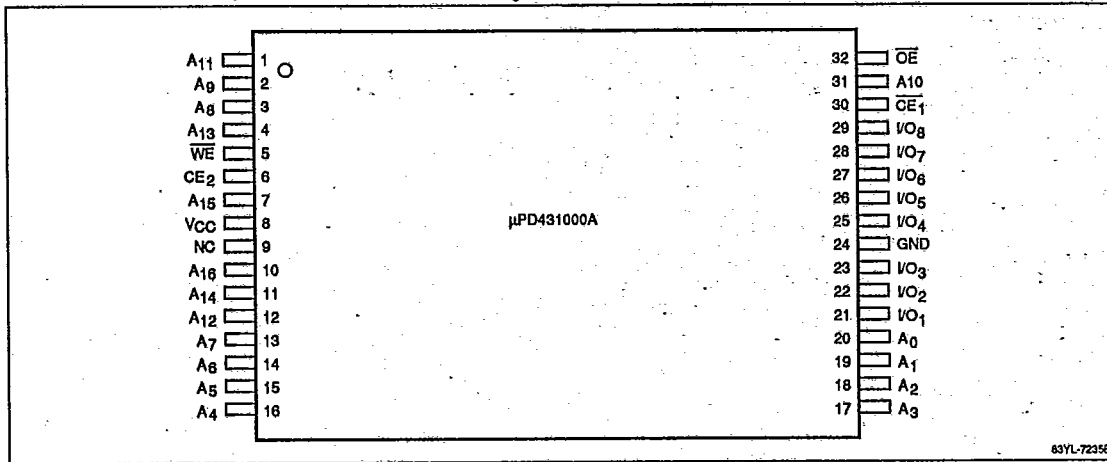
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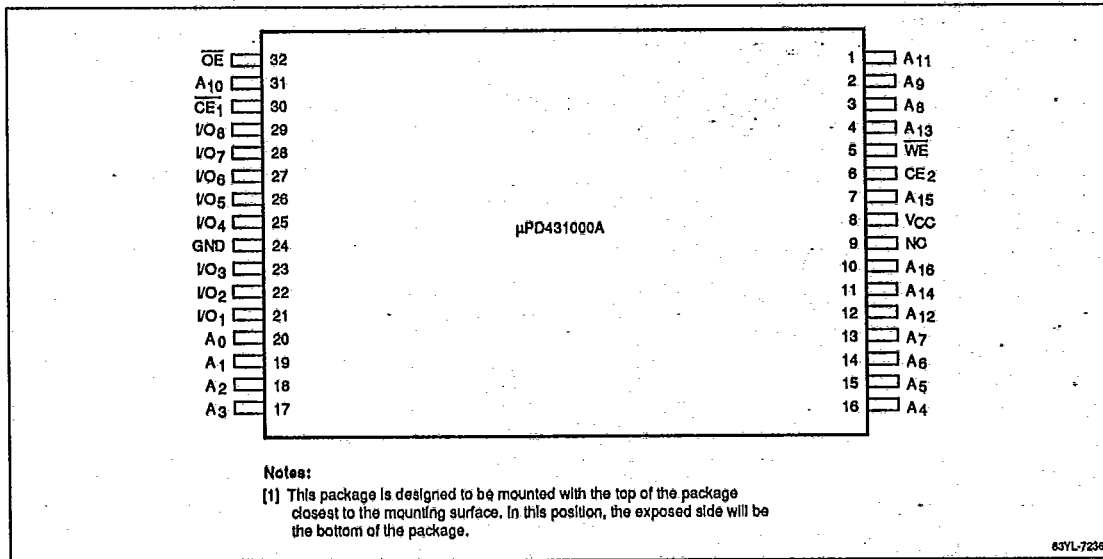
**Pin Configurations (cont)**

**32-Pin Plastic TSOP (normal leads, top view)**



83YL-7235B

**32-Pin Plastic TSOP (reverse bent leads, bottom view)**



**Notes:**

[1] This package is designed to be mounted with the top of the package closest to the mounting surface. In this position, the exposed side will be the bottom of the package.

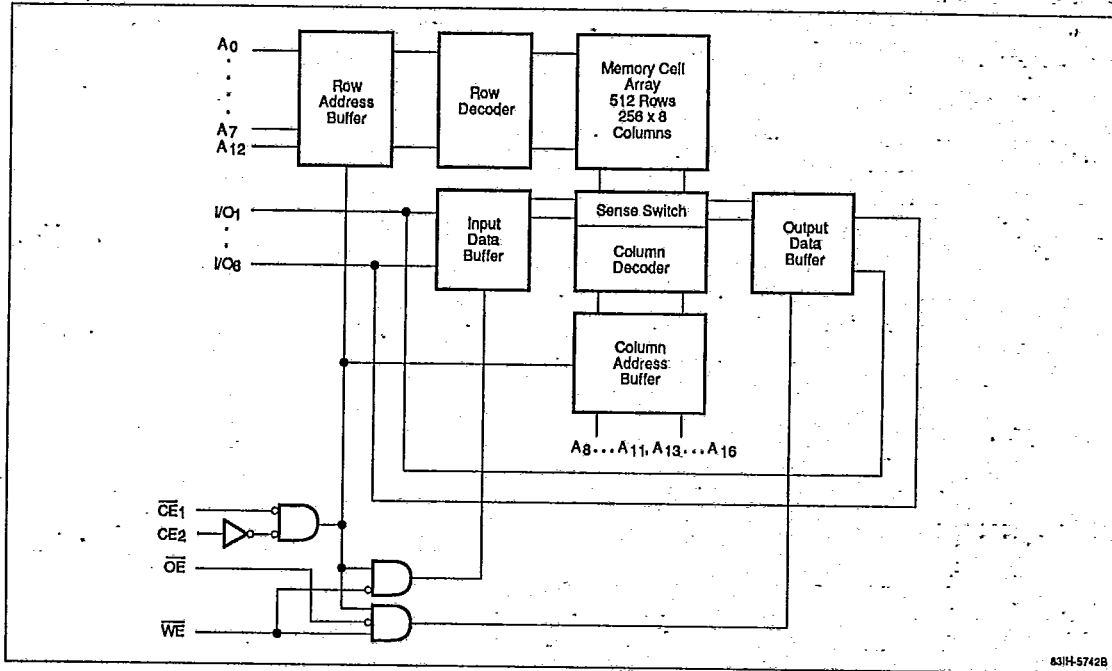
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Block Diagram



631H-5742B

Absolute Maximum Ratings

Supply voltage, $V_{CC}$ (Note 1)	-0.5 to +7.0 V
Input voltage, $V_{IN}$ (Note 1)	-0.5 to $V_{CC} + 0.5$ V
Output voltage, $V_{IO}$ (Note 1)	-0.5 to $V_{CC} + 0.5$ V
Operating temperature, $T_{OPR}$	0 to +70°C
Storage temperature, $T_{STG}$	-55 to +125°C
Power dissipation, $P_D$	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) -3.0 V minimum (pulse width = 50 ns).

Capacitance

$T_A = +25^\circ\text{C}$ ;  $f = 1$  MHz;  $V_{IN}$  and  $V_{OUT} = 0$  V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	$C_i$			6	pF
Input/output capacitance	$C_{IO}$			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Input voltage, high	$V_{IH}$	2.2		$V_{CC} + 0.5$	V
Ambient temperature	$T_A$	0		70	°C

Notes:

(1) -3.0 V minimum (pulse width = 50 ns).

Truth Table

Function	$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	I/O	$I_{CC}$
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
Selected	L	H	H	H	High-Z	Active
Read	L	H	L	H	$D_{OUT}$	Active
Write	L	H	X	L	$D_{IN}$	Active

Notes:

(1) X = don't care.



**μPD431000A****NEC**

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**Ordering Information**

Part Number	Access Time (max)	I <sub>SB1</sub> (max)	Package
μPD431000AGZ-70	70 ns	2 mA	32-pin plastic DIP
CZ-85	85 ns		
CZ-10	100 ns		
μPD431000AGZ-70L	70 ns	0.1 mA	
CZ-85L	85 ns		
CZ-10L	100 ns		
μPD431000AGW-70L	70 ns	0.1 mA	32-pin plastic miniflat
GW-85L	85 ns		
GW-10L	100 ns		
μPD431000AGZ-70-KJH	70 ns	2 mA	32-pin plastic TSOP (normal leads)
GZ-85-KJH	85 ns		
GZ-10-KJH	100 ns		
μPD431000AGZ-70L-KJH	70 ns	0.1 mA	
GZ-85L-KJH	85 ns		
GZ-10L-KJH	100 ns		
μPD431000AGZ-70-KKH	70 ns	2 mA	32-pin plastic TSOP (reverse bent leads)
GZ-85-KKH	85 ns		
GZ-10-KKH	100 ns		
μPD431000AGZ-70L-KKH	70 ns	0.1 mA	
GZ-85L-KKH	85 ns		
GZ-10L-KKH	100 ns		

**Notes:**

- (1) Contact your NEC sales representative for data sheet and product availability for the -LL version of the μPD431000A.

**DC Characteristics**T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I <sub>LI</sub>	-1		1	μA	V <sub>IN</sub> = 0 V to V <sub>CC</sub>
I/O leakage current	I <sub>LO</sub>	-1		1	μA	V <sub>I/O</sub> = 0 V to V <sub>CC</sub> ; $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I <sub>COA1</sub>		40	70	mA	$\overline{CE}_1 = V_{IL}$ ; $CE_2 = V_{IH}$ ; t <sub>RC</sub> = t <sub>RC</sub> (min); I <sub>I/O</sub> = 0 mA
	I <sub>COA2</sub>			15	mA	$\overline{CE}_1 = V_{IL}$ ; $CE_2 = V_{IH}$ ; I <sub>I/O</sub> = 0 mA
	I <sub>COA3</sub>			10	mA	V <sub>CE1</sub> ≤ 0.2 V; V <sub>CE2</sub> ≥ V <sub>CC</sub> - 0.2 V; t <sub>RC</sub> or t <sub>WO</sub> = 1 MHz; V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V
Standby supply current	I <sub>SB</sub>			5	mA	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ (Note 1)
	I <sub>SB1</sub>		0.02	2	mA	$\overline{CE}_1$ and $CE_2 \geq V_{CC} - 0.2 V$ (Note 2)
	I <sub>SB2</sub>		0.02	2	mA	$CE_2 \leq 0.2 V$ (Note 2)
Output voltage, low	V <sub>OL</sub>			0.4	V	I <sub>OL</sub> = 2.1 mA
Output voltage, high	V <sub>OH</sub>	2.4			V	I <sub>OH</sub> = -1.0 mA

**Notes:**

- (1) I<sub>SB</sub> = 3 mA (max) for -L versions.  
 (2) I<sub>SB1</sub> and I<sub>SB2</sub> = 0.02 mA (typ) and 0.1 mA (max) for -L versions.

**NEC****μPD431000A****T-46-23-14****AC Characteristics** $T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0\text{V} \pm 10\%$ 

Parameter	Symbol	μPD431000A-70		μPD431000A-85		μPD431000A-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
<b>Read Operation</b>									
Read cycle time	$t_{RC}$	70		85		100		ns	
Address access time	$t_{AA}$		70		85		100	ns	(Note 2)
$\overline{CE}_1$ access time	$t_{CO1}$		70		85		100	ns	(Note 2)
$CE_2$ access time	$t_{CO2}$		70		85		100	ns	(Note 2)
Output enable to output valid	$t_{OE}$		35		45		50	ns	(Note 2)
Output hold from address change	$t_{OH}$	10		10		10		ns	
$\overline{CE}_1$ to output in low-Z	$t_{LZ1}$	10		10		10		ns	(Note 3)
$CE_2$ to output in low-Z	$t_{LZ2}$	10		10		10		ns	(Note 3)
Output enable to output in low-Z	$t_{OLZ}$	5		5		5		ns	(Note 3)
$\overline{CE}_1$ to output in high-Z	$t_{HZ1}$		25		30		35	ns	(Note 3)
$CE_2$ to output in high-Z	$t_{HZ2}$		25		30		35	ns	(Note 3)
Output enable to output in high-Z	$t_{OHZ}$		25		30		35	ns	(Note 3)
<b>Write Operation</b>									
Write cycle time	$t_{WC}$	70		85		100		ns	
$\overline{CE}_1$ to end of write	$t_{CW1}$	60		75		90		ns	
$CE_2$ to end of write	$t_{CW2}$	60		75		90		ns	
Address valid to end of write	$t_{AW}$	60		75		90		ns	
Address setup time	$t_{AS}$	0		0		0		ns	
Write pulse width	$t_{WP}$	55		65		75		ns	
Write recovery time	$t_{WR}$	5		5		5		ns	
Data valid to end of write	$t_{DW}$	35		35		40		ns	
Data hold time	$t_{DH}$	0		0		0		ns	
Write enable to output in high-Z	$t_{WHZ}$		25		30		35	ns	(Note 3)
Output active from end of write	$t_{OW}$	5		5		5		ns	(Note 3)

**Notes:**

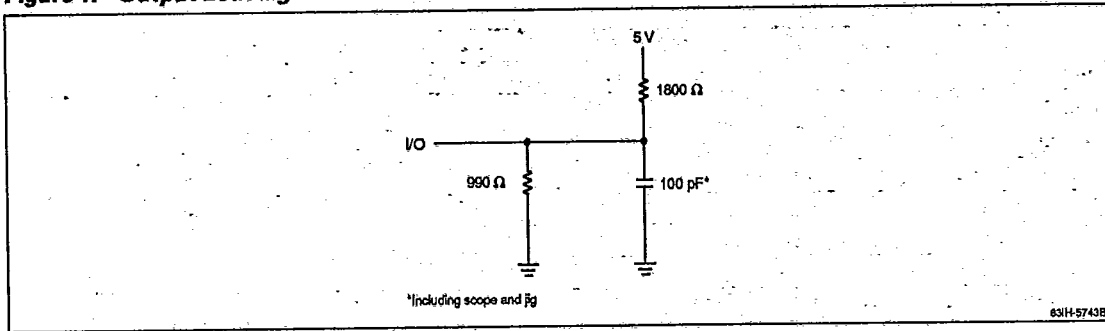
- (1) Input pulse levels = 0.8 to 2.2 V; Input rise and fall times = 5 ns; timing reference levels = 1.5 V.
- (2) See figure 1 for output loading.
- (3) See figure 2 for output loading.

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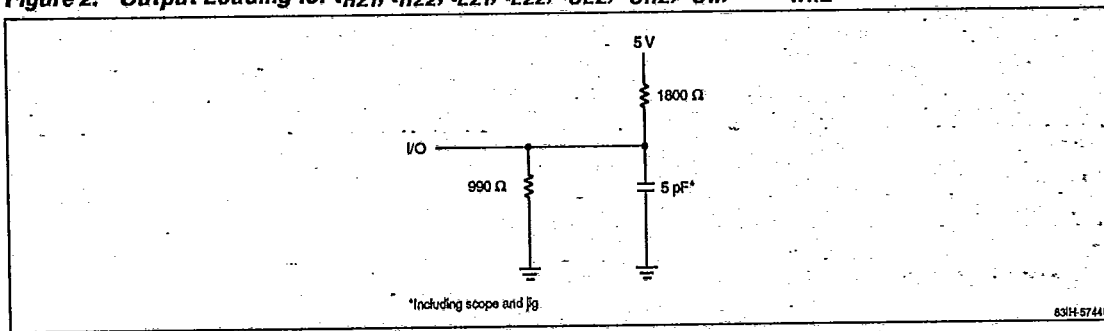
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**Figure 1. Output Loading**



**Figure 2. Output Loading for  $t_{HZ1}$ ,  $t_{HZ2}$ ,  $t_{LZ1}$ ,  $t_{LZ2}$ ,  $t_{OLZ}$ ,  $t_{OHZ}$ ,  $t_{OW}$ , and  $t_{WHZ}$**



**Low  $V_{CC}$  Data Retention Characteristics (-L Version Only)**

$T_A = 0$  to  $+70^\circ\text{C}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	$V_{CCDR1}$	2		5.5	V	$CE_1 \geq V_{CC} - 0.2\text{V}$ ; $CE_2 \geq V_{CC} - 0.2\text{V}$ or $CE_2 \leq 0.2\text{V}$
	$V_{CCDR2}$	2		5.5	V	$CE_2 \leq 0.2\text{V}$
Data retention supply current	$I_{CCDR1}$		1	50	$\mu\text{A}$	$V_{CC} = 3.0\text{V}$ ; $CE_1 \geq V_{CC} - 0.2\text{V}$ ; $CE_2 \geq V_{CC} - 0.2\text{V}$ or $CE_2 \leq 0.2\text{V}$ (Note 1)
	$I_{CCDR2}$		1	50	$\mu\text{A}$	$V_{CC} = 3.0\text{V}$ ; $CE_2 \leq 0.2\text{V}$ (Note 1)
Chip deselection to data retention	$t_{CDR}$	0			ns	
Operation recovery time	$t_R$	5			ms	

**Notes:**

(1) At 0 to  $40^\circ\text{C}$ , the maximum for  $I_{CCDR1}$  and  $I_{CCDR2}$  is  $15\ \mu\text{A}$ .



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Figure 3.  $\overline{CE}_1$ -Controlled Data Retention Timing

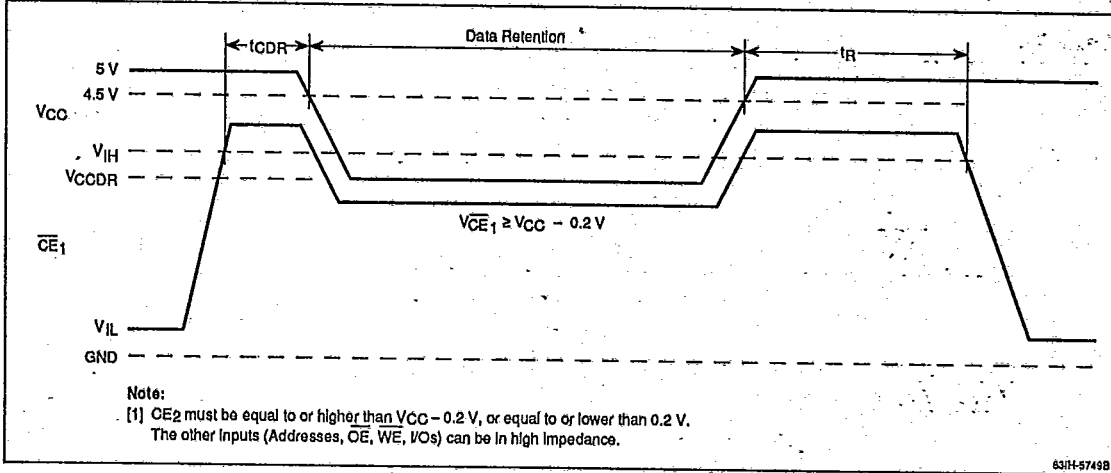
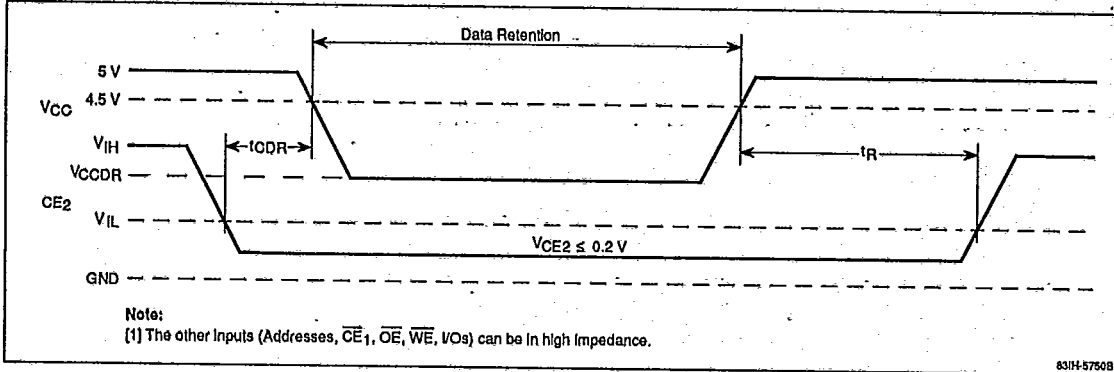


Figure 4.  $\overline{CE}_2$ -Controlled Data Retention Timing



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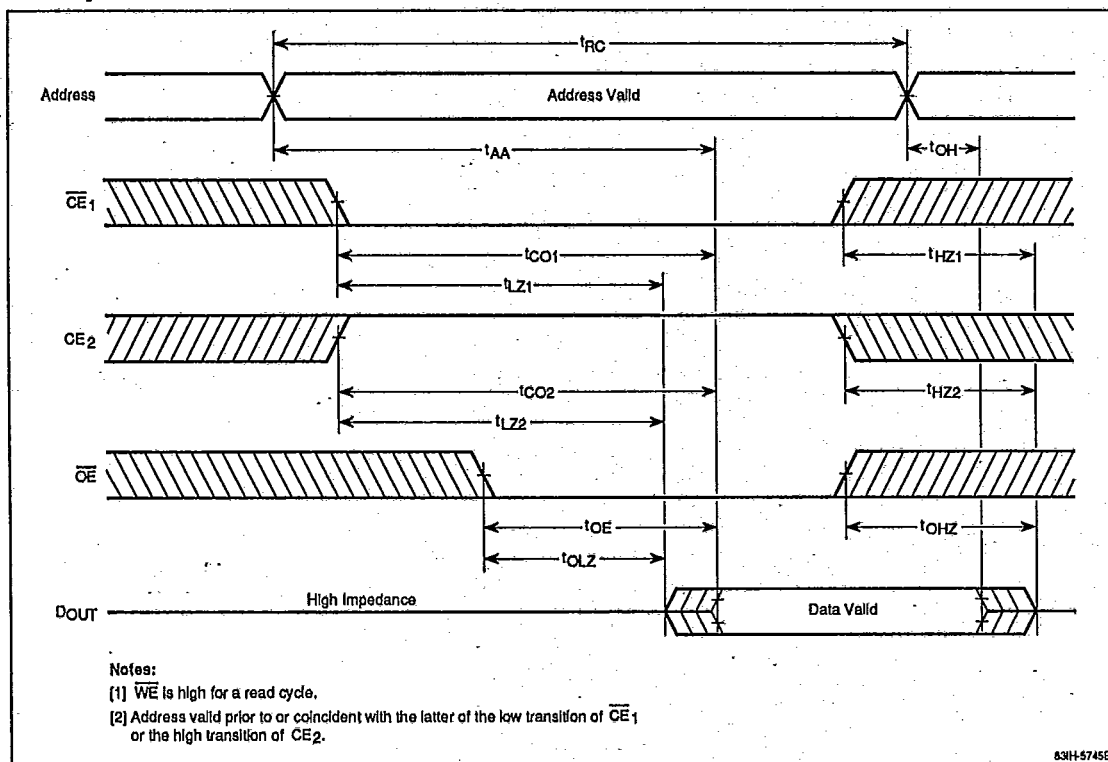
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**Timing Waveforms**

**Read Cycle**



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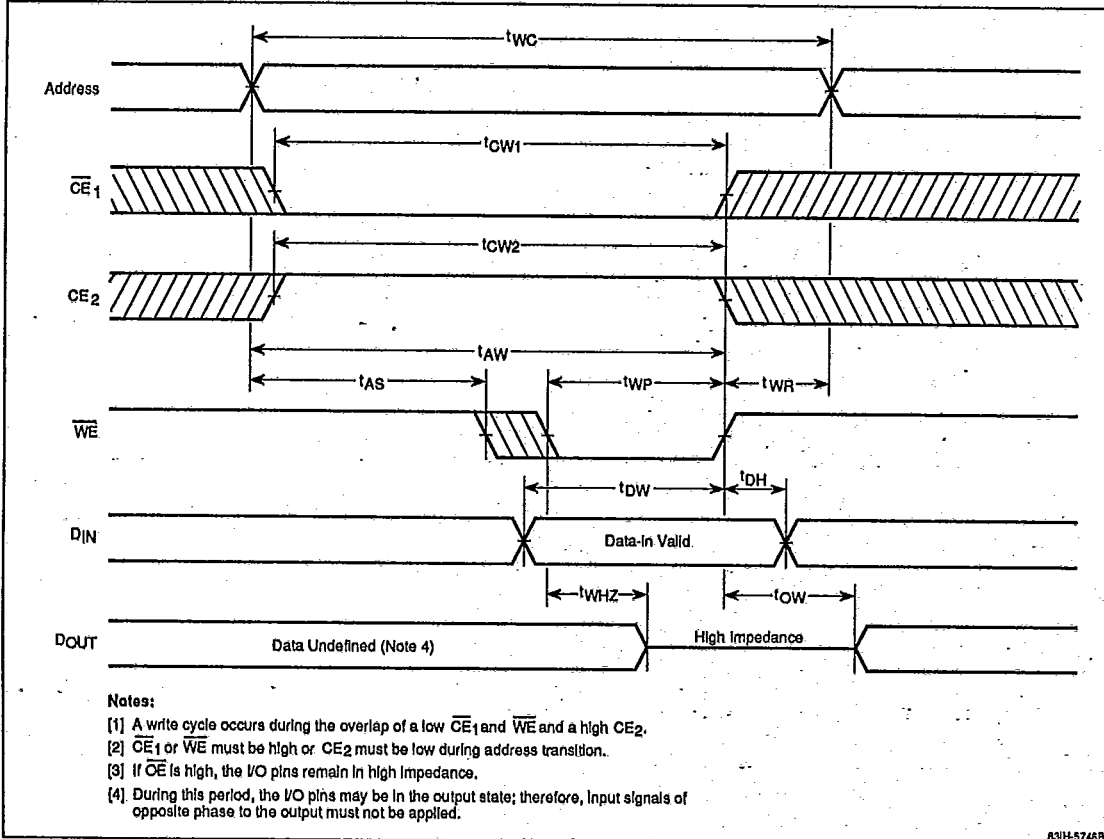


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Timing Waveforms (cont)

**$\overline{WE}$ -Controlled Write Cycle**



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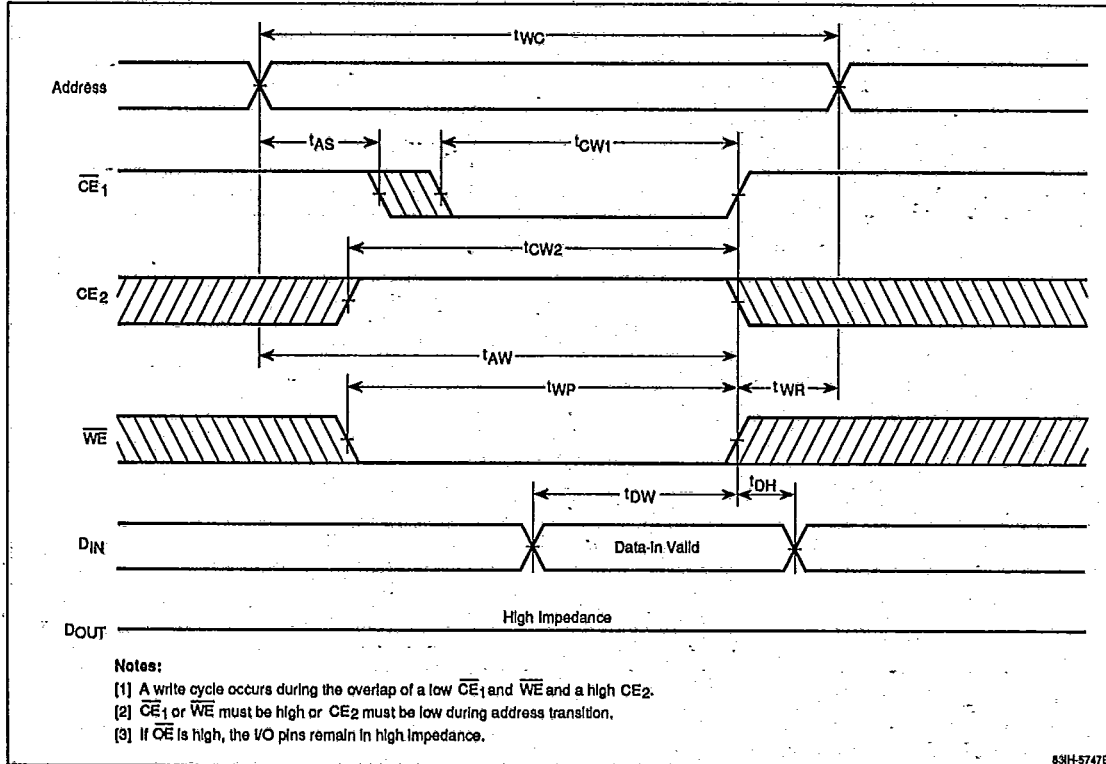
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Timing Waveforms (cont)

**$\overline{CE}_1$ -Controlled Write Cycle**



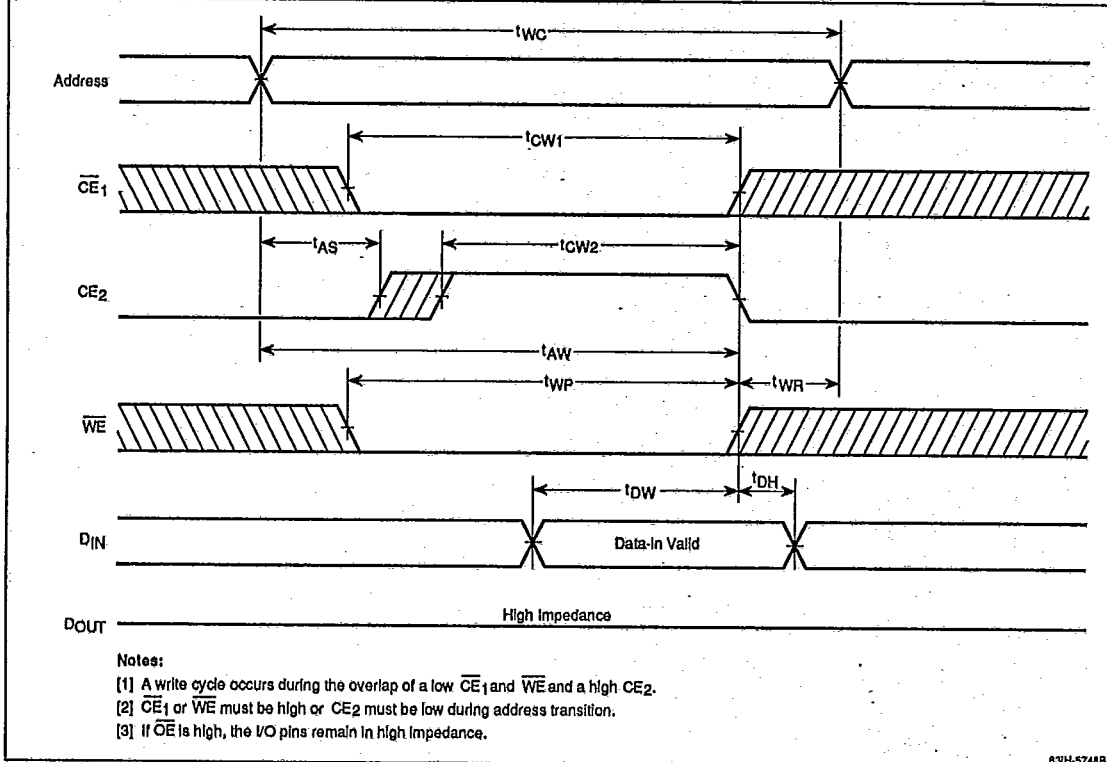


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Timing Waveforms (cont)

$CE_2$ -Controlled Write Cycle



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