Gigabit Ethernet PHY Solutions

Users Manual

GigaPHY-SD

Gphysd_1b
Gigabit Evaluation Board

GigaPHY(TM) -SD Device

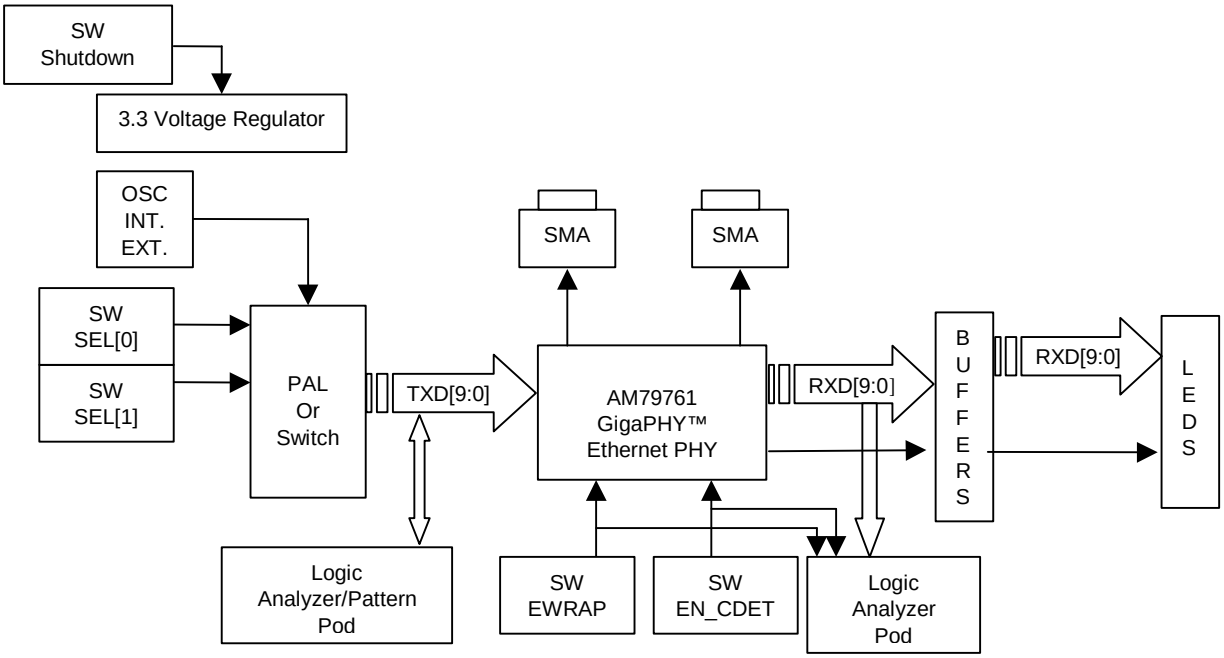
Physical Layer 10-Bit Transceiver for Gigabit Ethernet

Last Updated 11/04/97

Features

- Evaluation System for use in studying the GigaPHY™ Am79761.
- Switches for Driving Control Lines.
- LED's for Monitoring Control Lines.
- On Board Generation of 3.3V from External 5V through 12V supply.
- Internal or External Clock Source.
- 10-bit Transmit Data Provided From Switches or onboard PAL or from a Pattern Generator.
- 10-bit Receive Data Monitored on LED's or Through a Logic Analyzer Pod.

Block Diagram



General Description

The GigaPHY™ GPHYSD_1B Board, provides a low cost, easy-to-use tool to evaluate the Gigabit Transceiver, AM79761, with regard to signal quality and performance. It is intended that the GigaPHY™ board be a self-contained Evaluation Unit. In its simplest form, the switches on the GPHYSD_1B can be used to set the transmit data and control lines while monitoring received data and status lines with LED's. A pre-programmed PAL in addition to the switch settings can generate simple word patterns.

More in-depth evaluations can be implemented by connecting a Pattern Generator (10-bits at 125MHz) to pods on the board in order to generate transmit data and control signals. A logic analyzer can also be connected to pods on the board in order to monitor receive data and status signals. With this setup 8B/10B data can be sent to the transmitter on the Evaluation Unit to generate Gigabit data and monitored on the Logic Analyzer.

Other useful features of the board include the presence of an on-board, removable oscillator with Tri-state (normally at 125MHz) in a DIP, half DIP or Surface Mount form. An on-board voltage regulator is used to provide 3.3V to the board with a shutdown switch used to turn off power to all components.

Scope of this Document

It is intended that the AM79761 datasheet be used for reference in understanding the device function. Additionally, the following items are enclosed in this document:

1. Schematics for the board
2. Artwork for the board (copies of each layer)
3. Fabrication drawing for the board
4. Bill of materials for the board.

Operation and Switch Settings

HP1	TXD Logic Analyzer/Pattern input
HP2	RXD Logic Analyzer
LED0	RXD[0] Status
LED1	RXD[1] Status
LED2	RXD[2] Status
LED3	RXD[3] Status
LED4	RXD[4] Status
LED5	RXD[5] Status
LED6	RXD[6] Status
LED7	RXD[7] Status
LED8	RXD[8] Status
LED9	RXD[9] Status
LED10	COMDET Comma Character Status
LED11	+5POS External Power Supply Input indicator
LED12	+3.3 Power Supply Input indicator
LED13	/SHDN Status for Voltage Regulator if [ON] Shutdown [OFF] Enabled
LED14	SEL[0]
LED15	SEL[1]
LED16	EWRAP
LED17	EN_CDET
P1	/SHDN [H] Voltage Regulator is [ON] Power to DUT [L] Shuts down the Voltage Regulator[OFF] No power to DUT.
P2	SEL[0]
P3	SEL[1]
P4	EWRAP
P5	EN_CDET
PWR1	Ext. Lab bench +5V DC supply
PWR2	Ext. Wallmount +5V DC supply
SMA1	External 125Mhz Clock Install [0]ohm resistor R2 and W1[to Tristate Clock Crystal].
SMA2	TX[+] Output
SMA3	TX[-] Output
SMA4	RX[+] Output
SMA5	RX[-] Output
SMA6	RCLKN Output
SMA7	RCLK Output
SW1	Manual Setting to TXD[0:9]
U1	AM79761
U2	PAL for TXD[0:9] inputs
U3	Buffer to LED's
U4	Buffer to LED's
VR1	+5POS to +3.3POS Voltage Regulator with Shutdown.
W1	TRI-STATE Jumper to Tri-State Clock Crystal output.
X1	125 MHz Clock Crystal.
ZTP1	VDDIN [+5 volt power supply].
ZTP2	+5POS going to Voltage regulator.
ZTP3,5,6,7	DVSS
ZTP4	DVSS

Operation

The GigaPHY™ eval board provides potential customers with a simple, easy-to-use evaluation tool for understanding the function and performance of the AM79761 10-bit Gigabit Transceiver.

A 125MHz 3.3V crystal oscillator provides a reference clock (REFCLK) to the AM79761. The clock trace has been minimized to provide the best signal quality possible. Since REFCLK is used to latch data into the AM79761, the trace length between the REFCLK clock and the TXD[0-9] data should be kept somewhat similar (i.e. within 1") so as to maximize the timing margin for the chip generating the transmit data. The recovered clocks, RCLK and RCLKN, can be monitored through the SMA connectors.

The TEST pins of the AM79761 are tied HIGH for manual switch operation. The EN_CDET pin, which is set by a switch, allows SYNC detection and framing. When EN_CDET is enabled, the detection of COMMA will generate a COM_DET, which is monitored by an LED. In order to select loopback mode, the EWRAP must be HIGH which will cause the parallel input data TXD[0-9] be wrapped around inside the AM79761 and outputed as RXD[0-9] and the TX[+/-] outputs will be held high.

The on board 125 MHz oscillator generates the transmit clock for the AM79761 (REFCLK). TXD[0-9] is latched into the AM79761 on every rising edge of this clock. The AM79761 recovers the data with the word-oriented clock (RBC-) at 62.5MHz.

An on-board diagnostic path is provided to allow testing of the board. The input parallel data can be generated by a 10-bit switch or by a pre-programmed PAL. The 10-bit switch only allows a static 10 bit word pattern but the PAL can be used to generate a longer repetitious word patterns. A more sophisticated word pattern can be generated from a Pattern Generator through the pod connector. If non-loopback mode is selected, the parallel, TXD[0-9], will be serialized by the AM79761 and pumped out through the TX[+/-]. Then, the high-speed serial data is received through the RX[+/-] into the AM79761 and is deserialized to a 10-bit parallel data bus, RXD[0-9]. LED's or a logic analyzer through the on-board pod can monitor the RXD[0-9].

For a 50 ohm environment, the AM79761 transmitters PECL outputs drive 50 ohm traces with a 182 ohm current sinking resistor and an AC-coupled 0.01uF capacitor to the 50-ohm SMA connectors labeled TX[+] (SMA1) and TX[-] (SMA2). The resistor-capacitor termination circuit are needed to supply current and decouple the 3.3V-referenced PECL outputs of the AM79761 from the PECL-levels required on the coaxial cable. The AM79761 receives differential PECL serial data from the coax cable on the 50-ohm SMA connectors labeled RX+/-. This input is immediately AC-coupled through a 0.01uF capacitor and terminated with 182-ohm pull-down resistors. The AM79761 provides internal resistors to set the DC Bias to Vdd/2. The termination resistors and AC coupling caps are located as near as possible to the input pins on the AM79761 to maximize signal quality.

The Evaluation board has voltage regulator that supplies the board with 3.3Volts. The input to the voltage regulator can be from 5 volts DC to 12 volts DC from either a lab bench supply through PWR1 or from a wall mounted supply through PWR2. The voltage regulator output can be shutdown with the shutdown a switch [P1]. When LED13 is ON the regulator output is OFF.

PAL and Manual Switch Pattern Generator Settings

SEL[0] L	SEL[1] L	Undetermined	Undetermined
SEL[0] L	SEL[1] H	Pseudo-random	
SEL[0] H	SEL[1] L	00111100xx	Repeating 00111100xx
SEL[0] H	SEL[1] H	Alternating	Alternating +/- K28.5

Note; for the PAL to output the right data the Manual switch setting SW1 all have to be off.

Note; for the Manual Switch to work , the PAL has to be removed.

Layout Considerations

The board has been designed in a simple, straightforward manner in which highest priority was given to properly routing of high-speed signals. This four layer, controlled impedance PCB contains signal layers on the top and bottom of the board with internal Power (Vdd=3.3V) and GND planes. Components are mounted on both sides of the board so that passives may be placed as close as possible to their ideal location regardless of which side of the board the part is placed. The PCB accommodates a special socket for the AM79761 so placement of passives on the topside near the pins was not possible.

The 1Gb/s transmit and receive signals between the chipset and the connector were the first priority. Since they form a differential PECL pair these traces were of minimal and equal length and, in this example, have characteristic impedance of 50 ohm. The passive components should be packed as closely as possible to minimize stub lengths and maximize signal quality. On the receiver inputs, minimization of trace length between the AC Coupling Caps (C28/C29), the input pins (RX[+],RX[-]) and the 182 ohm termination resistors are very important since the terminator resistors act as the virtual end of the line. Stubs on these lines will cause degradation of signal quality into the receivers due to reflections.

Diagonal corners were used so as to avoid the impedance mismatches found in right angle traces. The same considerations as other high-speed signals apply here.

Transmit data jitter is generated through two main factors: Power Supply Noise and TBC jitter. Proper layout of the REFCLK traces is essential to minimize REFCLK jitter into the part. Curved traces are used to minimize reflections. Generous bypassing of the power supplies and separate isolation and decoupling for each sensitive supply type is one easy method to eliminate much of this noise.

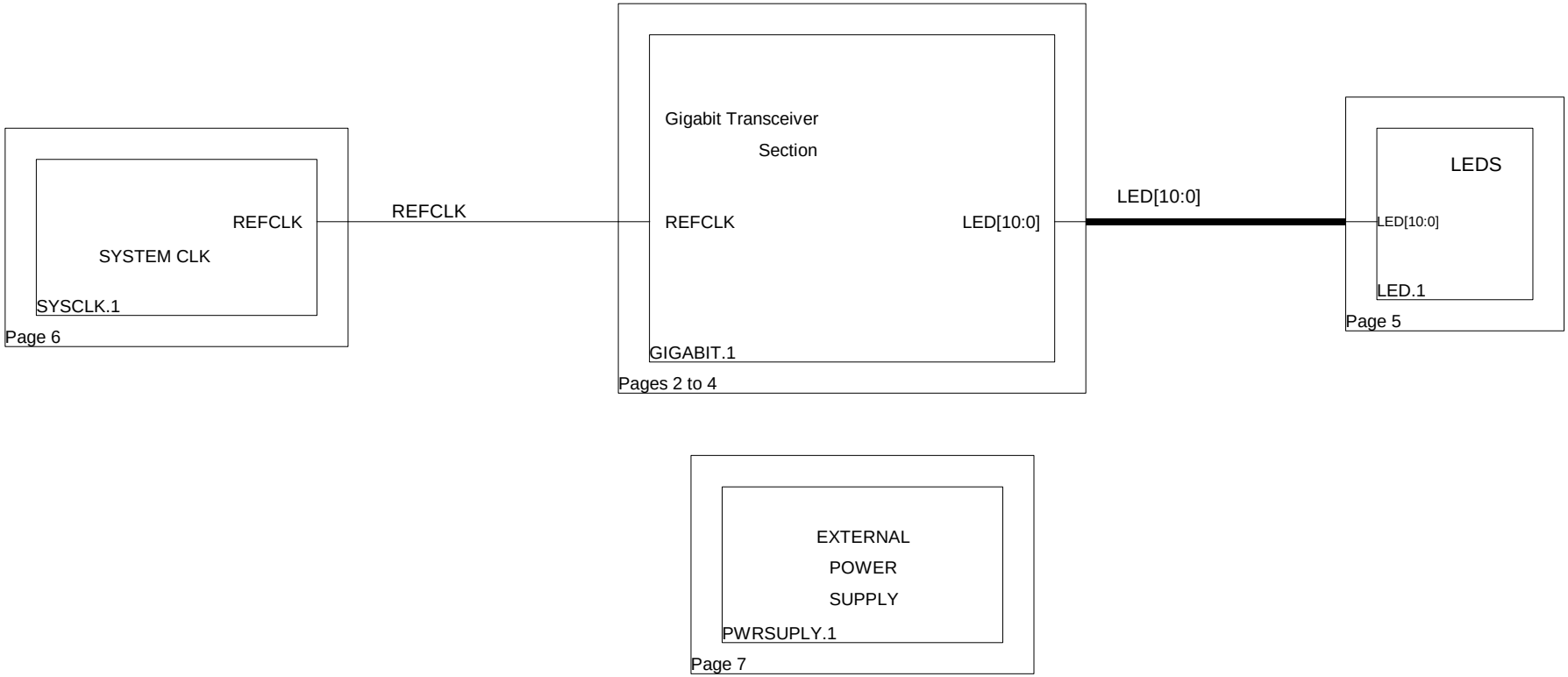
In general, common layout/placement techniques developed for lower speed PCBs apply here and should lead to first-pass success.

Table 1: Bill of Materials

Item	Qty.	Device Description	Part Number	Manufacture	Reference Number
1)	2	Straight .1"x.1" 20 pin Low Profile Header	2520-6002UG	3M	HP1-2
2)	1	Gigabit Ethernet Transceiver	AM79761	AMD	U1
3)	1	2 pin jumper	103240-1	AMP	W1
4)	1	Shunt	15-38-1024	MOLEX	W1
5)	1	Euro Terminal Block 2 PIN	5LEV-02	Augot	PWR1
6)	1	10 Position Surface Mount Extended Actuator Dip Switch	ADE10S	Augot/Alcoswitch	SW1
7)	5	Surface Mount Toggle Switch SPDT	GT11MSCKE	C&K	P1-5
8)	7	P.C. Pin	10-8025-2-03	Concord	ZTP1-7
9)	1	Power Supply Jack	PJ-002	Cui/Stack Inc.	PWR2
10)	1	49.9 ohm Resistor	CRCW080549R9F	DALE	R1
11)	1	0 ohm Resistor	CRCW1206000J	DALE	R3
12)	5	0 ohm Resistor	CRCW0805000J	DALE	R4,R6,R31-33
13)	4	182 ohm Resistor	CRCW12061820F	DALE	R5,R7,R34-35
14)	5	10K ohm Resistor	CRCW08051002F	DALE	R8,R11,R14,R26,R29
15)	16	301 ohm Resistor	CRCW08053010F	DALE	R9,R13,R25,R27,R30,R36-46
16)	1	1K ohm Resistor	CRCW08051001F	DALE	R10
17)	1	619 ohm Resistor	CRCW08056190F	DALE	R12
18)	10	4.75K ohm Resistor	CRCW08054751F	DALE	R15-24
19)	1	750 ohm Resistor	CRCW08057500F	DALE	R28
20)	3	Straight PC mount Jack Receptacle	142-0701-201	E-F-Johnson	SMA1,SMA6-7
21)	4	End Launch PC mount Jack Receptacle	142-0701-801	E-F-Johnson	SMA2-5
22)	1	Wound Bead	29-43-666681	Fair-Rite	FB1
23)	6	0.01MF COG Ceramic Capacitor	C1812C103J5GAC	Kemet	C6-9,C30-31
24)	1	0.1MF X7R Ceramic Capacitor	C1206C104K5RAC	Kemet	C10
25)	1	1000pf X7R Ceramic Capacitor	C0805C102J5RAC	Kemet	C32
26)	1	High Performance EECMOS PLD 3.3volt	GAL22LV10D-4LJ	Lattice	U2
27)	1	28 pin PLCC SMT socket	822066-4	AMP	U2
28)	10	"ULTRA Yellow" Surface Mount LED	SML10Y4B-TR	LEDTRONICS	LED0-9
29)	7	"HI-EFF Green" Surface Mount LED	SML10G4B-TR	LEDTRONICS	LED10-12,LED14-17
30)	1	"ULTRA Red" Surface Mount LED	'SML10R6C-TR	LEDTRONICS	LED13
31)	1	.+3.3V Low Dropout Micropower Voltage Regulator 3A	LT1529CT-3.3	Linear Technology	VR1
32)	1	TO-220 Mounting Kit	Thermalloy	4880	VR1
33)	1	Heat Sink for To-220	Thermalloy	6078B	VR1
34)	1	SMF Omni-Blok Fuse Block with 750MA Fuse	154750	LittleFuse	F1
35)					
36)	1	125 MHz Half-size Clock Crystal 3.3Volt with TRI_STATE	H3390-125	MF Electronics	X1
37)	6	Mini Spring Socket	50935-1	AMP	X1
38)	1	Empty do not stuff	N/A	N/A	R2
39)	2	Low Voltage Octal Buffer/Line Driver	74LCX540WM	National Semiconductor	U3-4
40)	20	0.01MF X7R Ceramic Capacitor	ECU-V1H103KBG	Panasonic	C4-5,C11-21,C23-29
41)	3	33MF Tantalum Chip Capacitor 16WV	293D336X9016D2T	Sprague	C1,C3,C22

GDPHYSD_1B
Eval Board

Item	Qty.	Device Description	Part Number	Manufacture	Reference Number
42)	1	100MF Electrolytic Capacitor	518D107M016AX7S	Sprague	C2
43)	1	Ferrite Bead inductor	TDKBC50-1206	TDK	FB2
44)	6	NYLON Slotted Round Head Machine Screw Thread 6-32 Length 3/8"	112508	ASMCO	ZM1-6
45)	6	Nylon Threaded Spacer, Thread 6-32 Length ½"	1530 H – N -.500 - 1	ASMCO	ZM1-6
Lab Bench Power Supply Cable					
46)	1	12" Hookup wire for power supply Red	M16878/5-BGE-2	Anixter	
47)	1	12" Hookup wire for power supply Black	M16878/5BGE-0	Anixter	
48)	2	Plastic tiedowns 3-3/4"	4200	ASMCO	
Wall Power Supply					
49)	1	Switching Power Supply	DSA-0301-05	DVE	

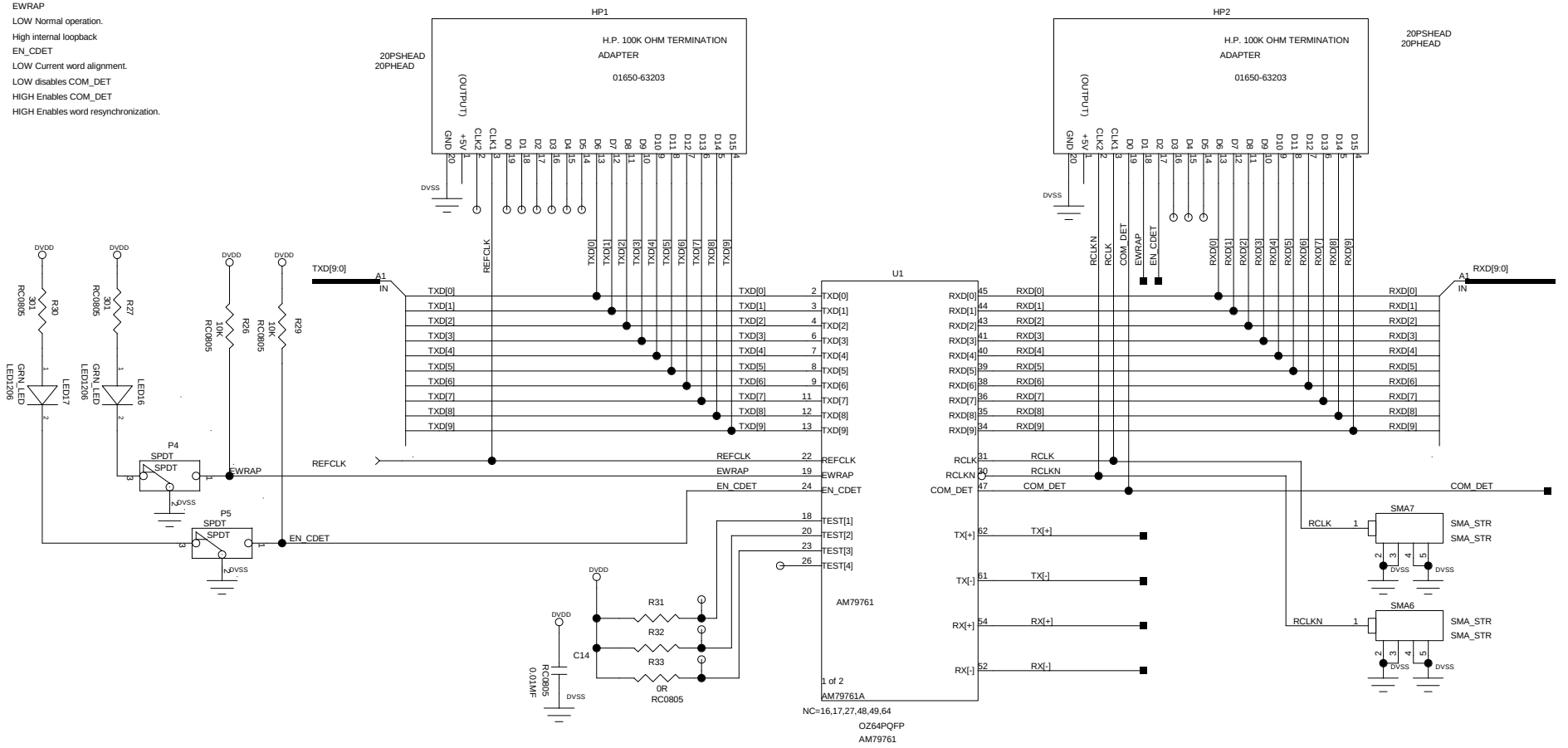


SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE				
MODULE	SHEET	SIZE	DWG. NO.	BRD. NO.	REV
GPHYSD_1B	1	D	GPHYSD_1B	GPHYSD_1B	B
DRAWN BY	ENGINEER	DATE		PAGE	
Steve Cooper	Robert Hartman	10-23-1997_14:48		1 of 7	

EWRAP
LOW Normal operation.
High internal loopback
EN_CDET
LOW Current word alignment.
LOW disables COM_DET
HIGH Enables COM_DET
HIGH Enables word resynchronization.



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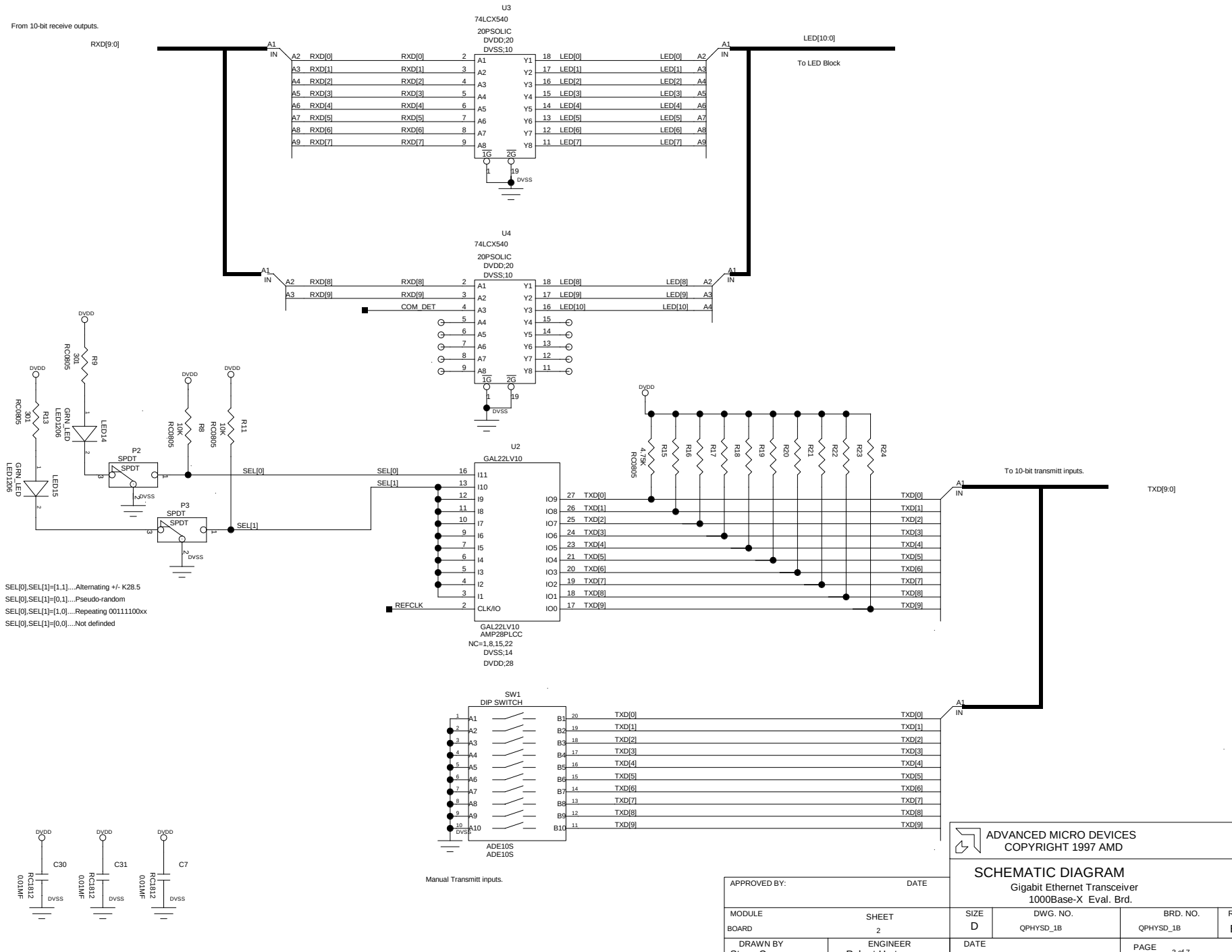
SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE			
MODULE: GIGABIT	SHEET: 1	SIZE: D	DWG. NO.: QPHYSD_1B	BRD. NO.: QPHYSD_1B / REV: B
DRAWN BY: Steve Cooper	ENGINEER: Robert Hartman	DATE: 10-21-1997_9:52	PAGE: 2 of 7	



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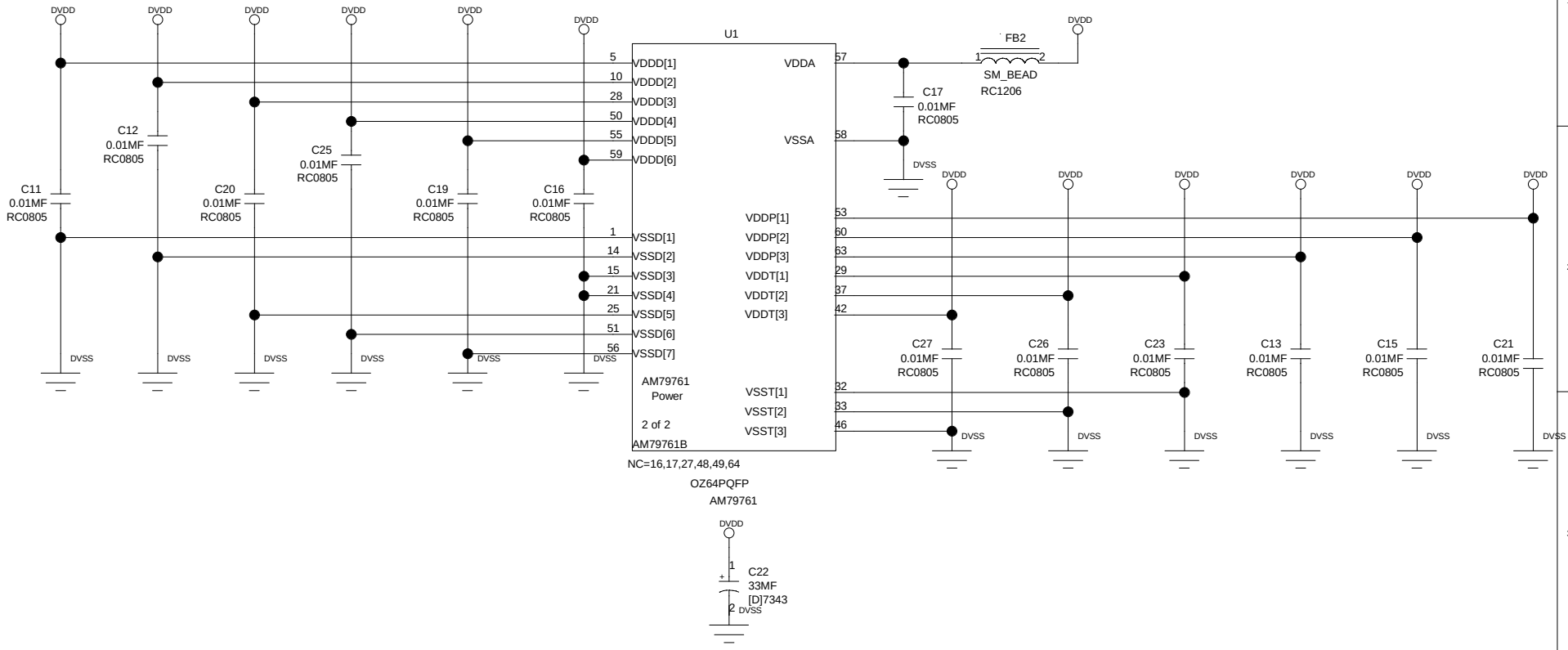
SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE			
MODULE	SHEET	SIZE	DWG. NO.	BRD. NO. / REV
BOARD	2	D	QPHYSD_1B	QPHYSD_1B / B
DRAWN BY: Steve Cooper	ENGINEER: Robert Hartman	DATE: 10-15-1997_13:36		PAGE: 3 of 7



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SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE				
MODULE / BOARD	SHEET	SIZE	DWG. NO.	BRD. NO.	REV
	3	D	GPHYSD_1B	GPHYSD_1B	B
DRAWN BY	ENGINEER	DATE		PAGE	
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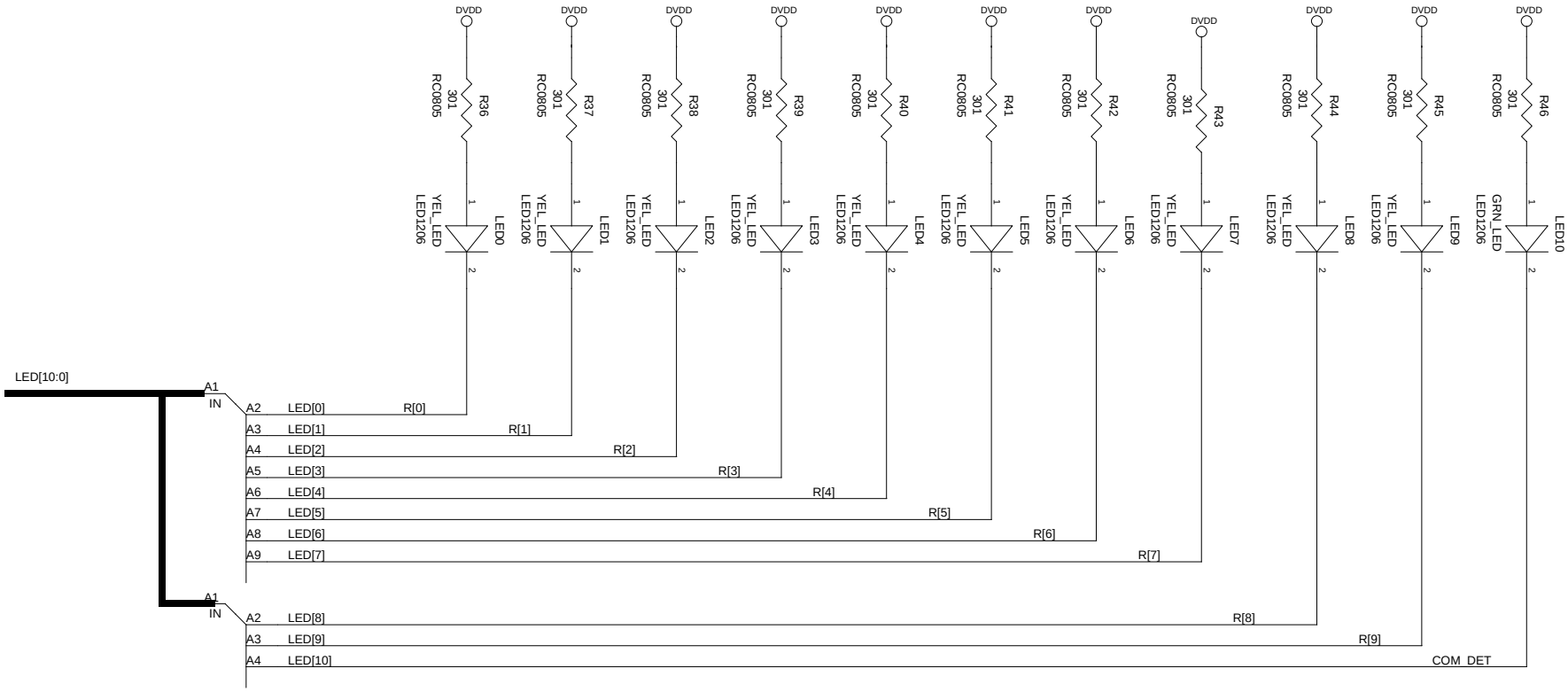

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SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE				
MODULE	SHEET	SIZE	DWG. NO.	BRD. NO.	REV
LEDS	1	D	GPHYSD_1B	GPHYSD_1B	B
DRAWN BY	ENGINEER	DATE		PAGE	
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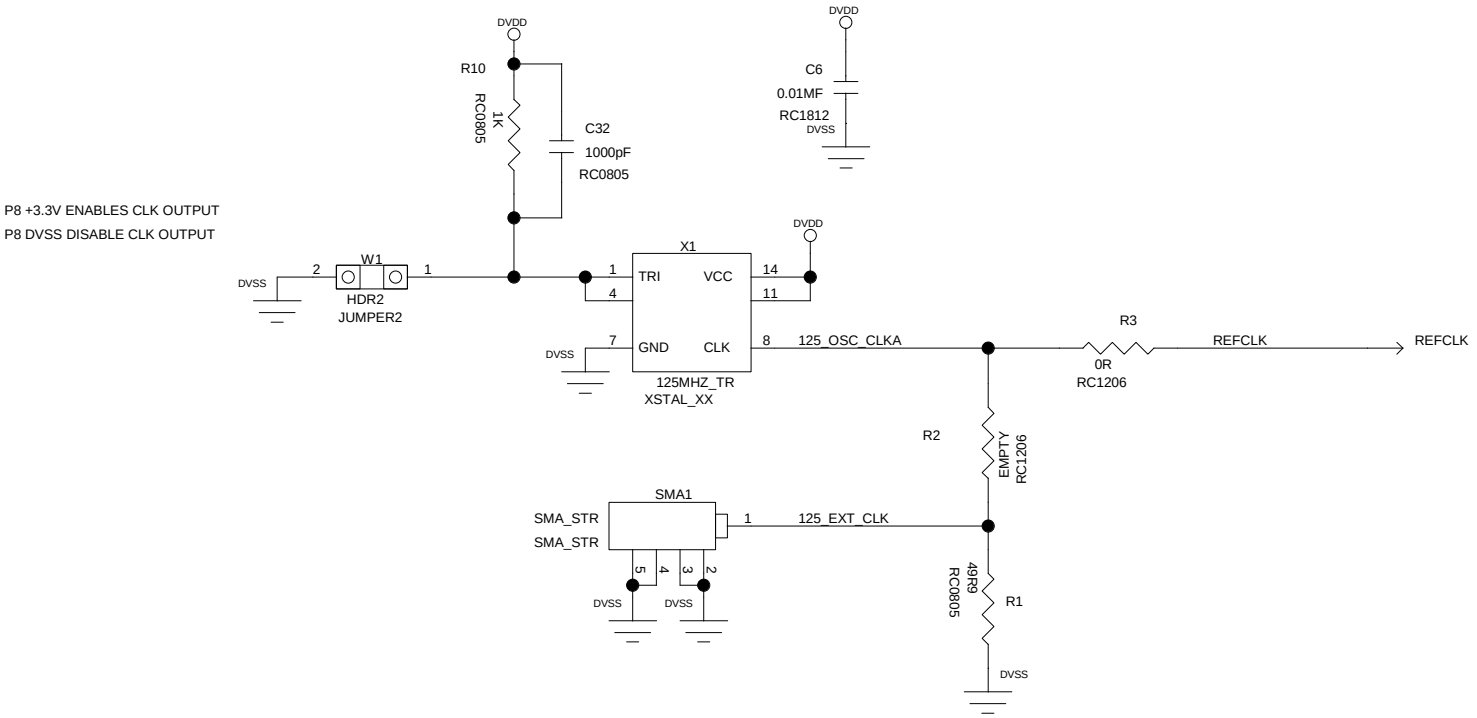

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SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE				
MODULE	SHEET	SIZE	DWG. NO.	BRD. NO.	REV
SYSCLK	1	D	GPHYSD_1B	GPHYSD_1B	B
DRAWN BY	ENGINEER	DATE		PAGE	
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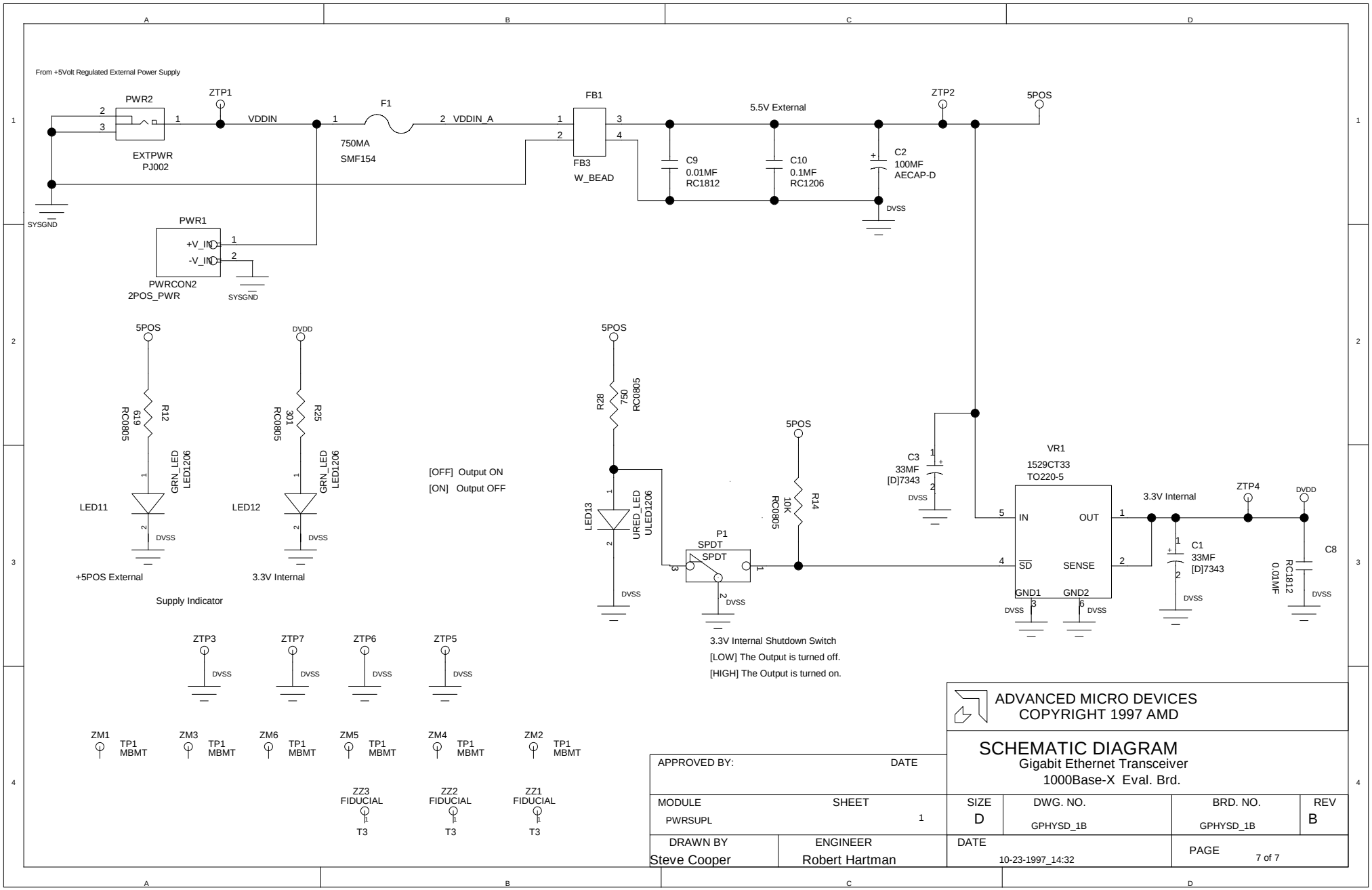

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SCHEMATIC DIAGRAM

Gigabit Ethernet Transceiver
1000Base-X Eval. Brd.

APPROVED BY:	DATE				
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PWRSUPL	1	D	GPHYSD_1B	GPHYSD_1B	B
DRAWN BY	ENGINEER	DATE		PAGE	
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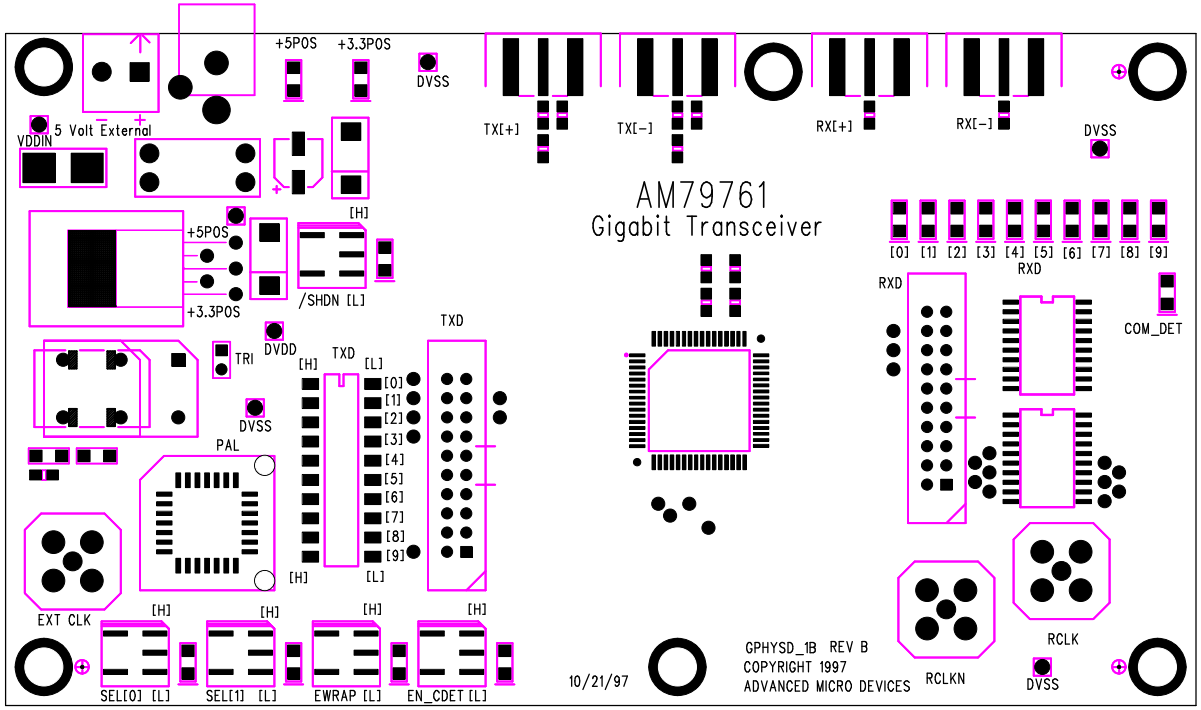

LAYER 1 TOP ROUTING

SILKSCREEN TOP

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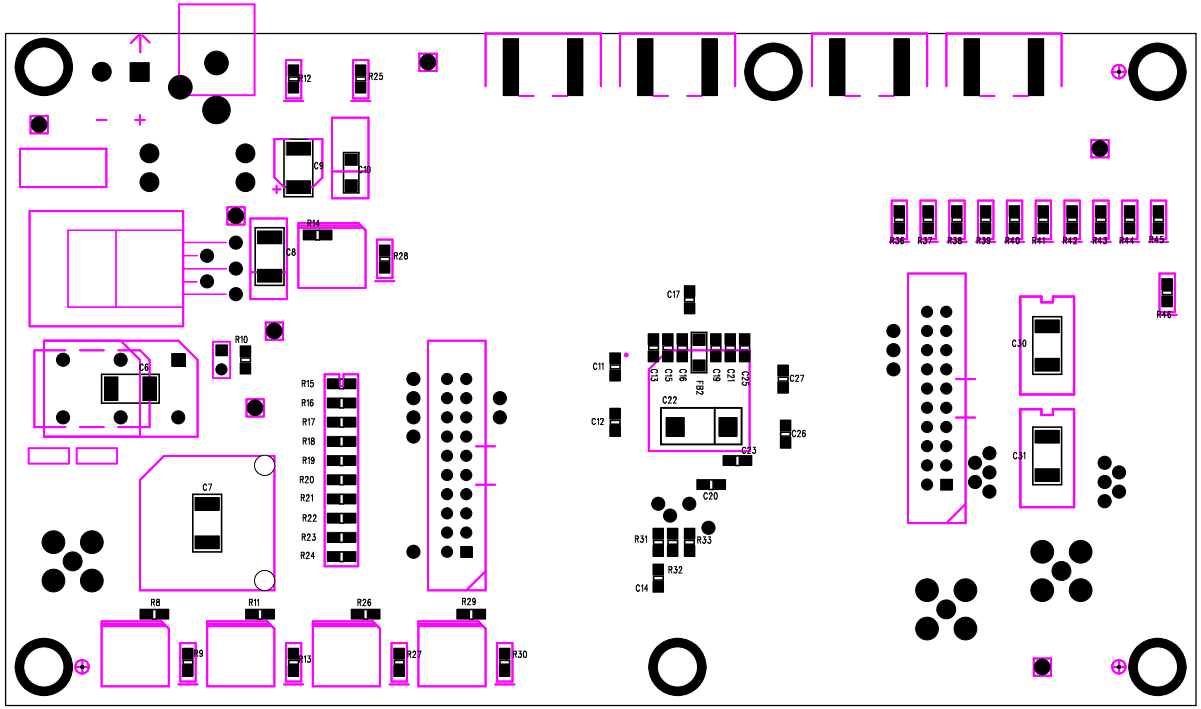
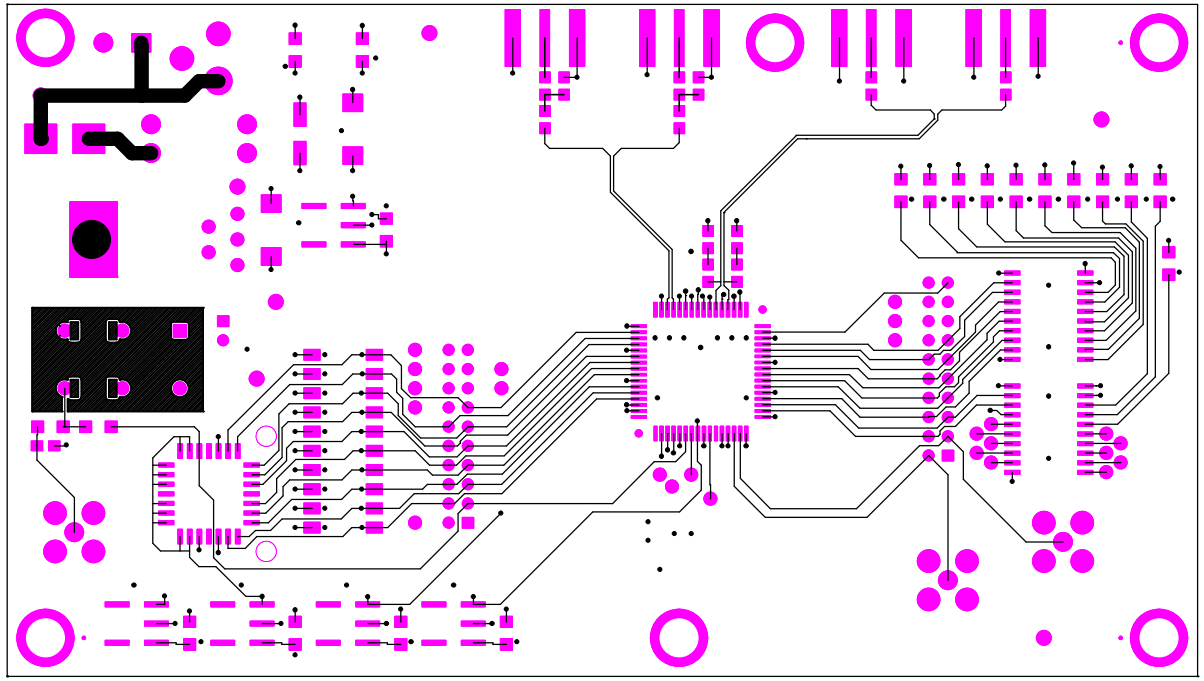
GPHYSD_1B REV B 10/21/97
Gigabit Ethernet Transceiver



SILKSCREEN BOTTOM

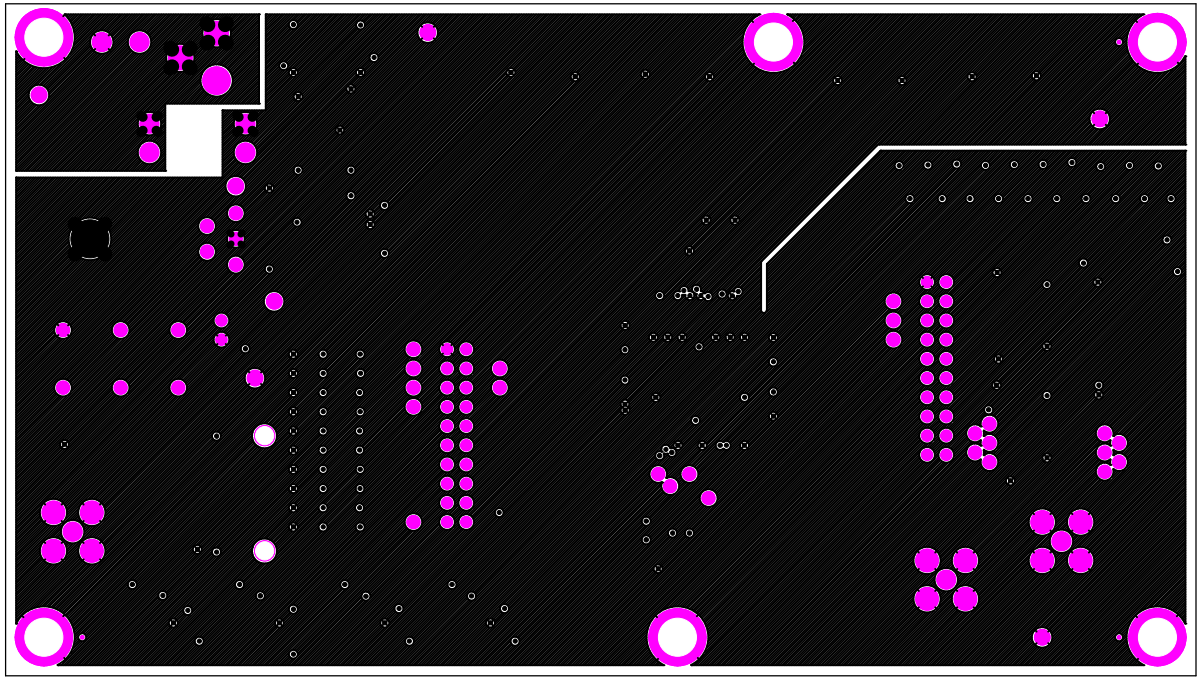
LAYER 4 BOTTOM ROUTING

GPHYSD_1B REV B 10/21/97
Gigabit Ethernet Transceiver



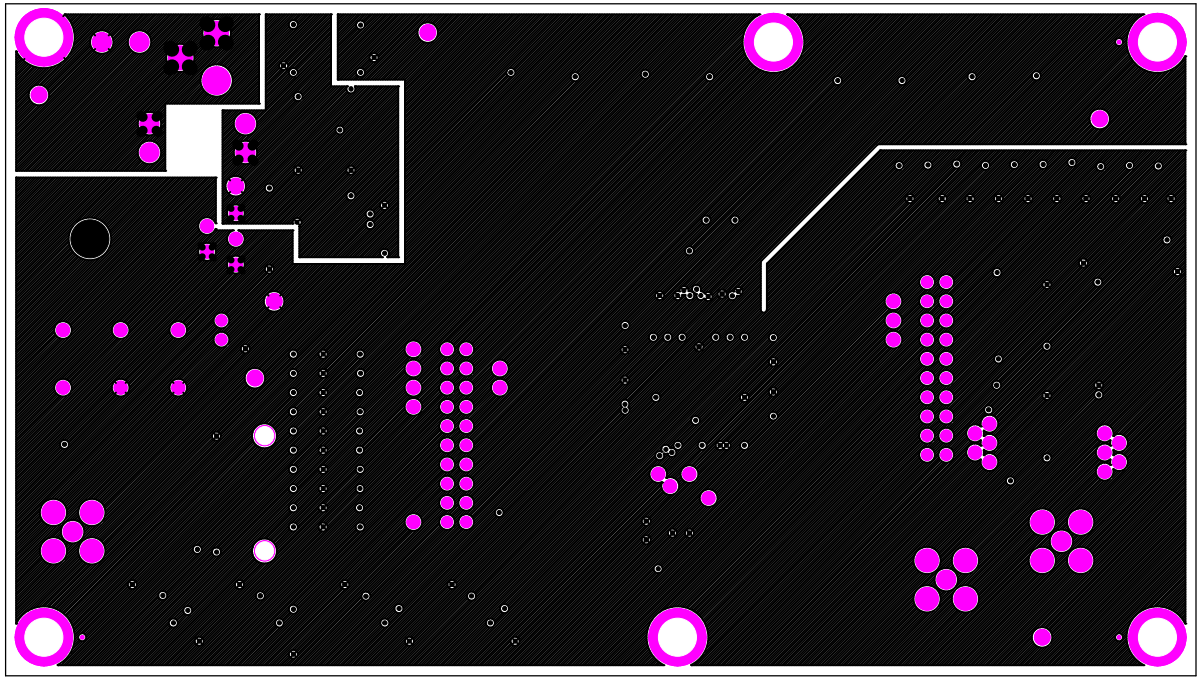
LAYER 1 TOP ROUTING

GPHYSD_1B REV B 10/21/97
Gigabit Ethernet Transceiver



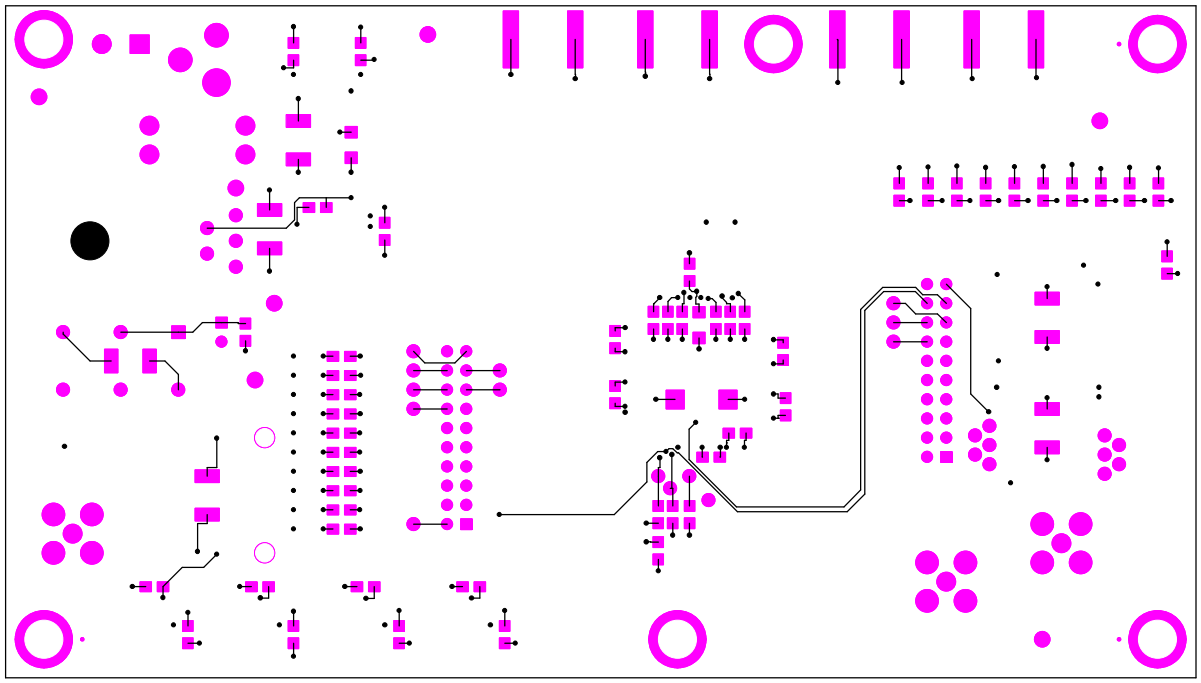
LAYER 2 INNER ROUTING DVSS

GPHYSD_1B REV B 10/21/97
Gigabit Ethernet Transceiver



LAYER 3 INNER ROUTING DVDD

GPHYSD_1B REV B 10/21/97
Gigabit Ethernet Transceiver



LAYER 4 BOTTOM ROUTING

GPHYSD_1B REV B 10/21/97
Gigabit Ethernet Transceiver