CYPRESS SEMICONDUCTOR

Reprogrammable 16K x 16 Registered PROM

Features

- 0.8-micron CMOS for optimum speed/power
- High speed
  - 20 ns max set-up
  - 12 ns clock to output
- 16-bit-wide words
- Registered outputs
- Three programmable input chip selects
- Synchronous or asynchronous chip selects
- Programmable output enable
- Initialization capability
  - Separate control pin ($\overline{INIT}$)
  - Programmable initialization word
- Programmable synchronous or asynchronous Init
- 44-pin PLCC and 44-pin LCC packages
- 100% reprogrammable in windowed packages
- TTL-compatible I/O
- Capable of withstanding greater than 2001V static discharge

Functional Description

The CY7C275 is a high-performance 16K-word by 16-bit CMOS PROM with output registers. It is available in a 44-pin PLCC and a 44-pin LCC, and is 100% reprogrammable in windowed packages. The memory cells utilize proven EPROM floating-gate technology and word-wide programming algorithms.

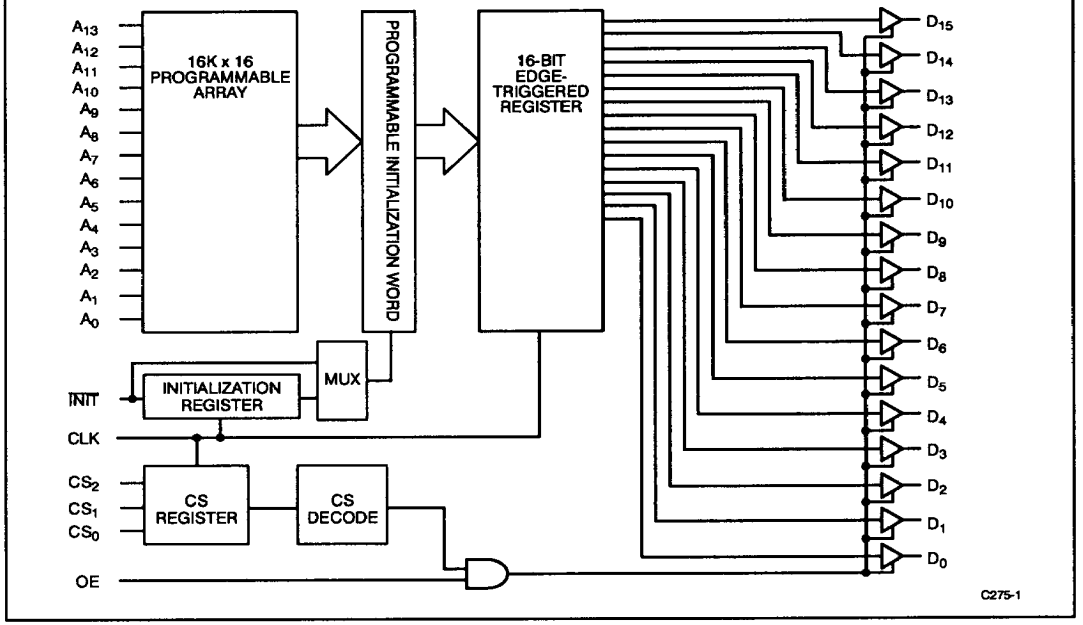
The CY7C275 features three independently programmable synchronous or asynchronous chip selects (CS_2 – CS_0) for on-chip address decoding of up to eight banks of PROMs. The active polarity of the output enable (OE) is also programmable.

In order to read the CY7C275, all three chip selects must be active and OE must be enabled. The data stored at the array location addressed by the address lines (A_{13} – A_0) is placed in the output register at the rising edge of CLK. The data will remain on the outputs until the following rising edge of CLK.

An initialization control input ($\overline{INIT}$) is provided. The initialization mode can be programmed to operate either synchronously or asynchronously. If the synchronous mode is being used, when $\overline{INIT}$ is LOW during the rising edge of CLK, a separate, programmable initialization word appears on the output at the next rising edge of CLK. The chip selects and output enable must be active when reading the initialization word.

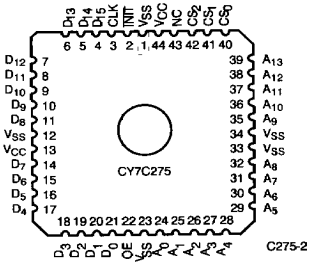
If the asynchronous initialize mode is being used, applying a LOW to $\overline{INIT}$ causes an immediate load of the programmable initialize word into the output registers and onto the outputs. The chip selects and output enable must be active when reading the initialization word. The asynchronous $\overline{INIT}$ LOW disables CLK and must return HIGH to re-enable CLK.

Logic Block Diagram



Pin Configurations

LCC, PLCC (Opaque Only)
Top View



C275-2

Selection Guide

		CY7C275–20	CY7C275–25	CY7C275–30
Maximum Set-Up Time (ns)		20	25	30
Maximum Clock to Output (ns)		12	15	18
Maximum Operating Current (mA)	Commercial	200	200	200
	Military		250	250

Shaded areas contain advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial[1]	– 40°C to +85°C	5V ±10%
Military[2]	– 55°C to +125°C	5V ±10%

Electrical Characteristics[3, 4]

Parameter	Description	Test Conditions		CY7C275–20 CY7C275–25 CY7C275–30 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA (6.0 mA Mil)			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	µA
V_{CD}	Input Clamp Diode Voltage			Note 3		
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		– 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[5]		– 20	– 90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0.0 mA	Com'l		200	mA
			Mil		250	

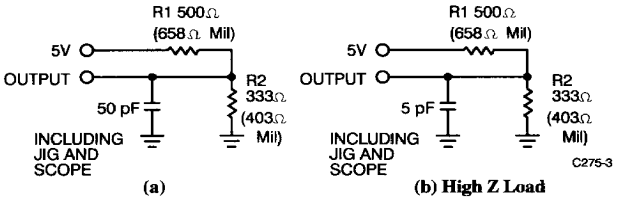
Notes:

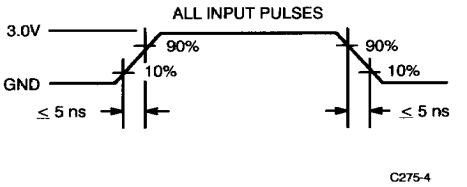
1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See Introduction to CMOS PROMs in this Data Book for general information on testing.
4. See the last page of this specification for Group A subgroup testing information.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Capacitance[3]

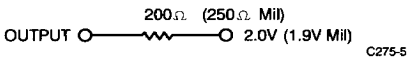
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT



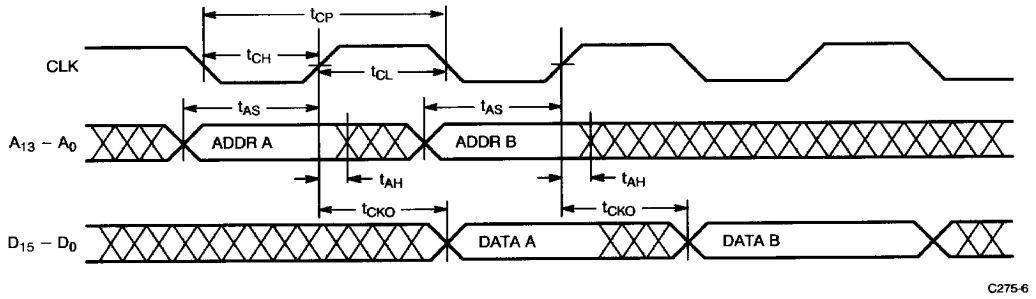
Switching Characteristics Over the Operating Range[3, 4]

Parameters	Description	CY7C275–20		CY7C275–25		CY7C275–30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	20		25		30		ns
t_{CH}	Clock HIGH Pulse Width	$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		ns
t_{CL}	Clock LOW Pulse Width	$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		$t_{CP}/2 - 2$		ns
t_{AS}	Address Valid to CLK Rise	20		25		30		ns
t_{AH}	Address Hold from CLK Rise	0		0		0		ns
t_{CKO}	Clock Rise to Output Data		12		15		18	ns
t_{CSS}	CS Set-Up to CLK Rise	4		4		5		ns
t_{CSH}	CS Hold from CLK Rise	3		4		4		ns
t_{COV}	Clock Rise to Output Valid		12		15		18	ns
t_{COZ}	Clock Rise to High Z Output		12		15		18	ns
t_{OEV}	OE Active to Output Valid		12		15		18	ns
t_{OEZ}	OE Inactive to High Z Output		12		15		18	ns
t_{IS}	$\overline{INIT}$ Set-Up to CLK Rise	20		25		30		ns
t_{IH}	$\overline{INIT}$ Hold from CLK Rise	0		0		0		ns
t_{IW}	Asynchronous Init Pulse Width	12		15		18		ns
t_{IDV}	Asynchronous Init to Data Valid		15		20		25	ns
t_{ICR}	Asynchronous Init Recovery to CLK	12		15		18		ns
t_{CSOV}	CS Active to Output Valid		15		18		21	ns
t_{CSOZ}	CS Inactive to High Z Output		15		18		21	ns

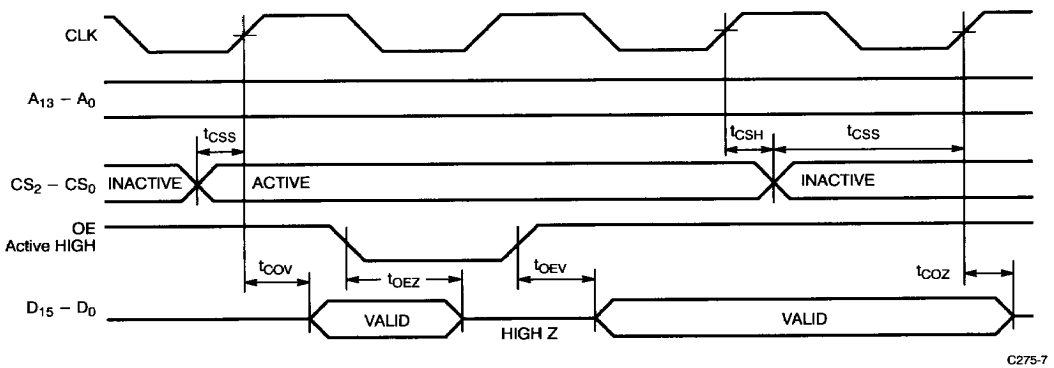
Shaded areas contain advanced information.

Switching Waveforms

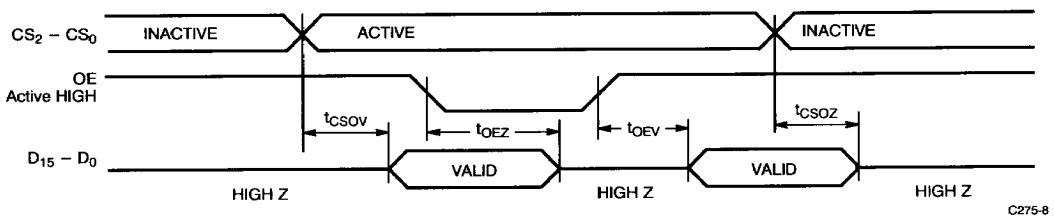
Read Operation[6]



Synchronous Chip Select and Output Enable



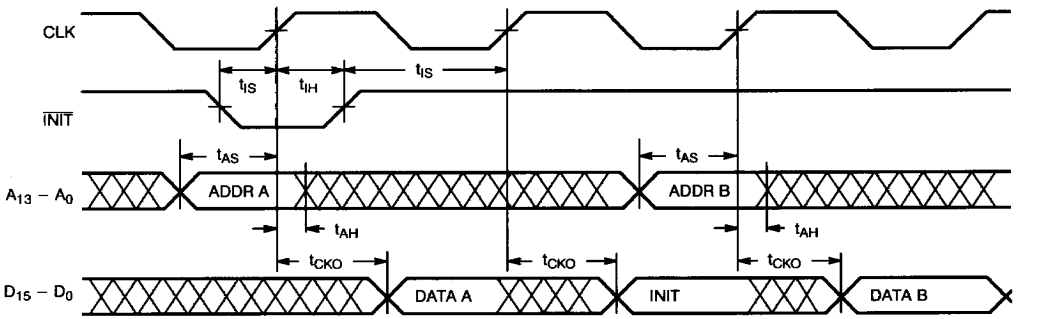
Asynchronous Chip Select and Output Enable



Notes:
6. $CS_2 - CS_0$, OE assumed active

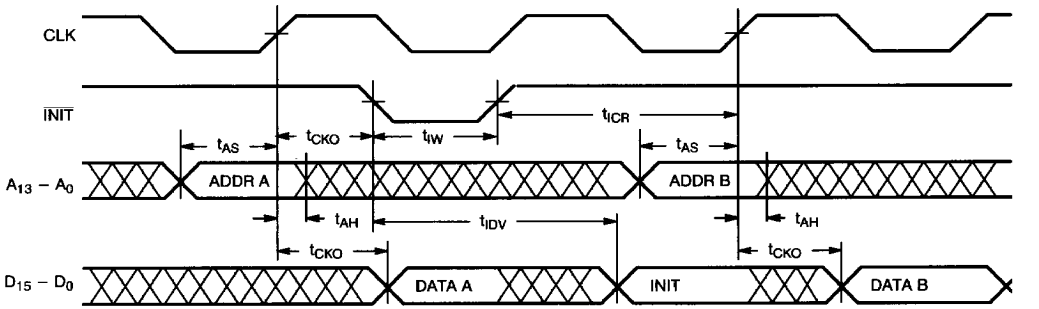
Switching Waveforms (continued)

Synchronous Initialization Timing Diagram[6]



C275-10

Asynchronous Initialization Timing Diagram[6]



C275-9

Architecture Configuration Bits

The CY7C275 has seven user-programmable options in addition to the reprogrammable data array. For detailed programming information, contact your local Cypress representative.

The first four programmable options determine the active polarity for the three chip selects (CS_2 – CS_0) and the active polarity of OE. When these control bits are programmed with a 0, the inputs are active LOW. When these control bits are programmed with a 1, the inputs are active HIGH. The fifth option determines the operation of the initialize function. When the control bit is programmed with a 0, initialize is synchronous. When the control bit is programmed with a 1, initialize is asynchronous. The sixth option determines the operation of the chip selects. When the control bit is programmed with a 0, the chip selects are synchronous. When the control bit is programmed 1, the chip selects are asynchronous. The initialization word is also user-programmable.

Control Option	Control Word Bit	Control Word Programmed Level	Function
OE	D_0	0 1	OE Active LOW OE Active HIGH
AE	D_3	0 1	Synchronous CS_{0-2} Asynchronous CS_{0-2}
CS_0	D_{12}	0 1	CS_0 Active LOW CS_0 Active HIGH
CS_1	D_{13}	0 1	CS_1 Active LOW CS_1 Active HIGH
CS_2	D_{14}	0 1	CS_2 Active LOW CS_2 Active HIGH
IA	D_{15}	0 1	INIT Synchronous INIT Asynchronous

Bit Map

Programmer Address (Hex)	RAM Data
0000	Data
.	.
.	.
.	.
3FFF	Data
4000	Control Word
4001	Initialization Word

Control Word (4000H)

D_{15} D_0

IA CS_2 CS_1 CS_0 X X X X X X X X X AE X X OE

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C275 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 35 minutes. The 7C275 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Program Mode Table

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	D_0 – D_{15}
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	High Z
Program Enable	V_{PP}	V_{ILP}	V_{IHP}	Data
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	Data

Table 2. Signature Mode Table

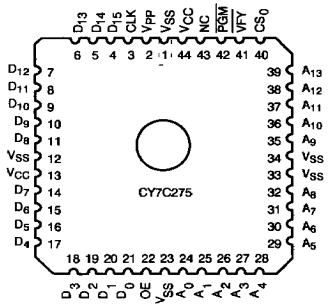
Signature Mode	A_0	A_9	D_0 – D_{15}
Cypress Code	V_{ILP}	V_{PP}	0034 (hex)
Device Code	V_{IHP}	V_{PP}	0014 (hex)

Table 3. Configuration Mode Table[7]

Mode	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_2	A_4	D_0 – D_{15}
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	X	X	High Z
Program Control Word	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Control Word
Verify Control Word	V_{PP}	V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Control Word
Program Init Word	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	Init Word
Verify Init Word	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	Init Word

Notes:

7. X = "don't care" but not to exceed V_{CC} ±5%.



C275-11

Figure 1. Programming Pinout

Ordering Information[8]

Speed (ns)		Ordering Code	Package Type	Operating Range
t_{AS}	t_{CKO}			
20	12	CY7C275–20HC	H67	Commercial
		CY7C275–20JC	J67	
25	15	CY7C275–25HC	H67	Commercial
		CY7C275–25JC	J67	
		CY7C275–25HMB	H67	Military
		CY7C275–25LMB	L67	
		CY7C275–25QMB	Q67	
30	18	CY7C275–30HC	H67	Commercial
		CY7C275–30JC	J67	
		CY7C275–30HMB	H67	Military
		CY7C275–30LMB	L67	
		CY7C275–30QMB	Q67	

Shaded areas contain advanced information.

Notes:

8. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7, 8, 9, 10, 11
t_{AH}	7, 8, 9, 10, 11
t_{CKO}	7, 8, 9, 10, 11
t_{CSS}	7, 8, 9, 10, 11
t_{CSH}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{IW}	7, 8, 9, 10, 11
t_{IDV}	7, 8, 9, 10, 11
t_{ICR}	7, 8, 9, 10, 11

Document #: 38–00181–A