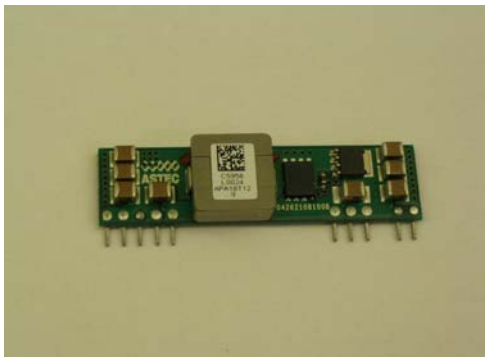
Technical Reference Note
APA18T12 DC - DC Series
Preliminary

APA18T12 - 12Vin, 75Watts, Non-isolated DC – DC POL SIP Converter

The single output APA18T12 is a non-isolated, 75W, SIP footprint Point-of-Load (POL) DC/DC converter. The new APA18T12 series can deliver an adjustable output voltage range from 0.75V – 5.5V at 18 Amps (A) with efficiency as high as 93.5%, and the input voltage range is from 10 – 14V.



Special Features

- **Point of Load (POL) applications**
- **High current slew rate at 1A/uS**
- **Industry standard footprint**
- **Open frame SIP**
- **-40°C to +85°C Ambient operating temperature**
- **Positive enable function**
- **Low output ripple and noise**
- **Adjustable output voltage through external resistor programming**
- **Regulation to zero load**

Safety

UL, cUL	**60950 Recognized**
TUV	**EN60950 Licensed**

Electrical Parameters

Input	
Input range	**10 to 14 VDC**
Input Surge	**15V**
Efficiency	**92%@3.3Vo (Typical)**
Output	
Line Regulation	**< 0.5%**
Load Regulation	
0.75Vo	**7mV**
0.75 < Vo < 3.3V	**15mV**
3.3V ≤ Vo	**25mV**
Regulation Over operating Temperature range	**< 1.0%**
Noise / Ripple	
0.75 – 5Vo	**60mV**
> 5Vo	**75mV**
Enable	**TTL compatible**
Transient Response	**200mV typical deviation For load change of 50% step Between 10% to 100% of load 200uS(max) recovery**
Remote Sense	**0.25V**
Turn on input voltage	**8.7 – 9.7V (Typ)**
OCP/OTP	**Hiccup – auto recovery**

APA18T12 SERIES

THIS TECHNICAL REFERENCE NOTES COVERS THE SPECIFICATIONS FOR A SINGLE OUTPUT, OPEN-FRAME, NON-ISOLATED DC-DC CONVERTER WITH ADJUSTABLE OUTPUT FROM 0.75V TO 5.5V HAVING 75W MAXIMUM OUTPUT POWER WHEN OPERATED FROM A NOMINAL 12 VDC SOURCE.

MODEL NUMBER	SIS CODE	Vin range	Vout/Iout	MODEL ID NO
APA18T12-9	APA18T12-9	10V – 14V	0.75 – 5.50V/ 18A*	C595
APA18T12-9H	APA18T12-9H	10V – 14V	0.75 – 5.50V/ 18A*	C596

*Options:

Suffix	Option
-9	Vo Trim, Vertical Mounting Pin
-9H	Vo Trim, Horizontal Mounting Pin

Note: * - 18A maximum output current with total power limited to 75W. Factory default output voltage set to 0.75V.

Electrical Specifications

The product shall comply with the requirements of this specification for all valid conditions of line input voltage, load current, temperature and other environmental conditions, unless otherwise specified in this document.

Description	
External Input Fuse[1,2]	Fast-acting 20A maximum
External Input Capacitance	22uF/16V*3 Ceramic Cap.
External Output Capacitance	10uF Tantalum Cap. +1uF Ceramic Cap.
$+V_{IN}$	+10Vdc to 14Vdc
Enable	Open
GND	Return for both V_{IN} and V_O
Trim	Resistor Programming [See App A6]
+Vout	Output Pin connected to Load
Airflow[3]	200LFM/300LFM
T_A (Ambient Temperature)	-40ºC to 85ºC

NOTE: 1. Refer to Appendix A4 for typical application circuit.
2. The converter is not internally fused; Engineering needs to specify a fuse appropriate to the package size of the converter.
3. Refer to Appendix A1 for correct airflow and module orientation &Appendix B for the derating curves of different airflow.

ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. The converter shall be designed, labeled and safety approved for maximum continuous rating as follows:

Parameter	Device	Symbol	Min	Typ	Max	Unit
Input Voltage Continuous Transient (100ms)	All	 V_{IN} $V_{IN, trans}$	 -0.3 -	 - -	 15 18	Vdc
Operating Temperature	All	Ta	-40	-	85	ºC
Storage Temperature	All	T_{STG}	-55	-	125	ºC
Operating Humidity	All	-	10	-	85	%
Max Voltage at Enable Pin	All		-	-	14	Vdc
Max Output Power	All		-	-	75	W

INPUT SPECIFICATIONS

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range	All	V_{IN}	10.0	12.0	14.0	Vdc
Input Under-Voltage Lock-out T_ON Threshold T_OFF Threshold	All		 8.7 7.9	 - -	 9.7 8.7	Vdc
Input Current ($V_{IN} = V_{IN, Min}$; $I_O = I_{O, Max}$)	5.50V 0.75V	I_{IN-MAX}	- -		10.0 2.0	A
Max P_{diss} @ I_O = 0A ($V_{IN} = V_{IN, Nom}$)	5.50V 0.75V		- -	- -	5.5 5.0	W
Input Ripple Current[1] 5Hz to 20MHz	All	I_{I1}	-	-	300	mAp-p
Input Voltage Rise Time 10% to 90% of Vout	All		NA	-	-	V/ms
Inrush Current dV_{IN}/dt	All		NA	-	-	Apk

NOTE: 1. External input capacitance required. See Input Ripple Current test measurement setup on Appendix A2.

OUTPUT SPECIFICATIONS

Parameter	Device	Symb	Min	Typ	Max	Unit
Output Voltage Set point $V_{IN} = V_{IN,\ MIN}$ to $V_{IN,MAX;}$ $I_O = I_{O,Max}$		$V_{O,SET}$	0.74	0.75	0.76	Vdc
Output Regulation Line: $V_{IN} = V_{IN,\ min}$ to $V_{IN,\ max}$ Load: $I_O = I_{O,\ min}$ to $I_{O,\ max}$ Temp: T_A = -40 ºC to +85ºC	All 0.75V 0.75<Vo<3.3V 3.3V≤Vo All	- - - -	- - - -	- - - -	0.5 7.0 15.0 25.0 1.0	% mV mV mV %
Ripple and Noise[2] Peak-to-Peak: (5Hz to 20MHz)	0.75≤Vo<5.0V 5V≤Vo	- -	- -	45 55	60 75	mVp-p mVp-p
Output Current and output power[3]	0.75≤Vo<4.16V 4.16V≤Vo	Io Po	0 0	- -	18 75	A W
External Load Capacitance Capacitor ESR	All	-	- 10	- -	5000 -	µF mΩ
Output Current-limit Inception V_{OUT} = 90% $V_{O,SET}$[4,9,10]	1.5V≤Vo	I_O	18.5	-	-	A
Over Temperature Range[6] (AVG. PCB TEMP)	All	-	100	110	125	°C
Efficiency $V_{IN} = V_{IN-NOM}$ $I_O = I_{O,MAX}$; T_A=25°C	0.75V 1.20V 1.50V 1.80V 2.50V 3.30V 5.00V	η η η η η η η	73.6 81.0 83.8 85.5 88.0 90.3 92.6	74.8 82.0 84.5 86.5 89.0 92.4 93.5		% % % % % % %
Turn-On Response Time[5] $V_{IN} = V_{IN-MIN}$ to V_{IN-MAX}	All	-	2.0	-	6.0	ms
Enable to Output Turn-ON Delay $V_{IN} = V_{IN-MIN}$ to V_{IN-MAX} $I_O = I_{O,MIN}$ to $I_{O,MAX}$	All	-	-	-	20.0	ms
+V_{IN} to Output Turn-On Delay Enable Pin: Active $V_{IN} = V_{IN-MIN}$ to V_{IN-MAX} $I_O = I_{O,MIN}$ to $I_{O,MAX}$	All	-	-	-	20.0	ms
Switching Frequency	All	-	270	300	330	KHz
Output Overshoot at T-on / T-off Passive Resistive Full Load	All	-	-	-	5	%Vo

OUTPUT SPECIFICATIONS

Parameter	Device	Symbol	Min	Typ	Max	Unit
Dynamic Response[6]: C_O=150uF*2 Polymer Cap. (Sanyo OS-CON 6SEP150) +10uF Tantalum Cap. +1uF Ceramic Cap. $\Delta I_O/\Delta t$=1.0A/µs Peak Deviation Load Change of 50% step anywhere between 10% to 100% of rated load	All	-	-	-	200	mV
Settling Time (to 0.5% $V_{O, Nom}$)	All	-	-	-	200	µs
Output Voltage Trim Range[7]	All		0.75	-	5.50	V
Remote Sense[8]	All			-	0.25	V
Output Enable ON/OFF Positive Enable Enable Pin Voltage: Mod-ON Mod-OFF	All	 - -	 2.5 -0.7	 - -	 14 0.8	 V V

NOTE: 2. Refer to Appendix A3 for the Output Ripple and Noise Test Measurement Setup.
3. Output Power Derating applies at elevated temperature. See Appendix B for the Derating Curves.
4. OCP and OTP are in shutdown mode. The converter will auto restart without the need to recycle the input voltage or toggle the enable signal and once the fault is removed.
5. Measure output rise time from 10%V_O to 90%V_O. See Appendix A5.
6. Load step response shall be measured at the load side of the output capacitors. See Appendix A4 for the output and input cap requirement.
7. See appropriate Trim Equation and configuration in Appendix A6.
8. The combination of remote sense and output trim adjust can not exceed 0.25V.
9. No OCP for Vo<1.5V. Module is protected by OTP when output is overload if Vo<1.5V.
10. Under 25°C.

APPENDIX A1: CONVERTER ORIENTATION WRT TO AIRFLOW

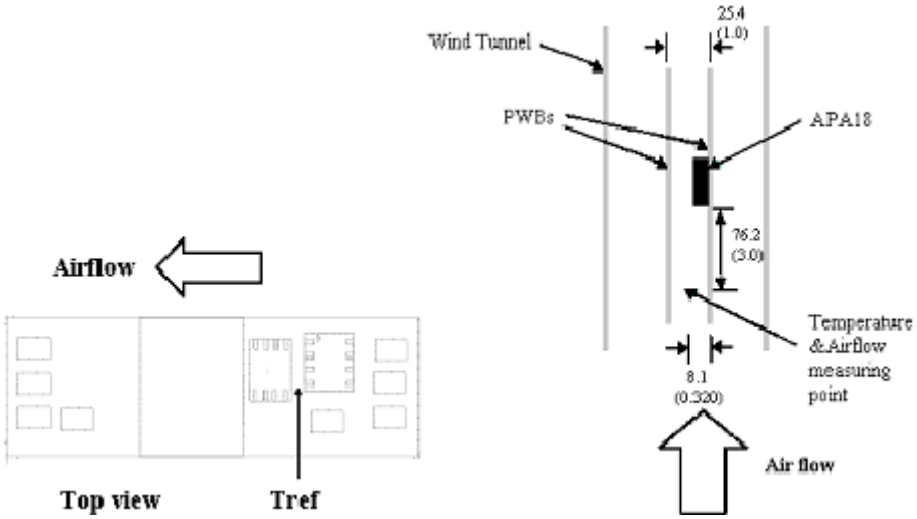
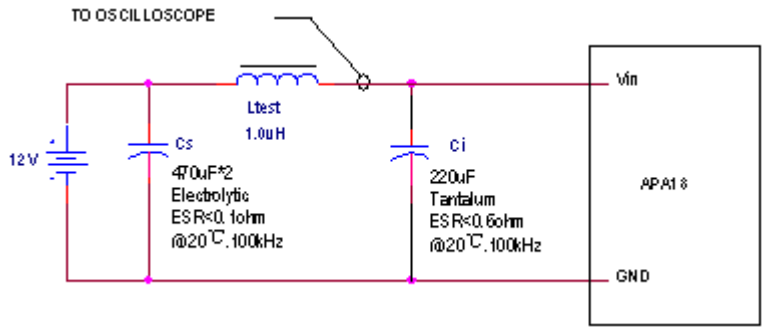


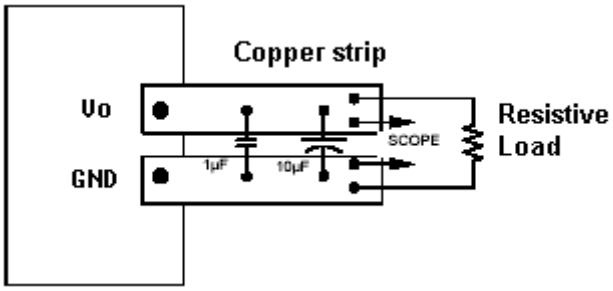
Figure 1. Airflow Orientation and Thermal Test Setup

APPENDIX A2: INPUT REFLECTED RIPPLE TEST SETUP



Note: Measure input reflected-ripple current with a simulated source inductance (Ltest) of 1uH. Capacitor Cs offsets possible battery impedance. Measure current as shown above.
Figure 2. Input Reflected-ripple current Test Setup.

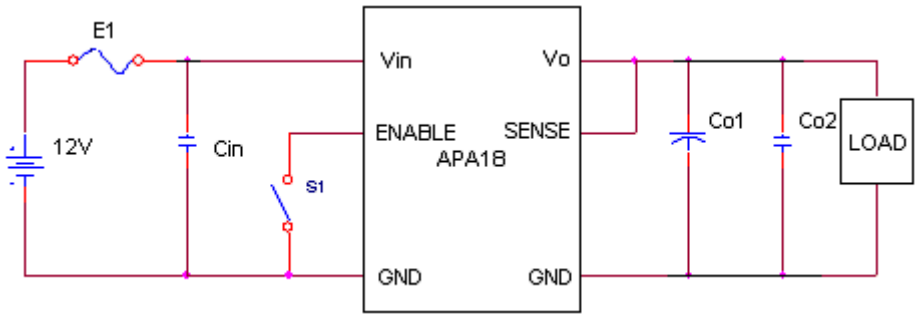
APPENDIX A3: OUTPUT RIPPLE TEST SETUP



Note: Use a 1µF@10V X7R ceramic capacitor and a 10µF @ 25V tantalum capacitor. Scope measurement should be made using a BNC socket. Position the load between 51 mm and 76 mm (2 in. and 3 in.) from module.

Figure 3. Peak-to-Peak Output Noise Measurement Test Setup.

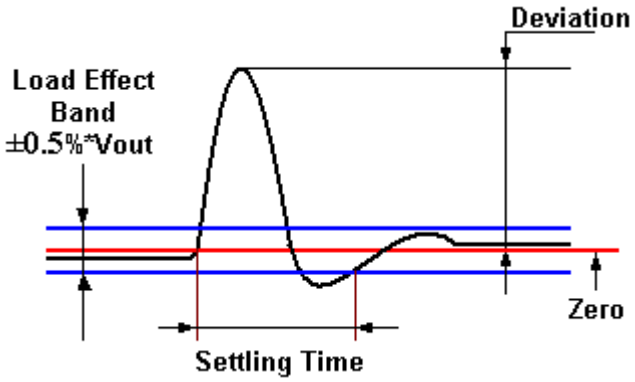
APPENDIX A4: TYPICAL APPLICATION CIRCUIT



Note:

F1: Fuse: Use external fuse (Fast-acting type 20A) for each unit.
Cin: Recommended 22uF/16V*3 ceramic capacitor.
Co1: Recommended 10uF/25V Tantalum capacitor.
Co2: Recommended 1uF/10V ceramic capacitor.

Figure 4.Typical Application Circuit



Note: When measuring dynamic deviation and settling time, 2*150uF Sanyo OS-Con 6SEP150 Polymer external output capacitors are needed.

Figure 5. Dynamic deviation and settling time

APPENDIX A5: TIMING DIAGRAM

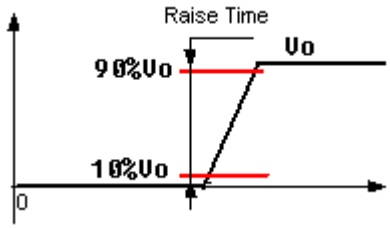


Figure 6. Timing diagram

APPENDIX A6: OUTPUT TRIM REQUIREMENT

Output voltage adjustment is accomplished by connecting an external resistor between the Trim Pin and Ground Pin terminals. Resistance and Output voltage relationship is established by Equation 1. If Trim pin is left open – default $V_O = 0.75V$

TRIM-UP EQUATION: $$Rtrim = \frac{10500}{Vo - 0.75} - 1000$$

Where R_{trim} is the resistance value in ohms and V_O is the output voltage desired.

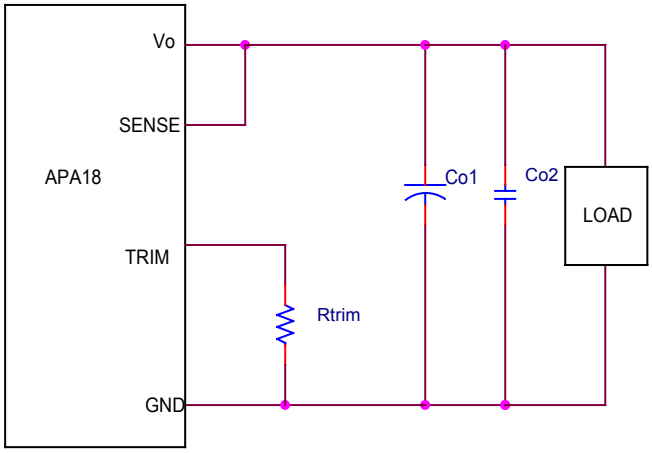


Figure 7. Trim UP test configuration (Pin Side Up)

$V_{O, set}$ (V)	*Rtrim* (K.)
0.75	Open
1.2	22.33
1.5	13.0
1.8	9.0
2.5	5.0
3.3	3.12
5.0	1.47

APPENDIX B: THERMAL DERATING:

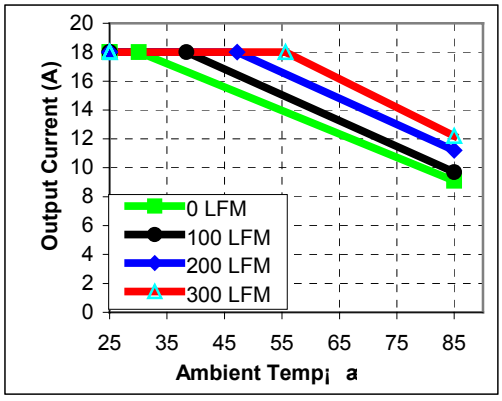


Figure 8: 0.75Vout@12Vin,Thermal Derating curve

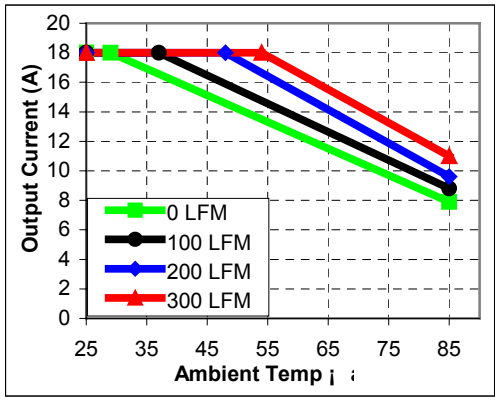


Figure 9: 1.2Vout@12Vin,Thermal Derating curve

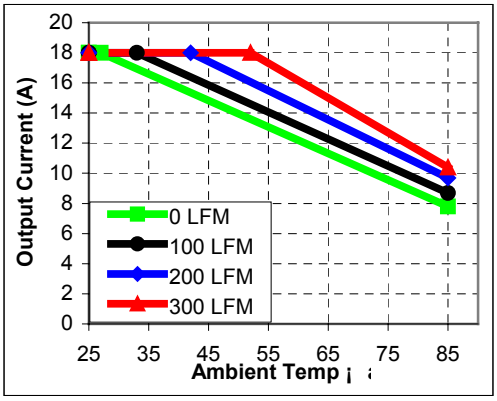


Figure 10: 1.5Vout@12Vin,Thermal Derating curve

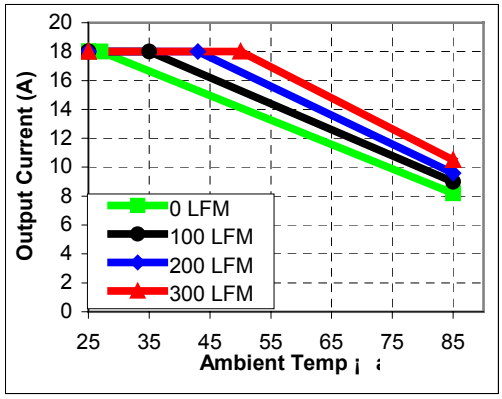


Figure 11: 1.8Vout@12Vin,Thermal Derating curve

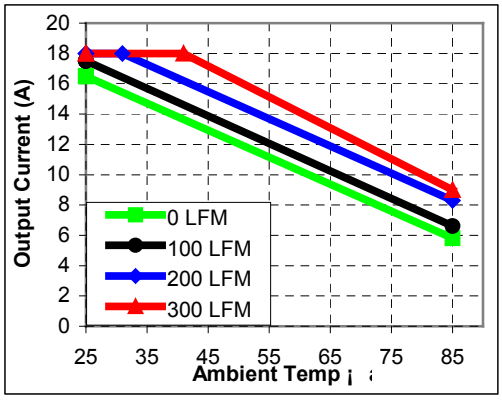


Figure 12: 2.5Vout@12Vin,Thermal Derating curve

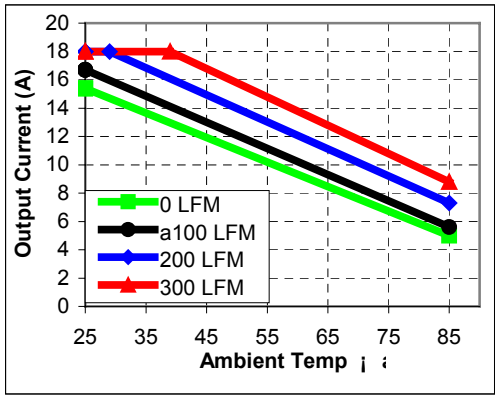


Figure 13: 3.3Vout@12Vin,Thermal Derating curve

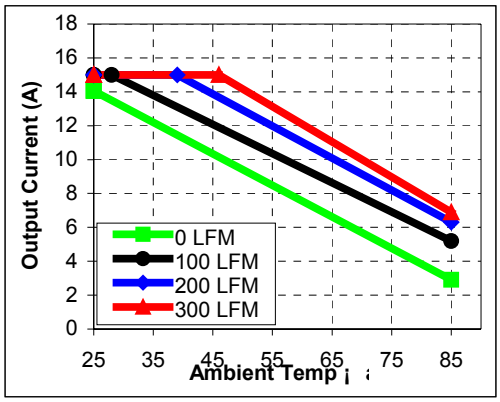


Figure 14: 5.0Vout@12Vin,Thermal Derating curve

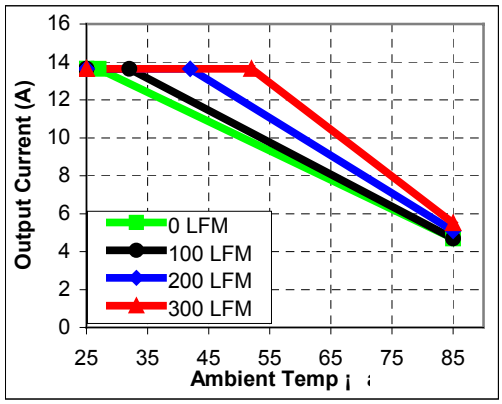


Figure 15: 5.5Vout@12Vin,Thermal Derating curve

APPENDIX C: MODULE PIN ASSIGNMENT

PIN #	DESIGNATION	PIN #	DESIGNATION
$+V_{IN}$	+ Input Voltage	V_O	+Output
Enable	ON/OFF	Trim	V_O Adjust
GND	Return for V_{IN} and V_O		
Sense	+Output Sense pin		

Note: The pinout assignment of APA18T12-9 and APA18T12-9H are the same.

APPENDIX D: MECHANICAL OUTLINE/DRAWING

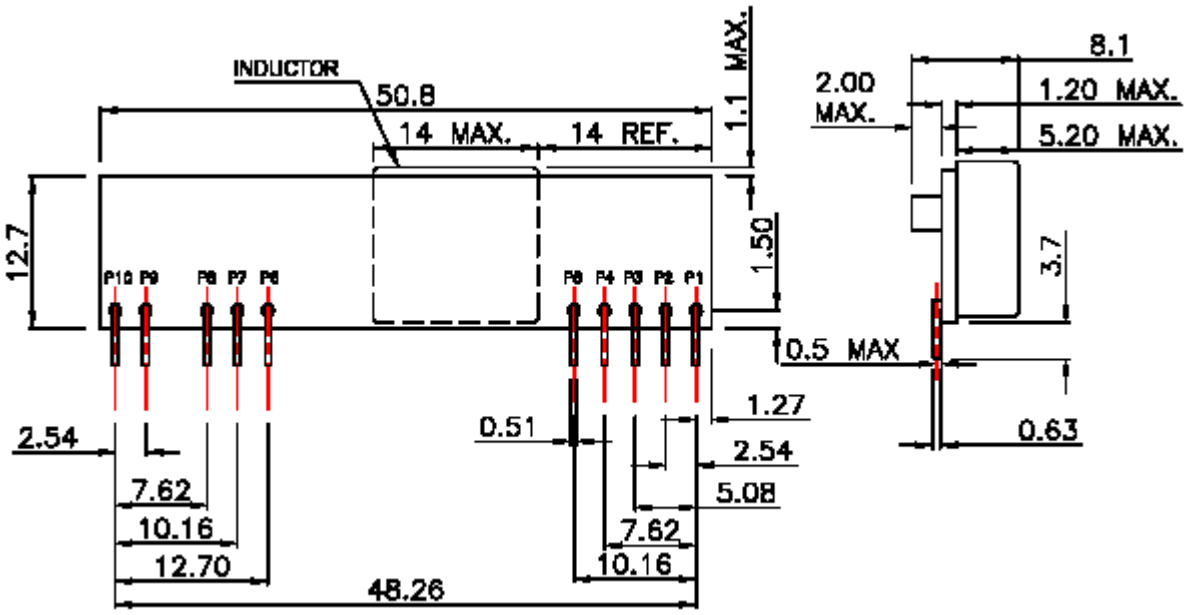


Figure 16. APA18 Mechanical Outline/ Drawing for Vertical type

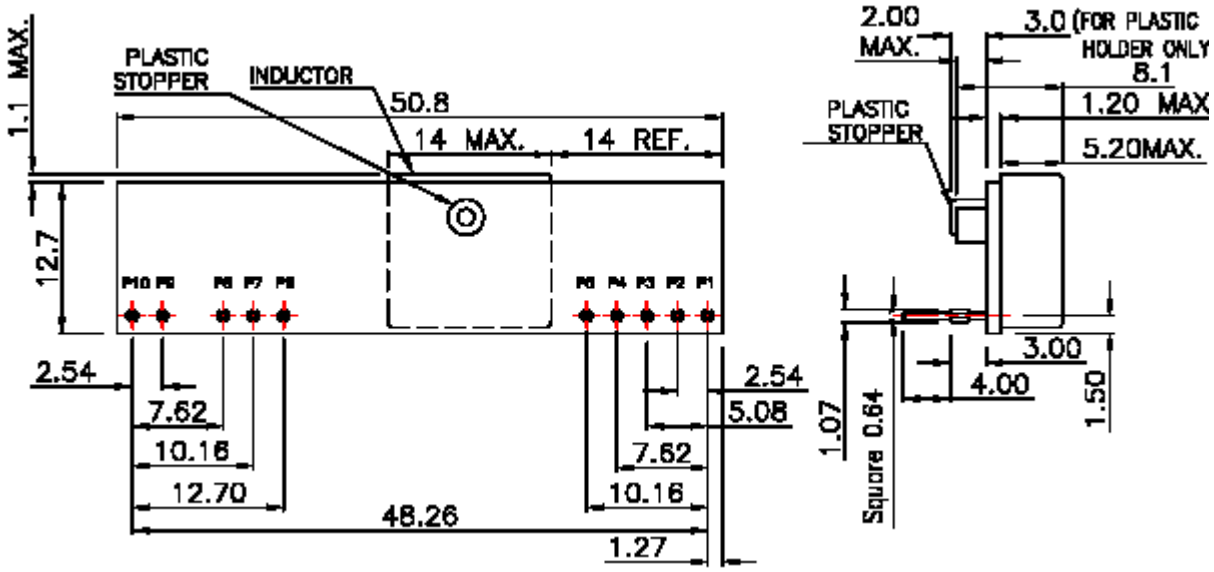


Figure 17. APA18 Mechanical Outline/ Drawing for Horizontal type

Pin Number	Pin Connection	Function
P1	Vo	Output Voltage
P2	Vo	Output Voltage
P3	SENSE	Sense
P4	Vo	Output Voltage
P5	GND	Ground
P6	GND	Ground
P7	Vin	Input Voltage
P8	Vin	Input Voltage
P9	TRIM	Output Voltage Adjustment
P10	ENABLE	Output Voltage Enable