DATA SHEET

Part No.	AN44067A
Package Code No.	HSOP034-P-0300A

Contents

AN44067A

Driver IC for stepping motor

■ Overview

AN44067A is s two channel H-bridge driver IC. Bipolar stepping motor can be controlled by a single driver IC.
2 phase excitation, half- step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation can be selected.

■ Features

- Built-in decoder for micro steps
  (2 phase excitation, half-step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation)
  Stepping motor can be driven by only external clock signal.
- PMW can be driven by built-in CR (3-value can be selected during PWM OFF period.)
  Selection during PWM OFF period enables the best PWM drive.
- Mix decay compatible (4-value for fast decay ratio can be selected.)
  Mix decay control can improve accuracy of motor current wave form.
- Built -in low voltage detection
  If supply voltage lowers less than the range of operating supply voltage, low voltage detection operates and all phases of motor drive output are turned OFF.
- Built-in thermal protection
  If chip junction temperature rises and reaches setup temperature, all phases of motor drive output are turned OFF.
- 1 power supply with built-in 5 V power supply (accuracy ±5%)
  Motor can be driven by only 1 power supply because of built-in 5 V power supply.
- Built-in standby function
  Operation of standby function can lower current consumption of IC.
- Built-in Home position function
  Home position function can detect the position of a motor.

■ Applications

- IC for stepping motor drives

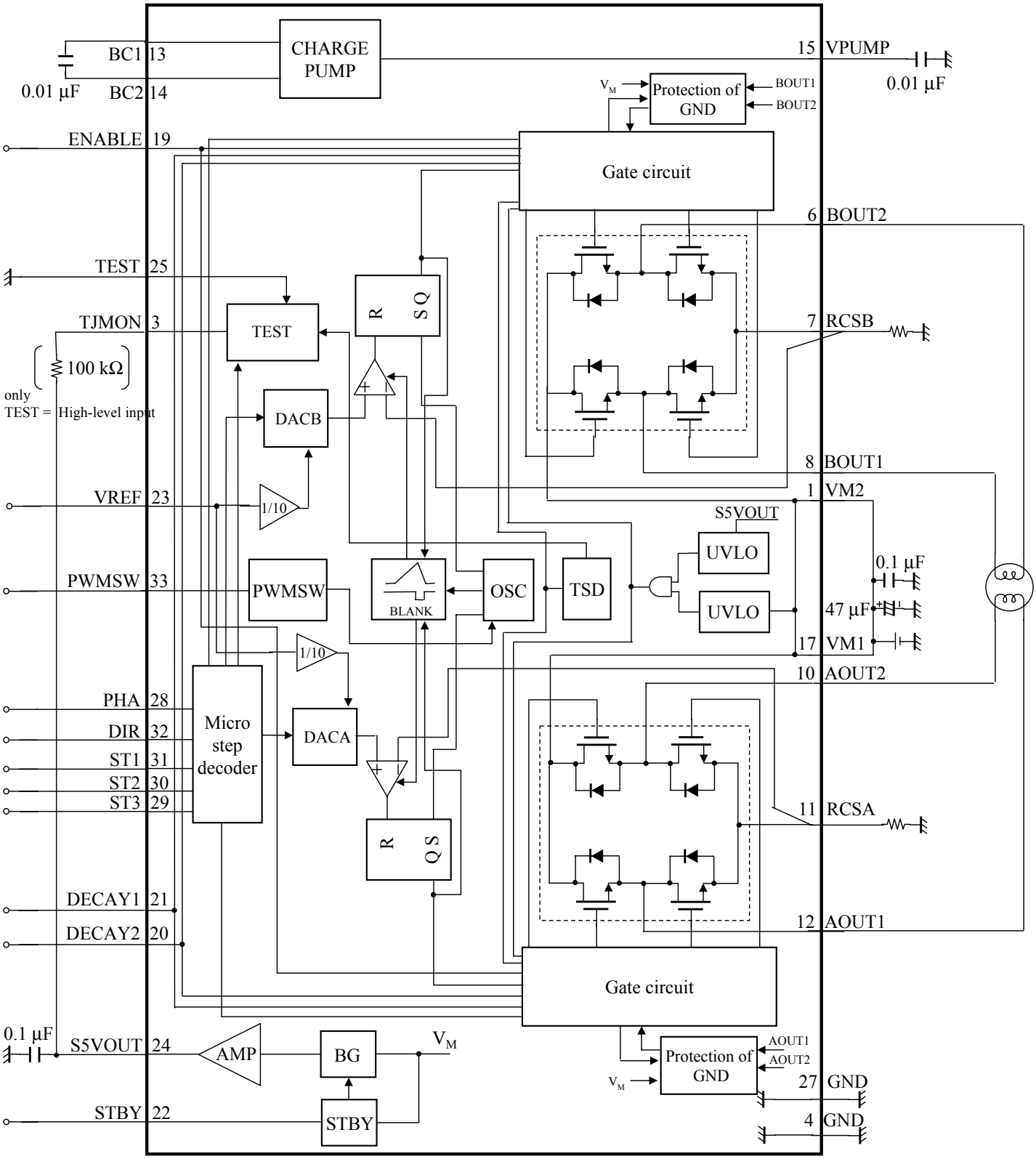
■ Package

- 34 pin plastic small outline package with heat sink (SOP type)

■ Type

- Bi-CDMOS IC

■ Application Circuit Example (Block Diagram)



Note) This application circuit is shown as an example but does not guarantee the design for mass production set.

■ Pin Descriptions

Pin No.	Pin Name	Type	Description
1	VM2	Power supply	Motor power supply 2
2	N.C.	—	—
3	TJMON	Output	VBE monitor / Test output / Home position output
4	GND	Ground	ground
5	N.C.	—	—
6	BOUT2	Output	Phase B motor drive output 2
7	RCSB	Input / Output	Phase B current detection
8	BOUT1	Output	Phase B motor drive output 1
9	GND	Ground	Die pad ground
10	AOUT2	Output	Phase A motor drive output 2
11	RCSA	Input / Output	Phase A current detection
12	AOUT1	Output	Phase A motor drive output 1
13	BC1	Output	Charge pump capacitor connection 1
14	BC2	Output	Charge pump capacitor connection 2
15	VPUMP	Output	Charge pump circuit output
16	N.C.	—	—
17	VM1	Power supply	Motor power supply 1
18	N.C.	—	—
19	ENABLE	Input	Enable / disable CTL
20	DECAY2	Input	Mix decay setup 2
21	DECAY1	Input	Mix decay setup 1
22	STBY	Input	Standby
23	VREF	Input	Torque reference voltage input
24	S5VOUT	Output	Internal reference voltage (output 5 V)
25	TEST	Input	Test mode
26	GND	Ground	Die pad ground
27	GND	Ground	Signal ground
28	PHA	Input	Clock input
29	ST3	Input	Step select 3
30	ST2	Input	Step select 2
31	ST1	Input	Step select 1
32	DIR	Input	Rotation direction
33	PWMSW	Input	PWM OFF period selection input
34	N.C.	—	—

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage (pin 1, pin 17)	V_M	37	V	*1
5	Output pin voltage (pin 6, pin 8, pin 10, pin 12)	V_{OUT}	37	V	*2
6	Motor drive current (pin 6, pin 8, pin 10, pin 12)	I_{OUT}	±2.5	A	*3, *4
7	Flywheel diode current (pin 6, pin 8, pin 10, pin 12)	I_f	2.5	A	*3, *4
2	Power dissipation	P_D	0.466	W	*5
3	Operating ambient temperature	T_{opr}	–20 to +70	°C	*6
4	Storage temperature	T_{stg}	–55 to +150	°C	*6

Note) *1: The range under absolute maximum ratings, power dissipation.

*2: This is output voltage rating and do not apply input voltage from outside to these pins. Set not to exceed allowable range at any time.

*3: Do not apply external currents to any pin specially mentioned. For circuit currents, (+) denotes current flowing into the IC and (–) denotes current flowing out of the IC.

*4: Rating when cooling fin on the back side of the IC is connected to the GND pattern of the glass epoxy 4-layer board.
(GND area: 2nd-layer or 3rd-layer: more than 1 500 mm^2)
In case of no cooling fin on the back side of the IC, rating current is 1.5 A on the glass epoxy 2-layer board.

*5: Power dissipation shows the value of only package at T_a = 70°C.
When using this IC, refer to the 7. $P_D - T_a$ diagram in the ■ Technical Data and use under the condition not exceeding the allowable value.

*6: Expect for the storage temperature and operating ambient temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	V_M	10.0 to 34.0	V	—

Note) The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Electrical Characteristics at V_M = 24 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Output drivers								
1	High-level output saturation voltage	V_{OH}	I = –1.2 A	V_M – 0.75	V_M – 0.42	—	V	—
2	Low-level output saturation voltage	V_{OL}	I = 1.2 A	—	0.54	0.825	V	—
3	Flywheel diode forward voltage	V_{DI}	I = 1.2 A	0.5	1.0	1.5	V	—
4	Output leakage current	I_{LEAK}	V_M = 37 V, V_{RCS} = 0 V	—	10	20	µA	—
5	Supply current (active)	I_M	ENABLE = High, STBY = High	—	5.5	10	mA	—
6	Supply current (STBY)	I_{MSTBY}	STBY = Low	—	25	50	µA	—
I/O block								
7	High-level STBY input voltage	V_{STBYH}	—	2.1	—	5.5	V	—
8	Low-level STBY input voltage	V_{STBYL}	—	0	—	0.6	V	—
9	High-level STBY input current	I_{STBYH}	STBY = 5 V	25	50	100	µA	—
10	Low-level STBY input current	I_{STBYL}	STBY = 0 V	–2	—	2	µA	—
11	High-level PHA input voltage	V_{PHAH}	—	2.1	—	5.5	V	—
12	Low-level PHA input voltage	V_{PHAL}	—	0	—	0.6	V	—
13	High-level PHA input current	I_{PHAH}	PHA = 5 V	25	50	100	µA	—
14	Low-level PHA input current	I_{PHAL}	PHA = 0 V	–2	—	2	µA	—
15	Highest-level PHA input frequency	f_{PHA}	—	—	—	100	kHz	—
16	High-level ENABLE input voltage	$V_{ENABLEH}$	—	2.1	—	5.5	V	—
17	Low-level ENABLE input voltage	$V_{ENABLEL}$	—	0	—	0.6	V	—
18	High-level ENABLE input current	$I_{ENABLEH}$	ENABLE = 5 V	25	50	100	µA	—
19	Low-level ENABLE input current	$I_{ENABLEL}$	ENABLE = 0 V	–2	—	2	µA	—
20	High-level PWMSW input voltage	V_{PWMSWH}	—	2.3	—	5.5	V	—
21	Middle-level PWMSW input voltage	V_{PWMSWM}	—	1.3	—	1.7	V	—
22	Low-level PWMSW input voltage	V_{PWMSWL}	—	0	—	0.6	V	—
23	High-level PWMSW input current	I_{PWMSWH}	PWMSW = 5 V	40	83	150	µA	—
24	Low-level PWMSW input current	I_{PWMSWL}	PWMSW = 0 V	–70	–36	–18	µA	—
25	PWMSW voltage at open	V_{PWMSWO}	—	1.3	1.5	1.7	V	—

■ Electrical Characteristics at V_M = 24 V (continued)

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I/O block (continued)								
26	High-level DECAY input voltage	V_{DECAYH}	—	2.1	—	5.5	V	—
27	Low-level DECAY input voltage	V_{DECAYL}	—	0	—	0.6	V	—
28	High-level DECAY input current	I_{DECAYH}	DECAY1 = DECAY2 = 5 V	25	50	100	µA	—
29	Low-level DECAY input current	I_{DECAYL}	DECAY1 = DECAY2 = 0 V	–2	—	2	µA	—
30	High-level DIR input voltage	V_{DIRH}	—	2.1	—	5.5	V	—
31	Low-level DIR input voltage	V_{DIRL}	—	0	—	0.6	V	—
32	High-level DIR input current	I_{DIRH}	DIR = 5 V	25	50	100	µA	—
33	Low-level DIR input current	I_{DIRL}	DIR = 0 V	–2	—	2	µA	—
34	High-level ST input voltage	V_{STH}	—	2.1	—	5.5	V	—
35	Low-level ST input voltage	V_{STL}	—	0	—	0.6	V	—
36	High-level ST input current	I_{STH}	ST1 = ST2 = ST3 = 5 V	25	50	100	µA	—
37	Low-level ST input current	I_{STL}	ST1 = ST2 = ST3 = 0 V	–2	—	2	µA	—
38	High-level TEST input voltage	V_{TESTH}	—	4.0	—	5.5	V	—
39	Middle-level TEST input voltage	V_{TESTM}	—	2.3	—	2.7	V	—
40	Low-level Test input voltage	V_{TESTL}	—	0	—	0.6	V	—
41	High-level TEST input current	I_{TESTH}	TEST = 5 V	25	50	100	µA	—
42	Low-level TEST input current	I_{TESTL}	TEST = 0 V	–2	—	2	µA	—
Torque control block								
43	Input bias current 1	I_{REFH}	V_{REF} = 5 V	–15	—	5	µA	—
44	Input bias current 2	I_{REFL}	V_{REF} = 0 V	–2	—	2	µA	—
45	PWM OFF time 1	T_{OFF1}	PWMSW = L	16.8	28	39.2	µs	—
46	PWM OFF time 2	T_{OFF2}	PWMSW = M	9.1	15.2	21.3	µs	—
47	PWM OFF time 3	T_{OFF3}	PWMSW = H	4.9	8.1	11.3	µs	—
48	Pulse blanking time	T_B	V_{REF} = 0 V	0.4	0.7	1.0	µs	—
49	Comp threshold	VT_{CMP}	V_{REF} = 5 V	475	500	525	mV	—
Reference voltage block								
50	Reference voltage	V_{S5VOUT}	I_{S5VOUT} = 0 mA	4.75	5.0	5.25	V	—
51	Output impedance	Z_{S5VOUT}	I_{S5VOUT} = –7 mA	—	—	10	Ω	—
Home position block								
52	At TEST high-level input TJMON output Low-level voltage	V_{TJL}	Pull up TJMON pin to 5 V with 100 kΩ.	—	0.1	0.3	V	—
53	At TEST high-level input TJMON output leakage current	$I_{TJ(leak)}$	V_{TJMON} = 5 V	—	—	5	µA	—

■Electrical Characteristics (Reference values for design) at V_M = 24 V

Note) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values for design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, Panasonic will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Output drivers								
54	Output slew rate 1	VT_r	Output voltage rise	—	220	—	V/µs	—
55	Output slew rate 2	VT_f	Output voltage fall	—	200	—	V/µs	—
56	Dead time	T_D	—	—	0.8	—	µs	—
Thermal protection								
57	Thermal protection operating temperature	TSD_{on}	—	—	150	—	°C	—
58	Thermal protection hysteresis width	ΔTSD	—	—	40	—	°C	—
Low voltage protection								
59	Protection operating voltage	V_{UVLO1}	—	—	7.9	—	V	—
60	Protection releasing voltage	V_{UVLO2}	—	—	8.7	—	V	—

■ Technical Data

1. Control mode

1) Truth table (step select)

ENABLE	DIR	ST1	ST2	ST3	Output excitation mode (phase B 90° delay: to phase A)
High	—	—	—	—	Output OFF
Low	Low	Low	Low	Low	2 phase excitation drive (4-step sequence)
Low	Low	Low	High	Low	Half-step drive (8-step sequence)
Low	Low	High	Low	Low	1-2 phase excitation drive (8-step sequence)
Low	Low	High	High	Low	W1-2 phase excitation drive (16-step sequence)
Low	Low	—	—	High	2W1-2 phase excitation drive (32-step sequence)

ENABLE	DIR	ST1	ST2	ST3	Output excitation mode (phase B 90° advance: to phase A)
High	—	—	—	—	Output OFF
Low	High	Low	Low	Low	2 phase excitation drive (4-step sequence)
Low	High	Low	High	Low	Half-step drive (8-step sequence)
Low	High	High	Low	Low	1-2 phase excitation drive (8-step sequence)
Low	High	High	High	Low	W1-2 phase drive (16-step sequence)
Low	High	—	—	High	2W1-2 phase drive (32-step sequence)

2) Truth table (control/charge pump circuit)

STBY	ENABLE	Control /Charge pump circuit	Output transistor
Low	—	OFF	OFF
High	High	ON	OFF
High	Low	ON	ON

3) Truth table (PWM OFF period selection)

PWMSW	PWM OFF period
Low	28.0 µs
Middle	15.2 µs
High	8.1 µs

4) Truth table (decay selection)

DECAY1	DECAY2	Decay control
Low	Low	Slow decay
Low	High	25%
High	Low	50%
High	High	100%

5) Truth table (test mode)

TEST	TJMON
Low	VBE monitor
Middle	Test output (Output transistor: OFF)
High	Home position output

Note) For each PWM OFF period, Fast decay is applied according to the above table.

■ Technical Data (continued)

2. Each phase current value

1) 1-2 phase, W1-2 phase, 2W1-2 phase DIR = Low

Note) The definition of Phase A and B current 100%: (VREF × 0.1) / current detection resistance

1-2 phase (8 step)	W1-2 phase (16 step)	2W1-2 phase (32 step)	Phase A current (%)	Phase B current (%)
		1	19.5	–98.1
	1	2	38.3	–92.4
		3	55.6	–83.2
1	2	4	70.7	–70.7
		5	83.2	–55.6
	3	6	92.4	–38.3
		7	98.1	–19.5
2	4	8	100	0
		9	98.1	19.5
	5	10	92.4	38.3
		11	83.2	55.6
3	6	12	70.7	70.7
		13	55.6	83.2
	7	14	38.3	92.4
		15	19.5	98.1
4	8	16	0	100
		17	–19.5	98.1
	9	18	–38.3	92.4
		19	–55.6	83.2
5	10	20	–70.7	70.7
		21	–83.2	55.6
	11	22	–92.4	38.3
		23	–98.1	19.5
6	12	24	–100	0
		25	–98.1	–19.5
	13	26	–92.4	–38.3
		27	–83.2	–55.6
7	14	28	–70.7	–70.7
		29	–55.6	–83.2
	15	30	–38.3	–92.4
		31	–19.5	–98.1
8	16	32	0	–100

■ Technical Data (continued)

2. Each phase current value (continued)

2) 1-2 phase, W1-2 phase, 2W1-2 phase DIR = High

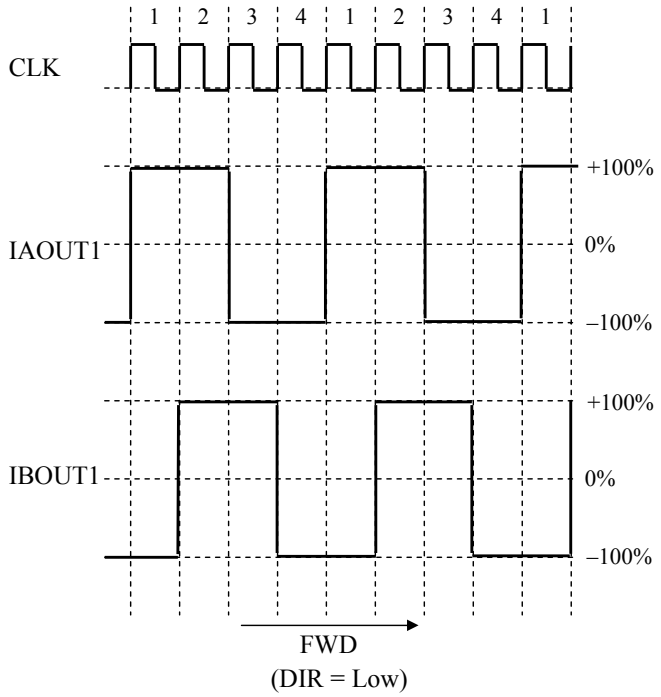
Note) The definition of Phase A and B current 100%: (VREF × 0.1) / current detection resistance

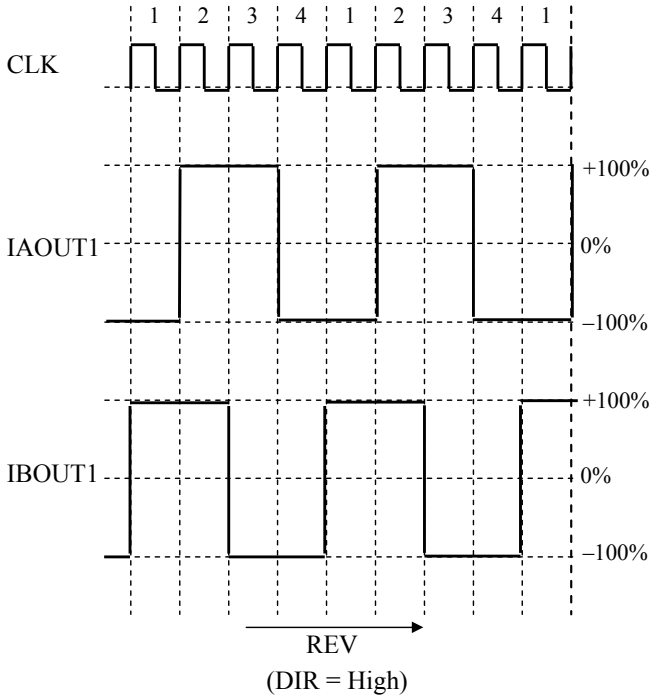
1-2 phase (8 step)	W1-2 phase (16 step)	2W1-2 phase (32 step)	Phase A current (%)	Phase B current (%)
		1	–19.5	–98.1
	1	2	–38.3	–92.4
		3	–55.6	–83.2
1	2	4	–70.7	–70.7
		5	–83.2	–55.6
	3	6	–92.4	–38.3
		7	–98.1	–19.5
2	4	8	–100	0
		9	–98.1	19.5
	5	10	–92.4	38.3
		11	–83.2	55.6
3	6	12	–70.7	70.7
		13	–55.6	83.2
	7	14	–38.3	92.4
		15	–19.5	98.1
4	8	16	0	100
		17	19.5	98.1
	9	18	38.3	92.4
		19	55.6	83.2
5	10	20	70.7	70.7
		21	83.2	55.6
	11	22	92.4	38.3
		23	98.1	19.5
6	12	24	100	0
		25	98.1	–19.5
	13	26	92.4	–38.3
		27	83.2	–55.6
7	14	28	70.7	–70.7
		29	55.6	–83.2
	15	30	38.3	–92.4
		31	19.5	–98.1
8	16	32	0	–100

■ Technical Data (continued)

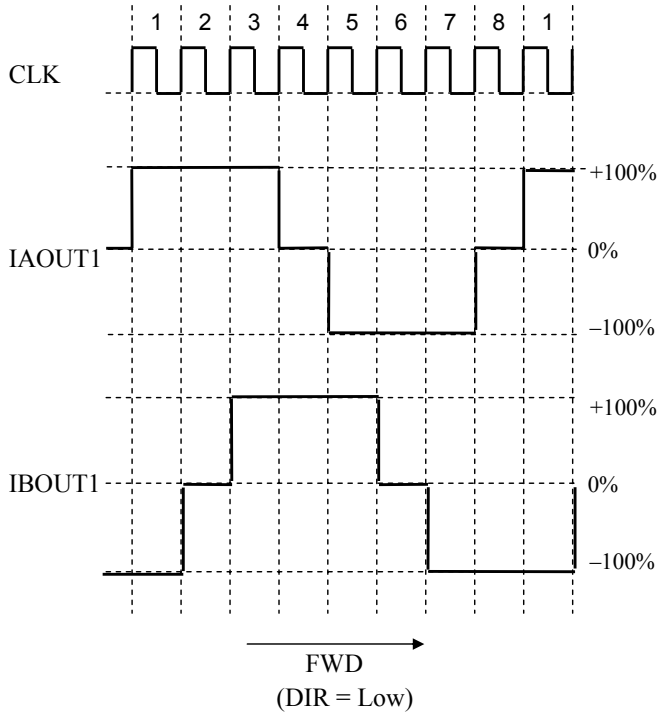
3. Each phase current (timing chart)

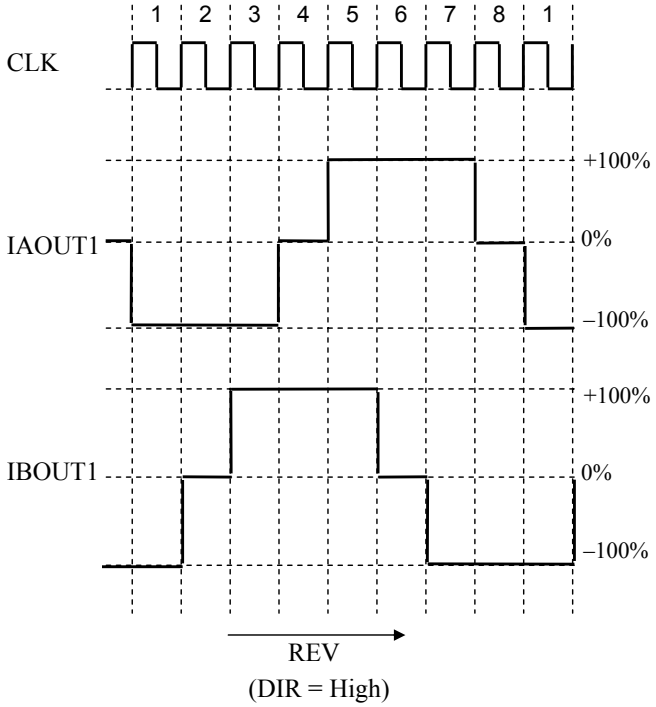
1) 2 phase excitation drive (4-step sequence)
(ST1 = Low, ST2 = Low, ST3 = Low)





2) Half-step drive (8-step sequence)
(ST1 = Low, ST2 = High, ST3 = Low)

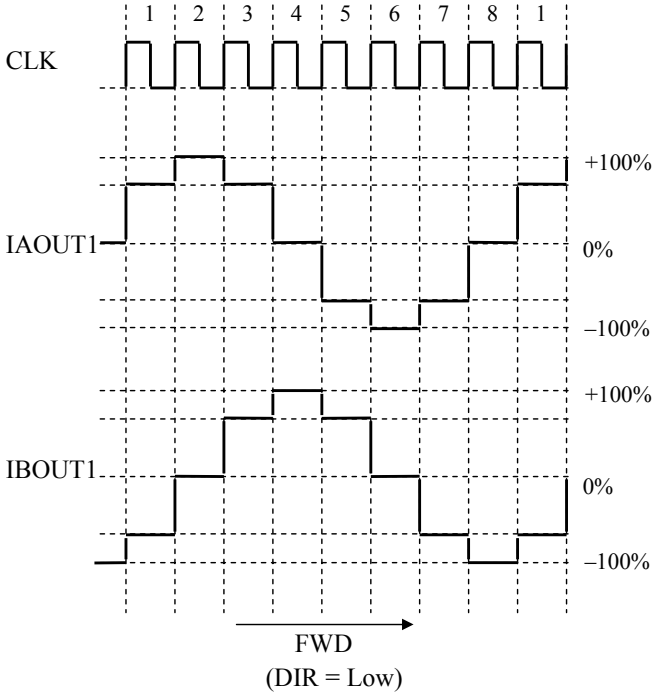


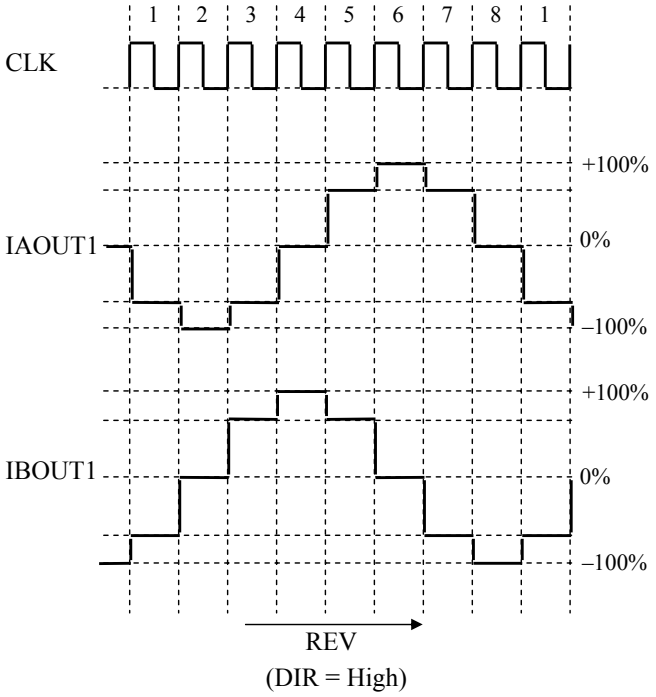


■ Technical Data (continued)

3. Each phase current (timing chart) (continued)

3) 1-2 phase excitation (8-step sequence)
(ST1 = High, ST2 = Low, ST3 = Low)

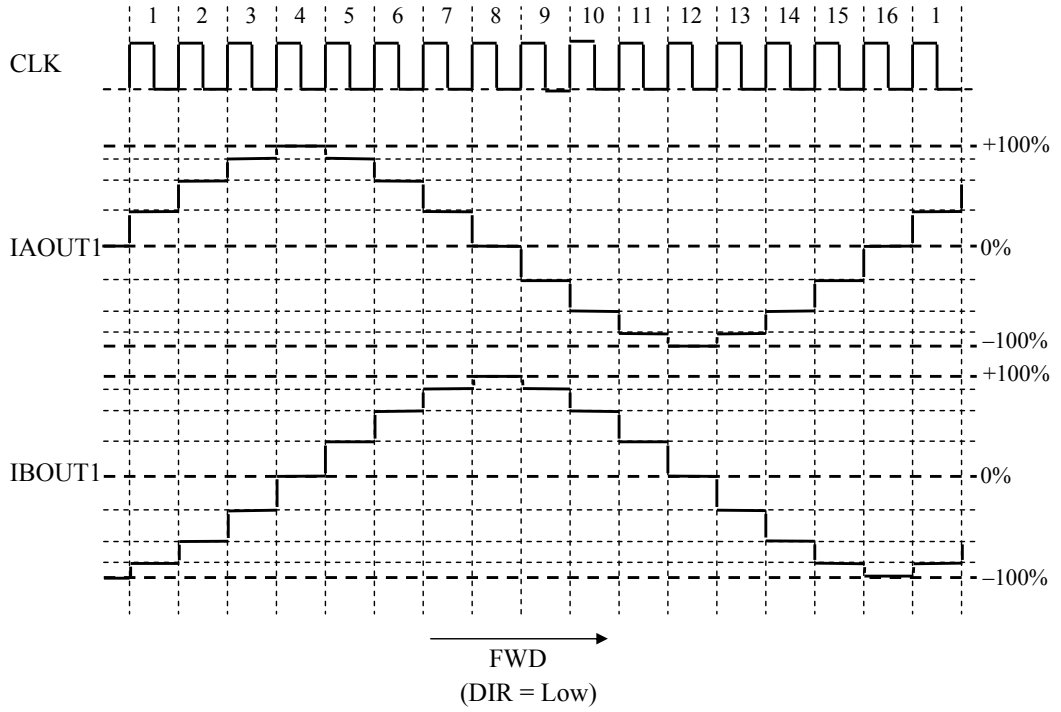


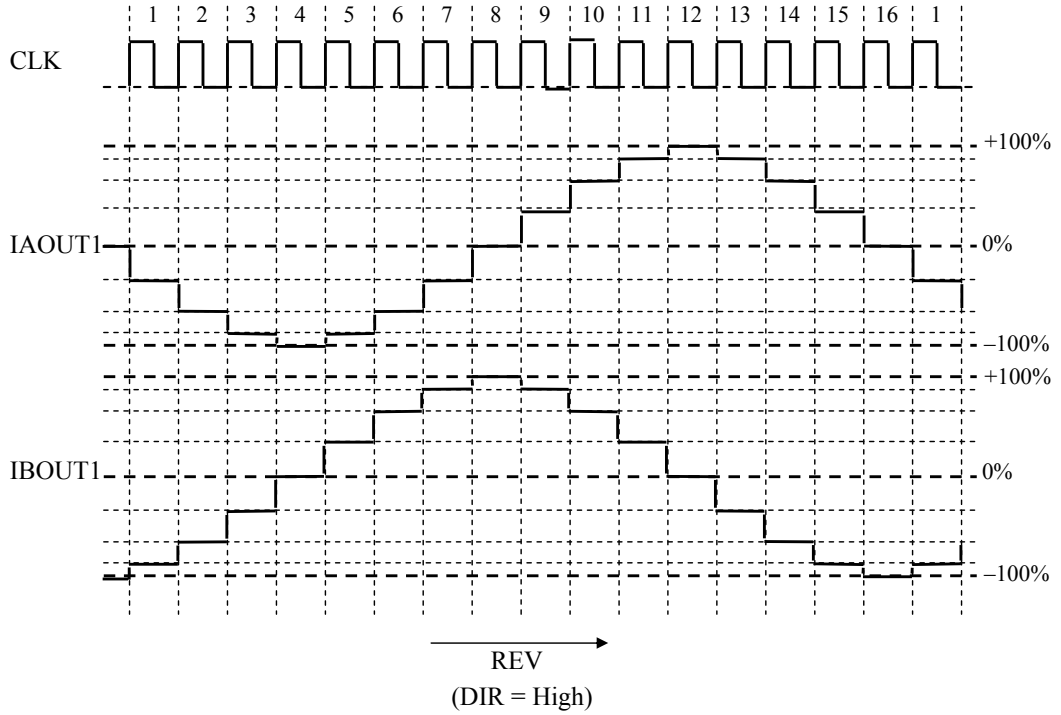


■ Technical Data (continued)

3. Each phase current (timing chart) (continued)

4) W1-2 phase excitation (16-step sequence)
(ST1 = High, ST2 = High, ST3 = Low)

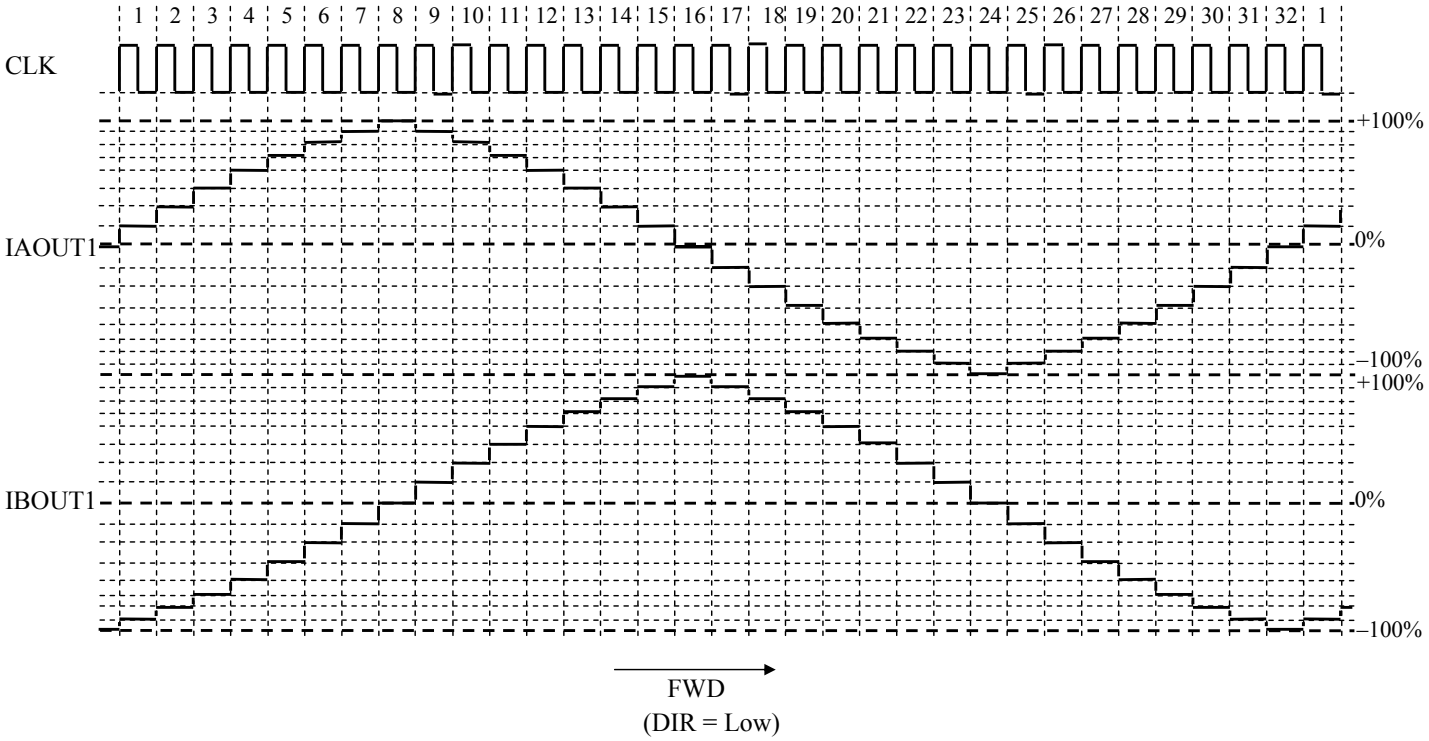


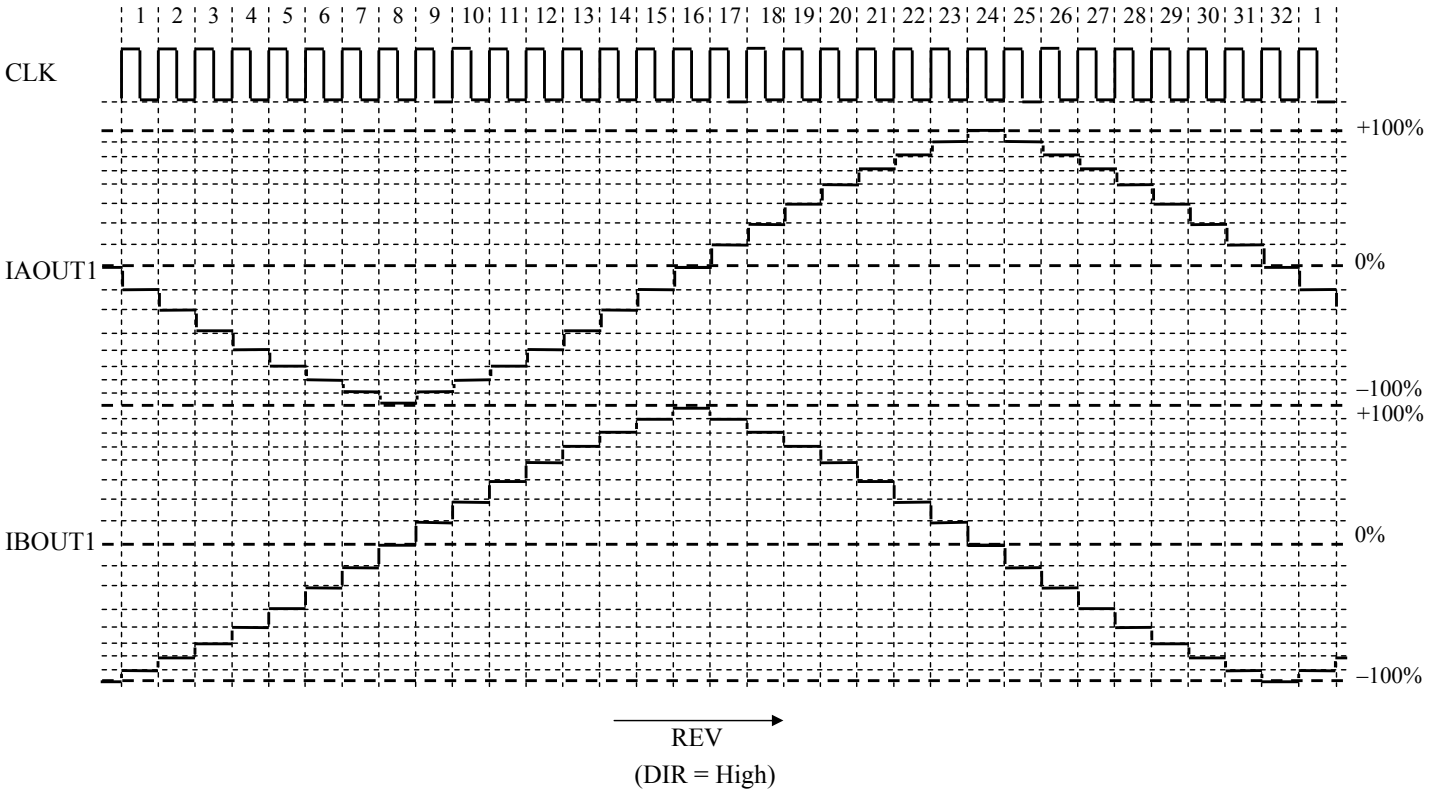


■ Technical Data (continued)

3. Each phase current (timing chart) (continued)

5) 2W1-2 phase excitation (32-step sequence)
(ST3 = High)

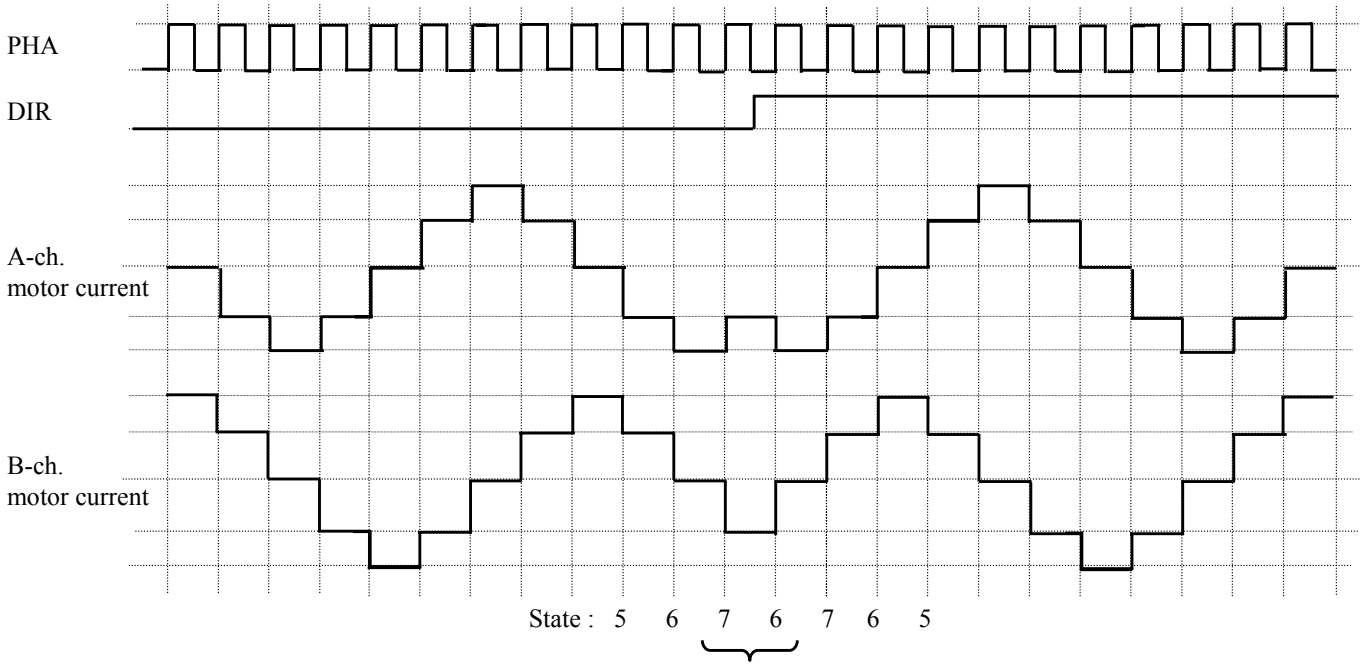




■ Technical Data (continued)

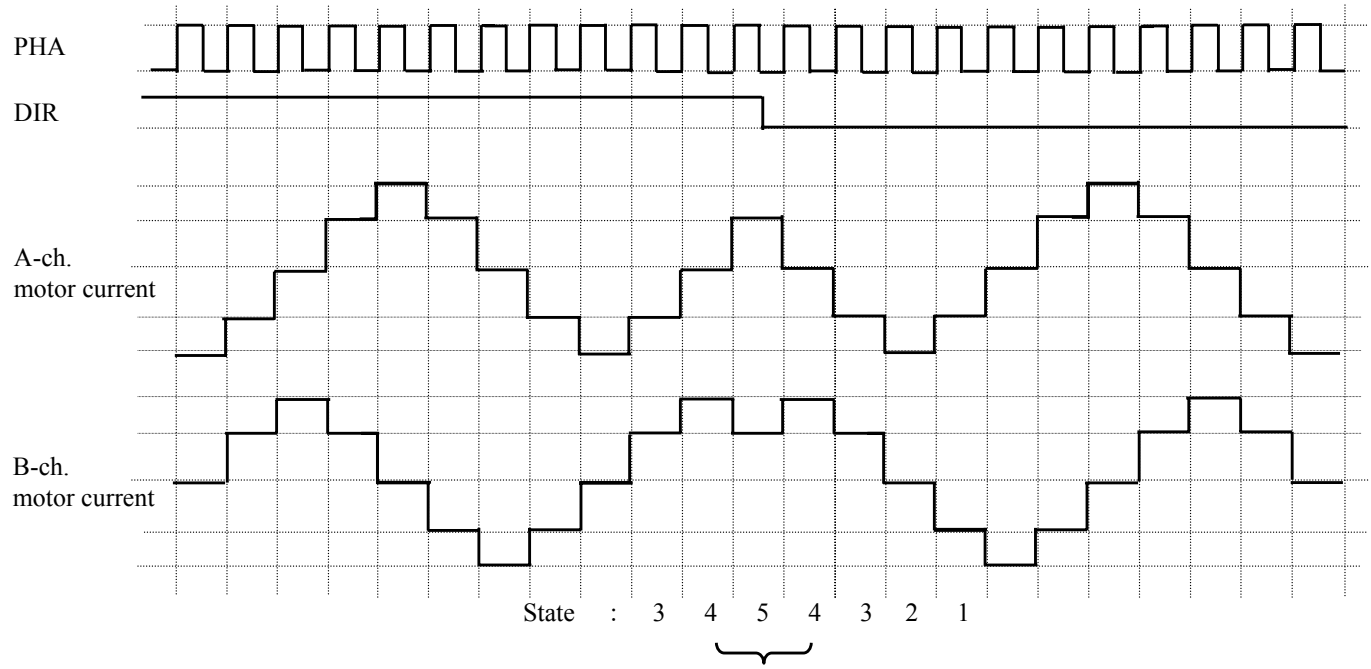
4. Timing chart at change of DIR

(Ex.1) Timing chart at 1-2 phase excitation (DIR: Low → High)



At change of DIR, the state before the change is held and the operation is continued.

(Ex.2) Timing chart at 1-2 phase excitation (DIR: High → Low)



At change of DIR, the state before the change is held and the operation is continued.

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(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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