YAMAHA LSI

YMU759

PRELIMINARY

May 8 .2000

MA-2

Outline

YMU759 is a synthesis LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decoder that are included in this device. As a synthesis, YMU759 is equipped with Yamaha's original FM synthesizer, with which the device is capable of simultaneously generating up to 16 voices with different tones. Since the device is capable of generating ADPCM data simultaneously synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects.
Since the play data of YMU759 are interpreted at anytime through FIFO, the length of the data (playing period) is not limited, so the device can flexibly support applications such as incoming call melody distribution service.
The hardware sequencer built in this device allows playing of complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

Features

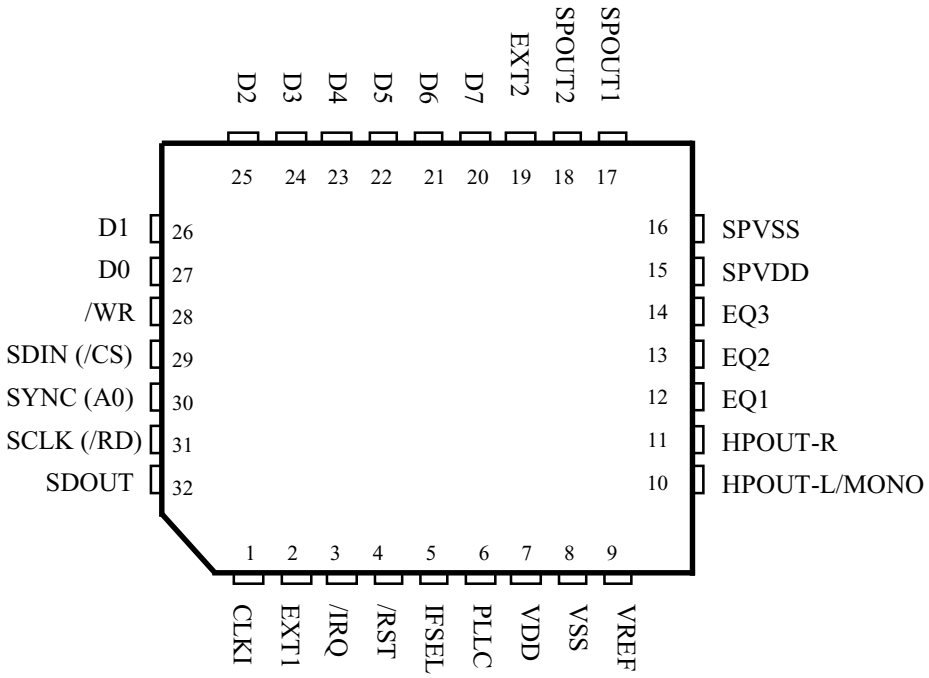
- Equipped with FM sound generator function and ADPCM playback function.
- Number of voices simultaneously generated
  When only 2-operator tones are used: up to 16 voices can be generated simultaneously.
  When only 4-operator tones are used: up to 8 voices can be generated simultaneously.
- Built-in 4-bits 1ch ADPCM decoder, and supports two kinds of sampling frequency, 4 kHz and 8 kHz.
- Built-in output 550mW(AVDD=3.6V) speaker amplifier:
- Built-in hardware sequencer.
- Built-in circuit for sound quality correcting equalizer.
- Supports stereophonic output.
- Built-in 16-bit stereophonic D/A converter.
- Provided with a stereophonic analog output terminal for headphone.
- 4 wire serial interface or 12 wire parallel interface can be selected.
- PLL is built-in to support master clock input in 2 MHz to 20 MHz range.
- Supports power down mode. (Typical current: 1 uA or less)
- Power supply is divided into analog power supply for speaker amplifier and power supply for the others.
  Analog power supply for speaker amplifier (SPVDD): 2.7V~4.5V(Typ 3.6V).
  Digital power supply for the others(VDD): 2.7V~3.3V(Typ 3.0V)
- 32-pin plastic QFN.

The contents of this booklet are target specifications and they are subject to change without a prior notice. Please check the finalized specifications before actually using this LSI.

YAMAHA CORPORATION

YMU759 CATALOG
CATALOG No.:LSI-4MU759A0
2000.5

Terminal configuration



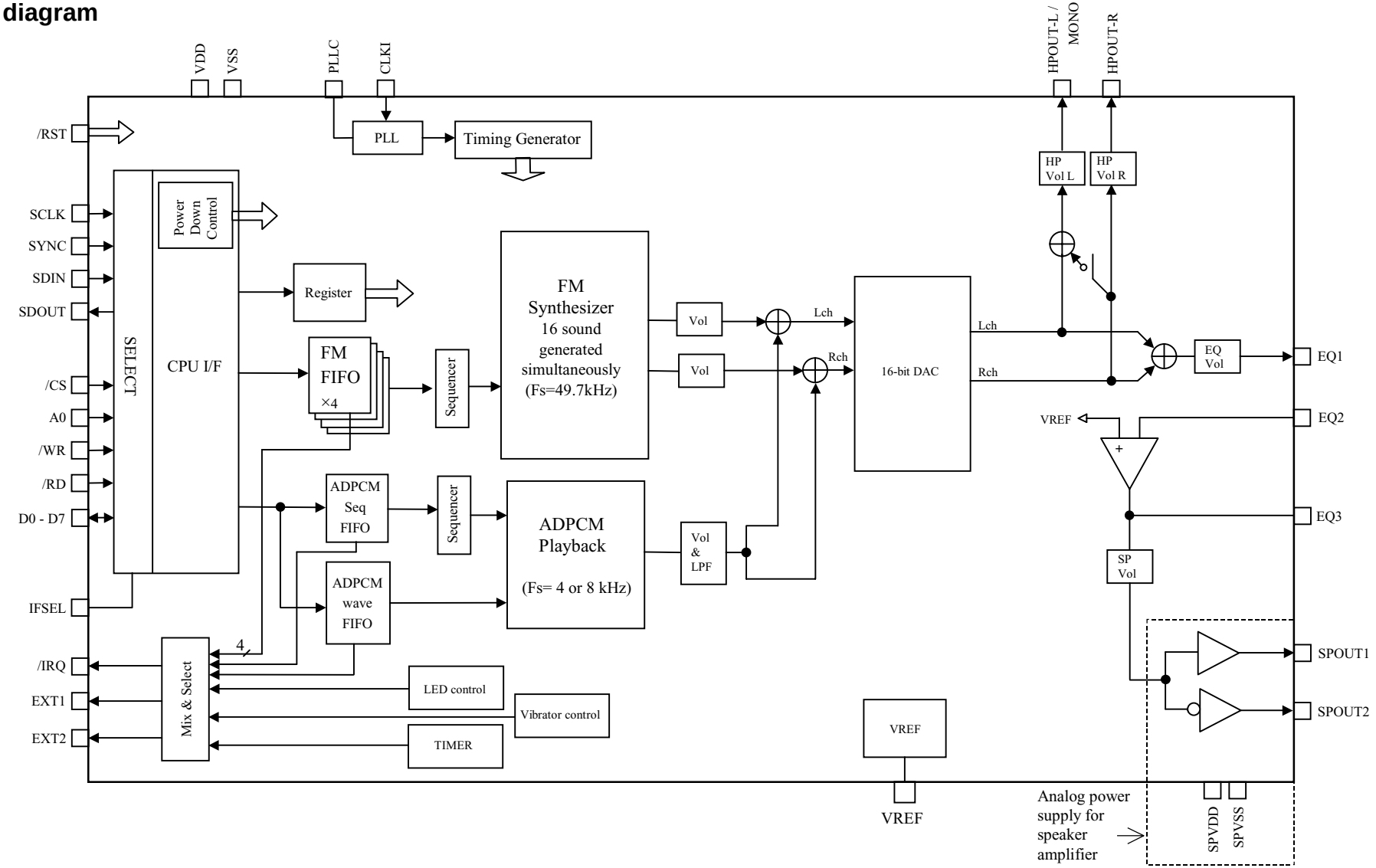
<32pin QFN Top View>

Terminal functions

No.	Name	I/O	Function
1	CLKI	Ish	Clock input (2~20MHz)
2	EXT1	O	External device control terminal 1
3	/IRQ	O	Interruption output
4	/RST	Ish	Hardware reset input
5	IFSEL	I	CPU I/F selection L: Serial I/F, H: Parallel I/F
6	PLLC	A	Connection of capacitor for built in PLL Connect 0.01 µF (expected) capacitor between this terminal and VSS.
7	VDD	-	Digital power supply (Typically +3.0V) Connect 0.1 µF and 4.7 µF capacitors between this terminal and VSS
8	VSS	-	Ground
9	VREF	A	Analog reference voltage. Connect 0.1 µF capacitor between this terminal and VSS
10	HPOUT-L / MONO	A	Headphone L channel output: can be switched to mono through register setting
11	HPOUT-R	A	Headphone R channel output
12	EQ1	A	Equalizer terminal 1
13	EQ2	A	Equalizer terminal 2
14	EQ3	A	Equalizer terminal 3
15	SPVDD	-	Analog power supply (Typically +3.6 V) Connect 0.1 µF and 4.7 µF capacitors between this terminal and SPVSS
16	SPVSS	-	Analog ground for speaker amplifier
17	SPOUT1	A	Speaker terminal 1
18	SPOUT2	A	Speaker terminal 2
19	EXT2	O	External device control terminal 2
20	D7	I/O	Parallel I/F data bus 7
21	D6	I/O	Parallel I/F data bus 6
22	D5	I/O	Parallel I/F data bus 5
23	D4	I/O	Parallel I/F data bus 4 (To be open when IFSEL=L)
24	D3	I/O	Parallel I/F data bus 3 (To be open when IFSEL=L)
25	D2	I/O	Parallel I/F data bus 2 (To be open when IFSEL=L)
26	D1	I/O	Parallel I/F data bus 1 (To be open when IFSEL=L)
27	D0	I/O	Parallel I/F data bus 0 (To be open when IFSEL=L)
28	/WR	Ish	Parallel I/F write pulse (To be open when IFSEL=L)
29	SDIN (/CS)	Ish	IFSEL= L Serial I/F data input IFSEL= H Parallel I/F chip select input
30	SYNC (A0)	Ish	IFSEL= L Serial I/F data take-in signal IFSEL= H Parallel I/F address signal
31	SCLK (/RD)	Ish	IFSEL= L Serial I/F bit clock input IFSEL= H Parallel I/F read pulse
32	SDOUT	OD	Serial I/F data output (Pull up resistance is necessary for the outside)

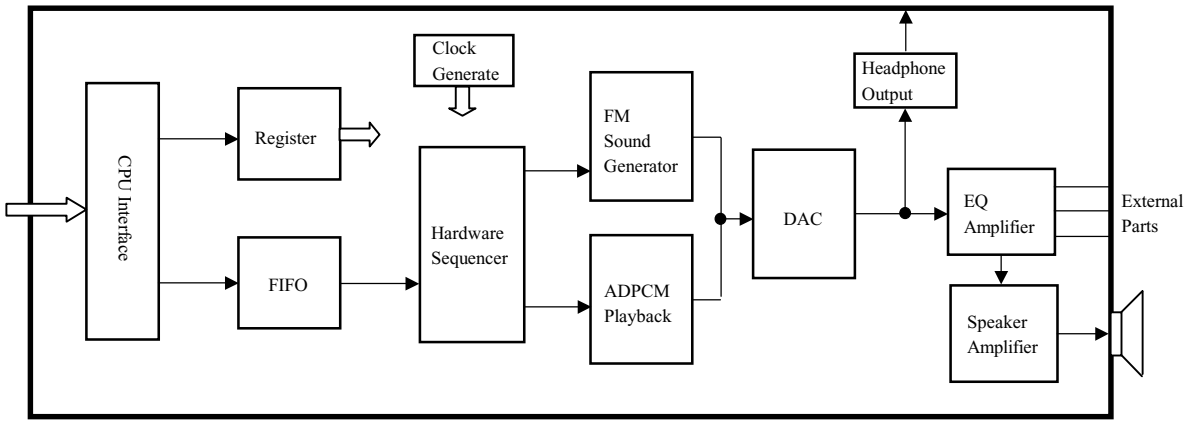
Comment: Ish= Schmitt input, OD= open drain terminal, A= Analog terminal

Block diagram



Outline of blocks

Explanation about outline of built-in each blocks and flow of the signal are follows.



CPU interface

Receives commands send from external CPU, interprets the contents, and then writes them into registers by index address. Controls reading of designated register data.

As interfaces for controlling YMU759, 4 wire serial and 12 wire parallel interfaces are provided, which can be selected through IFSEL terminal.

Registers

Register groups that control the LSI except for sequence data.

FM tone register data, various volumes and other control data are store here.

FIFO

Sequence data to move hardware sequencer and ADPCM wave data are stored in FIFO.

This device is equipped with four FIFOs for FM and two FIFOs for ADPCM.

The FIFOs for FM stores sequence data and those for ADPCM stores sequence and waveform data. The size of FIFOs for FM is 96 bytes, the one for ADPCM data is 384 bytes, and the one for sequence data is 32 bytes.

Hardware sequencer

FIFO is provided as a previous stage of the sequencer which reads sequence data from FIFO to control FM and ADPCM sections.

The sequence data are compatible with SMAF(Synthetic music Mobile Application Format) proposed by yamaha.

FM synthesis

This is a synthesis that uses Yamaha's original FM system. It is able to generate up to 16 voices simultaneously.

This section plays in accordance with commands from the sequencer.

It can also play by directly controlling various registers without using the sequencer.

The sampling frequency is 49.7 kHz that complies with stereophonic sound.

ADPCM playback

This section decodes 4 bit ADPCM data to 16 bit data by using the sampling frequency of 4 kHz or 8 kHz.

It can playback one voice. It playback according to command from sequencer.

And it can playback to control various register directly without using sequencer.

DAC

Converts digital signal from FM and ADPCM section to analog voice signal with resolution of 16 bits.

Headphone output

This section supports stereophonic analog output for the headphone. Monaural output is available by changing the setting. And built in volume adjust output level.

EQ amplifier

This section is used to set the response of filter or the gain by externally connecting a resistor and capacitor.

Speaker amplifier

A speaker amplifier is built in this device, which maximum output is 550 mW at AVDD=3.6 V.
Built in volume adjust output level in front of amplifier.
High ripple removal rate is provided.
And, include protection circuit for short of speaker output terminal.
(The final specification may not include the short-circuit protection circuit.)

Clock generate

This block makes a necessary clock by increasing 2 to 20 MHz clock inputted through CLK1 terminal using the built-in PLL.
The clock generated in this section is supplied to the inside of digital circuit.

Electrical Characteristics

Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
Power supply voltage (analog)	SPV_{DD}	-0.3	6.0	V
Power supply voltage (digital)	V_{DD}	-0.3	4.2	V
Analog input voltage	V_{INA}	-0.3	SPVDD+0.3	V
Digital input voltage	V_{IND}	-0.3	VDD+0.3	V
Operating ambient temperature	T_{OP}	-20	85	°C
Storage temperature	T_{STG}	-50	125	°C

Note: VSS = SPVSS = 0V

Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Operating voltage (Speaker amp)	SPV_{DD}	2.7	3.6	4.5	V
Operating voltage (The others)	V_{DD}	2.7	3.0	3.3	V
Operating ambient temperature	T_{OP}	-20	25	85	°C

Note: VSS = SPVSS = 0V

DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max	Unit
Input voltage “H” level	V_{IH1}		$0.7 \times V_{dd}$	-	-	V
Input voltage “L” level	V_{IL1}		-	-	$0.2 \times V_{DD}$	V
Output voltage “H” level	V_{OH}	I_{OL} = *1	$0.8 \times V_{dd}$	-	-	V
Output voltage “L” level	V_{OL}	I_{OH} = *1	-	-	0.4	V
Schmitt width	Vsh			1.0		V
Input leakage current	IL		-10		10	µA
Input capacity	CI				10	pF

Note: T_{OP}= -20 ~ 85°C, VDD=3.0±0.3 V, Capacitor load=50 pF.

*1 I_{OL}=and I_{OH}= 2 mA for /IRQ, SDOUT and D0 to D7 (Only I_{OL} for SDOUT)

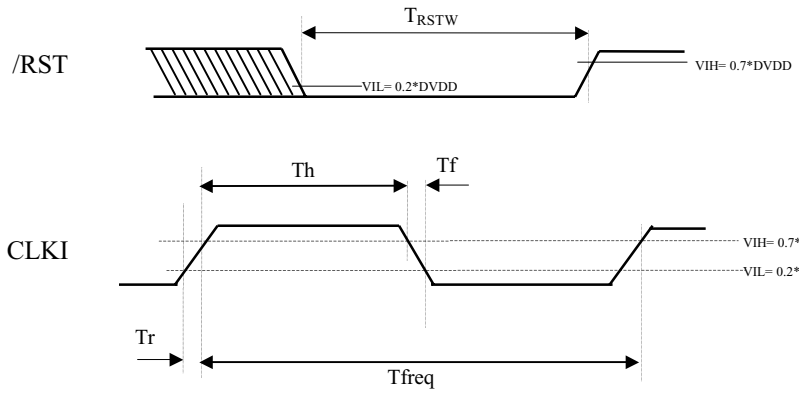
I_{OL}=I_{OH}= 6 mA for EXT1 and EXT2.

AC characteristics

/RST, CLKI

Item	Symbol	Min.	Typ.	Max.	Unit
/RST active “L” pulse width	T_{RSTW}	1024			× CLKI
CLKI frequency	1 / Tfreq	2		20	MHz
CLKI rise time / fall time	Tr / Tf			30	ns
CLKI duty	Th/Tfreq	30	50	70	%

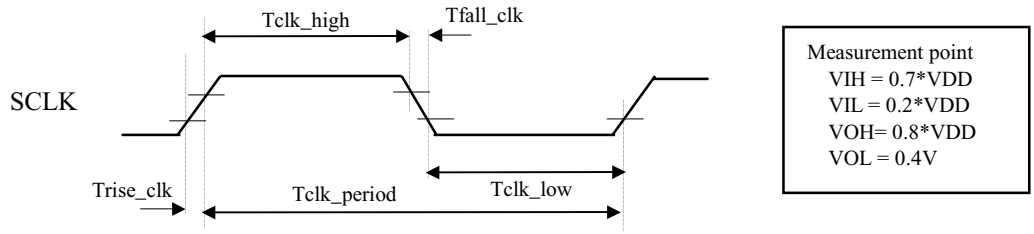
Note: T_{OP}=-20 ~ 85°C, VDD=3.0±0.3 V, Capacitor load=50 pF.

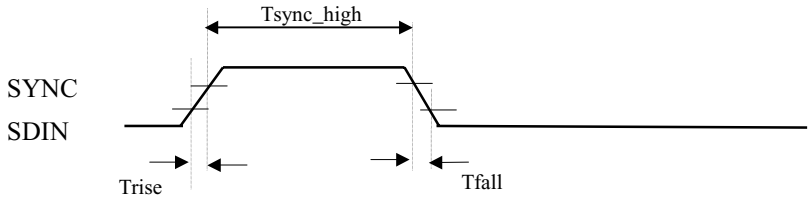


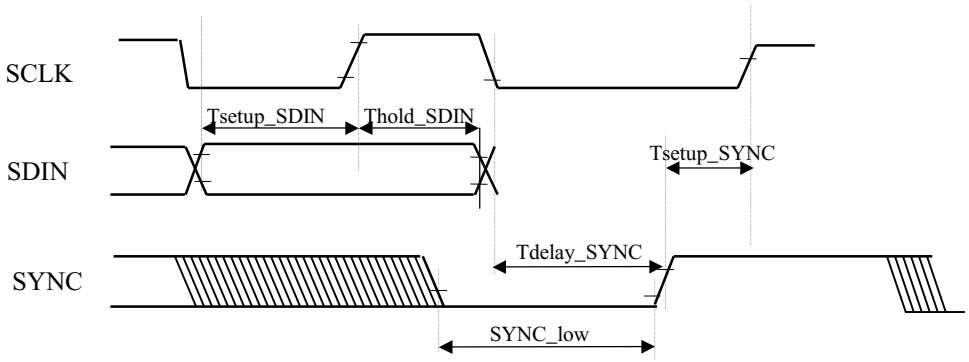
Serial I/F

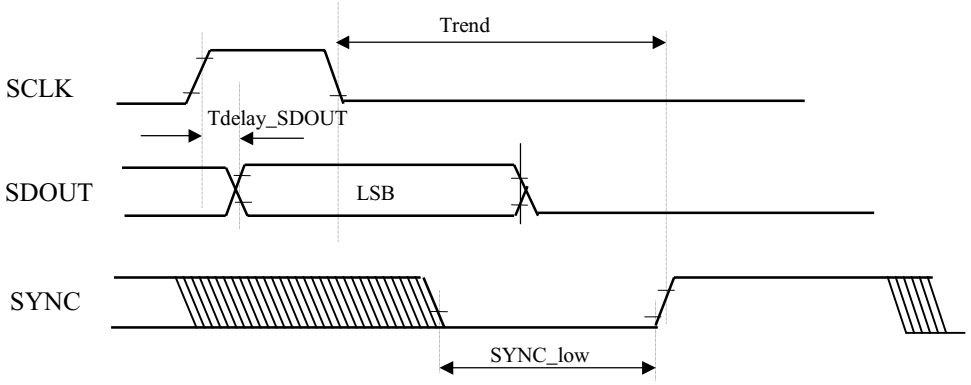
Item	Symbol	Min.	Typ.	Max.	Unit
SCLK clock period	Tclk_period	80			ns
SCLK “L” pulse width	Tclk_low	20			ns
SCLK “H” pulse width	Tclk_high	20			ns
SCLK rise time	Trise_clk			30	ns
SCLK fall time	Tfall_clk			30	ns
SYNC “H” pulse width	Tsync_high	30		-	ns
SYNC “L” pulse width	Tsync_low	30			ns
SYNC / SDIN rise time	Trise			30	ns
SYNC / SDIN fall time	Tfall			30	ns
SYNC delay time	Tdelay_SYNC	0			ns
SUNC -> SCLK setup time	Tsetup_SYNC	50			ns
SDIN setup time	Tsetup	20			ns
SDIN hold time	Thold	20			ns
SDOUT delay time	Tdelay_SDOUT			30	ns
Read Command clear time	Trend	50			ns
Read wait time	Trd_wait	300			ns

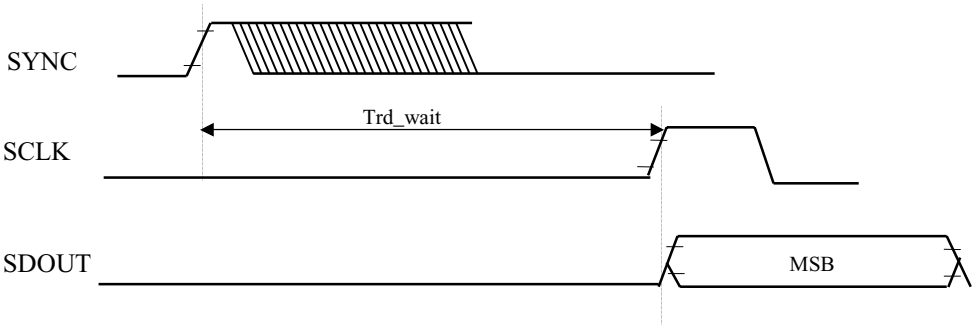
Note: T_{OP}=-20 ~ 85°C, VDD=3.0±0.3 V, Capacitor load=50 pF.


Tclk_high
Tfall_clk
SCLK
Trise_clk
Tclk_period
Tclk_low
Measurement point
VIH = 0.7*VDD
VIL = 0.2*VDD
VOH= 0.8*VDD
VOL = 0.4V


Tsync_high
SYNC
SDIN
Trise
Tfall


SCLK
Tsetup_SDIN
Thold_SDIN
SDIN
Tsetup_SYNC
Tdelay_SYNC
SYNC
SYNC_low


Trend
SCLK
Tdelay_SDOUT
SDOUT
LSB
SYNC
SYNC_low


SYNC
Trd_wait
SCLK
SDOUT
MSB

Parallel I/F (write cycle)

Item	Symbol	Min.	Max.	Unit
Chip select width	T_{CSW}	100		ns
Address setup time	T_{AS}	10		ns
Write pulse width	T_{WW}	50		ns
Data setup time	T_{WDS}	30		ns
Data hold time	T_{WDH}	0		ns

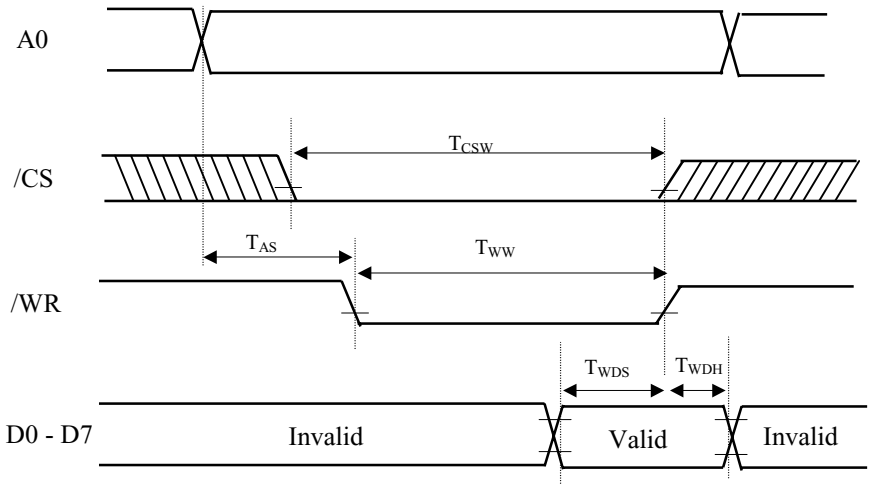
Note: T_{OP}=-20 ~ 85°C, VDD=3.0±0.3 V, Capacitor load=50 pF.

(Read cycle)

Item	Symbol	Min.	Max.	Unit
Chip select width	T_{CSR}	100		ns
Address setup time	T_{AS}	0		ns
Read pulse width	T_{RW}	80		ns
Read data access time	T_{ACC}		70	ns
Data hold time	T_{RDH}	10	50	ns

Note: T_{OP}=-20 ~ 85°C, VDD=3.0±0.3 V, Capacitor load=50 pF.

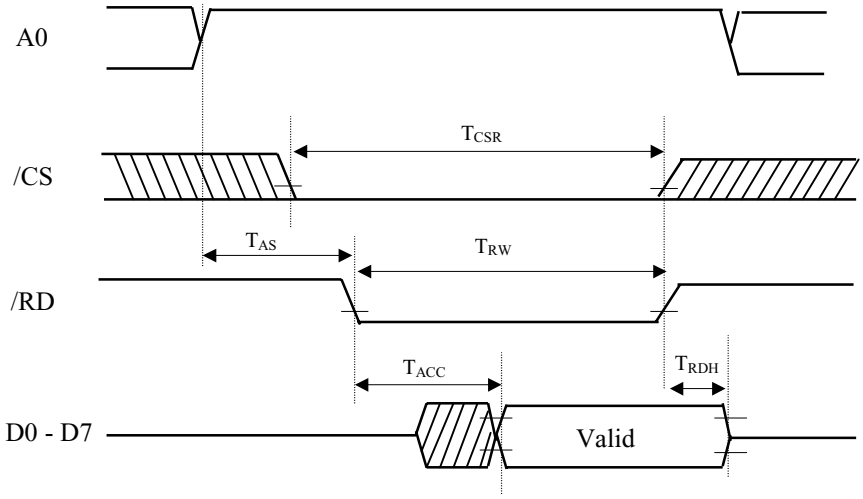
Write cycle



Note: T_{CSW}, T_{WW}, and T_{WDH} are defined with respect to the moment /CS or /WR becomes High level.

Measurement point
VIH = 0.7*VDD
VIL = 0.2*VDD
VOH= 0.8*VDD
VOL = 0.4V

Read cycle



Note: T_{ACC} is defined with respect to the moment /CS or /RD becomes Low level later.
T_{CSR}, T_{RW} and T_{RDH} are defined with respect to the moment /CS or /RD becomes High level.

Measurement point
VIH = 0.7*VDD
VIL = 0.2*VDD
VOH= 0.8*VDD
VOL = 0.4V

Power consumption

Item	Min.	Typ.	Max.	Unit
VDD section (normal operation)		15		mA
SPVDD section (no voice)		5(expectation)		mA
SPVDD section 8 Ω load and 500 mW output		TBD		mA
Power down mode (VDD + SPVDD)		1	TBD	µA

Note: T_{OP}=-20 ~ 85°C, VDD=3.0±0.3 V, SPVDD=3.6V.

Analog characteristics

SP amplifier

Item	Min.	Typ.	Max.	Unit
Gain setting (fixed)		±2		Times
Minimum load resistance (RL)		8		Ω
Maximum output voltage amplitude (RL=8 Ω)		6.0		Vp-p
Maximum output power (RL=8 Ω, THD+N<=0.05%)		520		mW
Maximum output power (RL=8 Ω, THD+N<=1.0%)		600		mW
THD + N (RL=8 Ω, f=1kHz, output=500 mW)		TBD		%
Noise at no signal (A-filter; filter equalize feeling of hearing)		-90		dBv
PSRR (f=1kHz)		TBD		dB

Note: T_{OP}=25 °C, VDD=3.0 V and SPVDD=3.6 V.

EQ amplifier

Item	Min.	Typ.	Max.	Unit
Gain setting range			30	dB
Maximum output current	120			µA
Maximum output voltage amplitude		1.5		Vp-p
THD + N (f=1kHz)			TBD	%
Noise at no signal (A-filter)		-90		dBv
Input impedance	10			MΩ

Note: T_{OP}=25 °C, VDD=3.0 V and SPVDD=3.6 V.

SP Volume

Item	Min.	Typ.	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBv
THD + N (f=1kHz)			TBD	%

Note: T_{OP}=25 °C, VDD=3.0 V and SPVDD=3.6 V

EQ Volume

Item	Min.	Typ.	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBv
Maximum output current	120			µA
Maximum output voltage amplitude		1.5		Vp-p
Output impedance		300	600	Ω

Note: T_{OP}=25°C, VDD=3.0V and SPVDD=3.6V.

HP Volume

Item	Min.	Typ.	Max.	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise at no signal (A-filter)		-90		dBv
Maximum output current	120			µA
Maximum output voltage amplitude		1.5		Vp-p
Output impedance		300	600	Ω

Note: T_{OP}=25°C, VDD=3.0V and SPVDD=3.6V

VREF

Item	Min.	Typ.	Max.	Unit
VREF voltage		×1/2		VDD

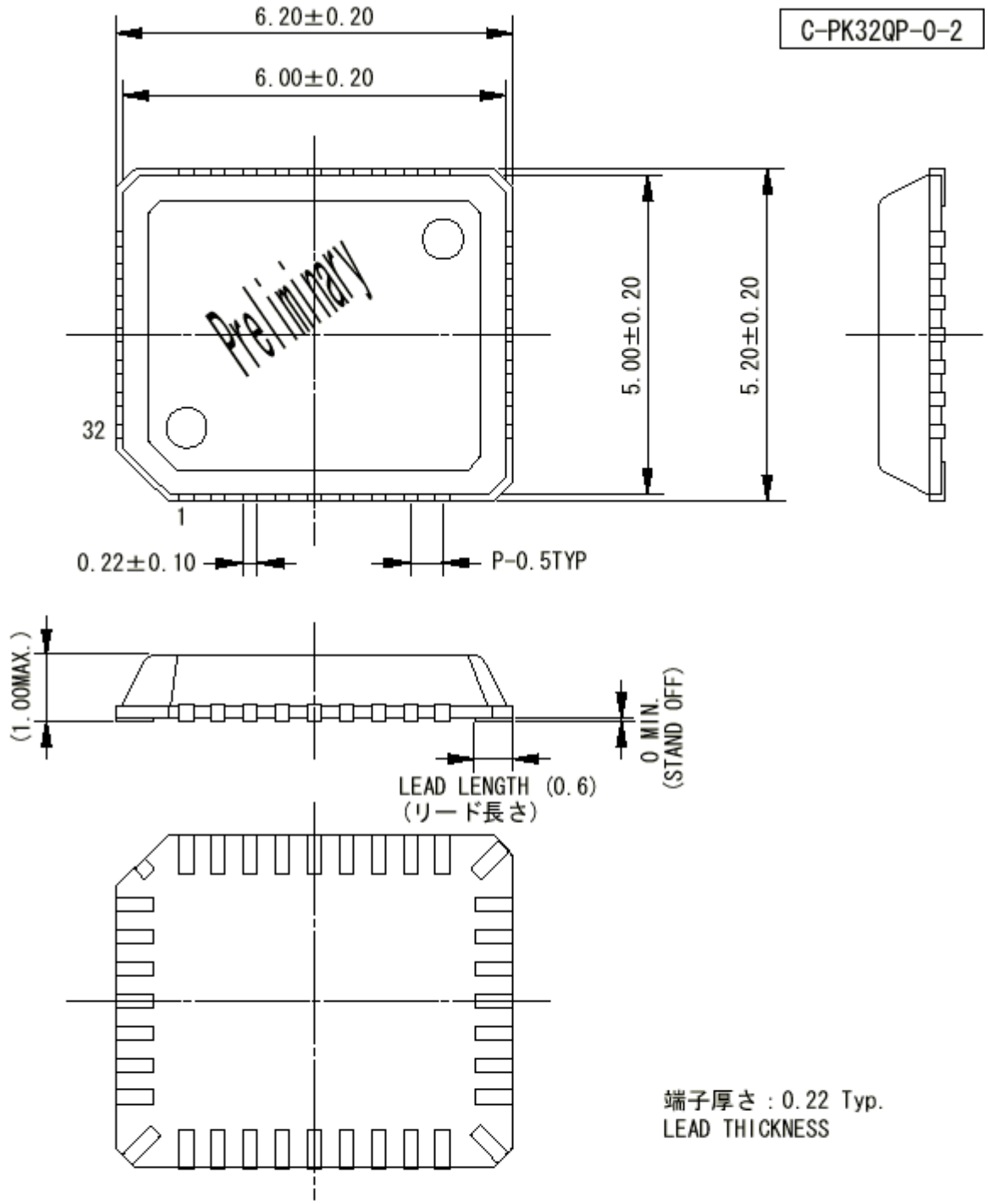
Note: T_{OP}=25°C, VDD=3.0V and SPVDD=3.6V.

DAC

Item	Min.	Typ.	Max.	Unit
Resolution		16		Bit
Full scale output voltage		1.5		Vp-p
THD+N (f= 1kHz)			0.5	%
Noise at no signal (A-filter)		-90		dBv
Frequency response (f=50 Hz to 12 kHz)	-0.5		+0.5	dB

Note: T_{OP}=25°C, VDD=3.0V and SPVDD=3.6V.

External dimensions of package



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。寸法値にはバリを含みます。
単位(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions include burr of resin.
UNIT: mm

Note) The surface installed LSI's require special precautions when storing and soldering them.
Please contact the Yamaha dealer for information for proper handling.

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