μPD424102
4,194,304 x 1-Bit
Dynamic CMOS RAM

Description

The μPD424102 is a static-column dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CS}$ low. The data output is returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

Features

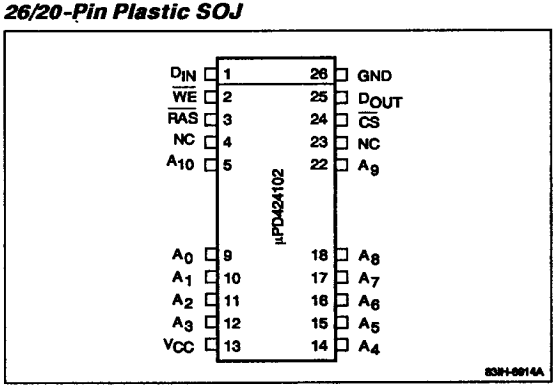
- 4,194,304-word by 1-bit organization
- Single +5-volt power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, or 26/20-pin TSOP plastic packaging

Pin Identification

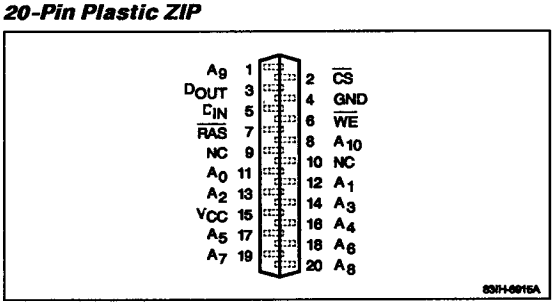
Name	Function
A_0 - A_{10}	Address inputs
$\overline{CS}$	Chip select
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

26/20-Pin Plastic SOJ

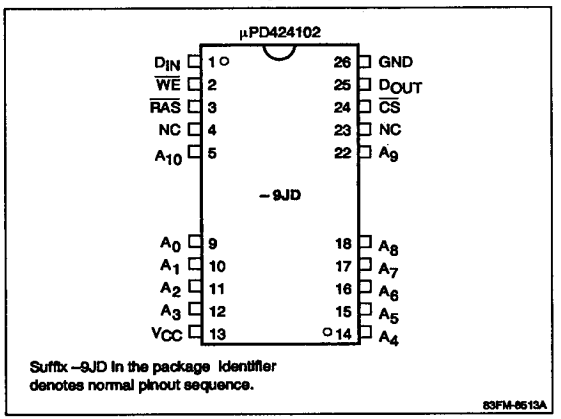


20-Pin Plastic ZIP



Pin Configurations (cont)

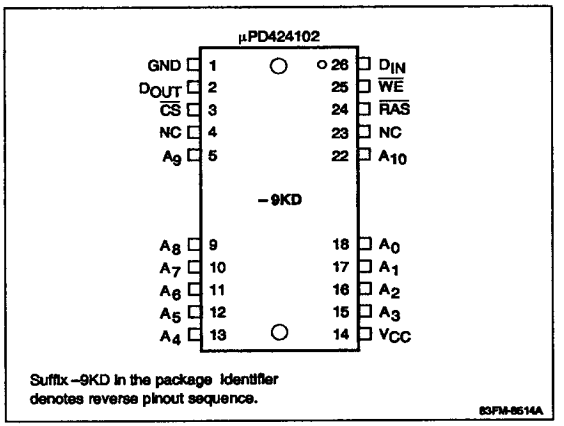
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83FM-8613A

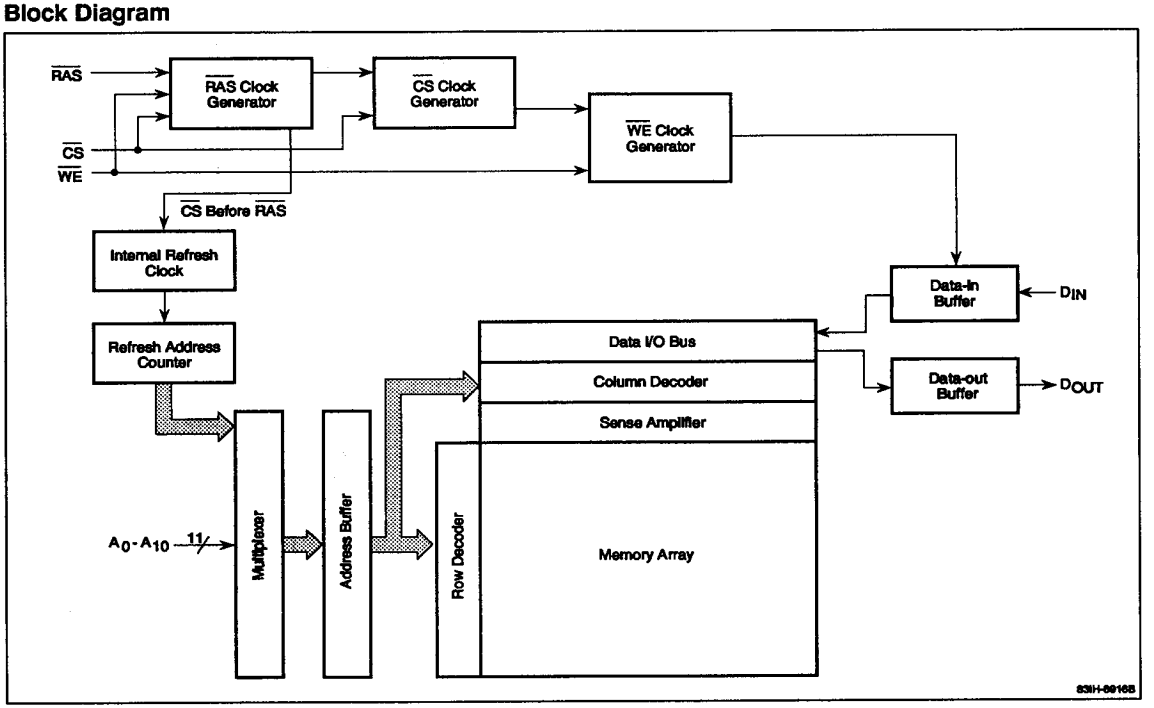
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83FM-8614A

Block Diagram



83IH-86168

Ordering Information

Part Number	RAS Access Time	R/W Cycle Time	Static-Column Cycle Time	Refresh Period	Standby Current	Package
μPD424102LA-60	60 ns	120 ns	35 ns	16 ms	1 mA	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	40 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD424102LA-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
LA-70L	70 ns	140 ns	40 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD424102V-60	60 ns	120 ns	35 ns	16 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD424102V-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
V-70L	70 ns	140 ns	40 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			
μPD424102GS-60	60 ns	120 ns	35 ns	16 ms	1 mA	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns			
GS-80	80 ns	160 ns	50 ns			
GS-10	100 ns	190 ns	60 ns			
μPD424102GS-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
GS-70L	70 ns	140 ns	40 ns			
GS-80L	80 ns	160 ns	50 ns			
GS-10L	100 ns	190 ns	60 ns			
μPD424102GSM-60	60 ns	120 ns	35 ns	16 ms	1 mA	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns			
GSM-80	80 ns	160 ns	50 ns			
GSM-10	100 ns	190 ns	60 ns			
μPD424102GSM-60L	60 ns	120 ns	35 ns	128 ms	300 μA	
GSM-70L	70 ns	140 ns	40 ns			
GSM-80L	80 ns	160 ns	50 ns			
GSM-10L	100 ns	190 ns	60 ns			

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Low-Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	≤ 1 μs	1024 refresh cycles (min) every 128 ms; $\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V or ≤ 0.2 V, as appropriate; D_{OUT} open; all other inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; D_{IN}, $\overline{WE}$, Addresses ≥ V_{CC} − 0.2 V or ≤ 0.2 V; D_{OUT} open
	300	μA	≤ 200 μs		
t_{REF}	128	ms			

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD424102-60		μPD424102-70		μPD424102-80		μPD424102-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		90		80	mA	$\overline{RAS}$ and $\overline{CS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Static column operating current, average	I_{CC4}		70		60		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)

AC Characteristics (cont)

Parameter	Symbol	μPD424102-60		μPD424102-70		μPD424102-80		μPD424102-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 8, 9)
Column address hold time	t_{CAH}	15		15		15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 15)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 14)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$ (rising edge)	t_{OW}		25		25		25		25	ns	
Access time from previous $\overline{WE}$	t_{PWA}		60		70		90		110	ns	(Note 7, 17)

5c

AC Characteristics (cont)

Parameter	Symbol	μPD424102-60		μPD424102-70		μPD424102-80		μPD424102-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time referenced to previous $\overline{WE}$	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
Static-column $\overline{RAS}$ pulse width	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 12)
Read cycle time	t_{RSC}	35		40		50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	145		165		185		220		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Static-column read/write cycle time	t_{RWSC}	65		75		95		115		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)

AC Characteristics (cont)

Parameter	Symbol	μPD424102-60 Min	μPD424102-60 Max	μPD424102-70 Min	μPD424102-70 Max	μPD424102-80 Min	μPD424102-80 Max	μPD424102-10 Min	μPD424102-10 Max	Unit	Test Conditions
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 17)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 15)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Output hold time from $\overline{WE}$	t_{WOH}	0		0		0		0		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 13)
Write cycle time	t_{WSC}	35		40		50		60		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

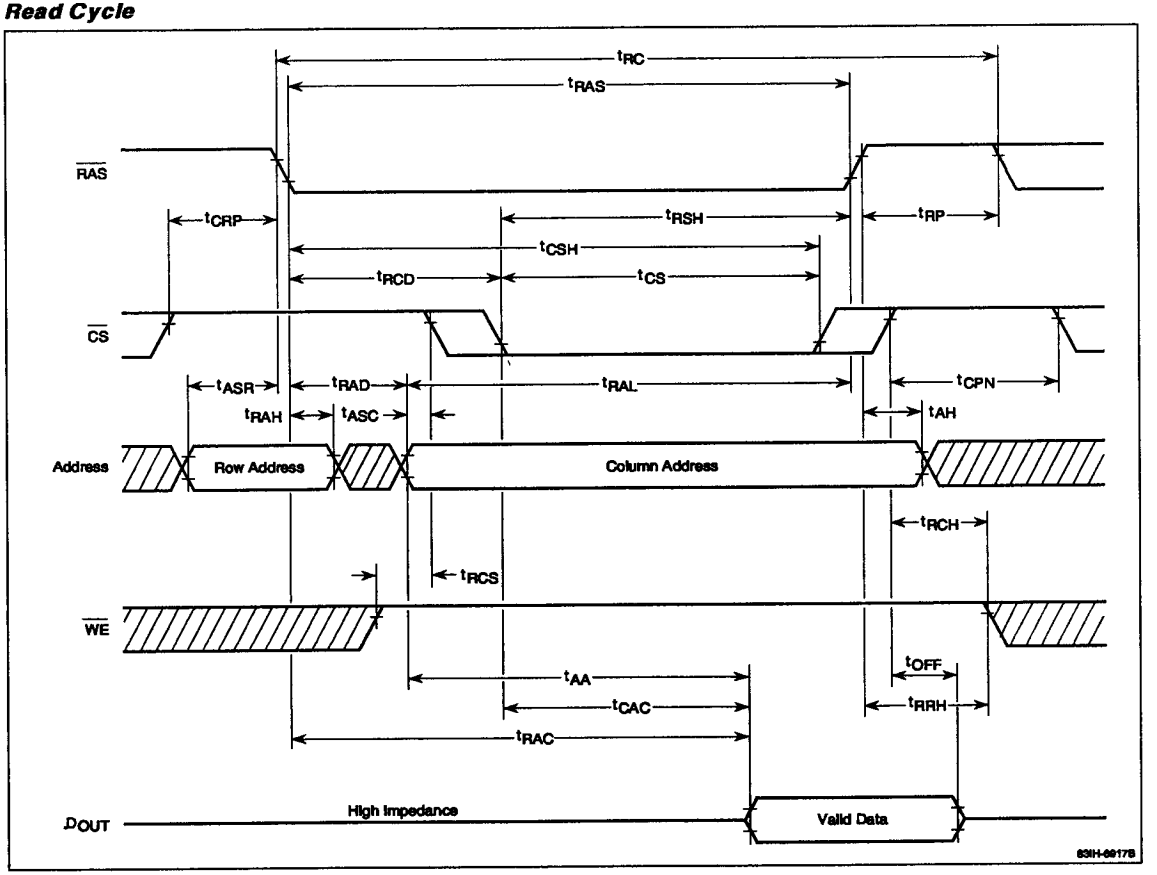
(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes that $t_{WAD} \leq t_{WAD}$ (max).

5c

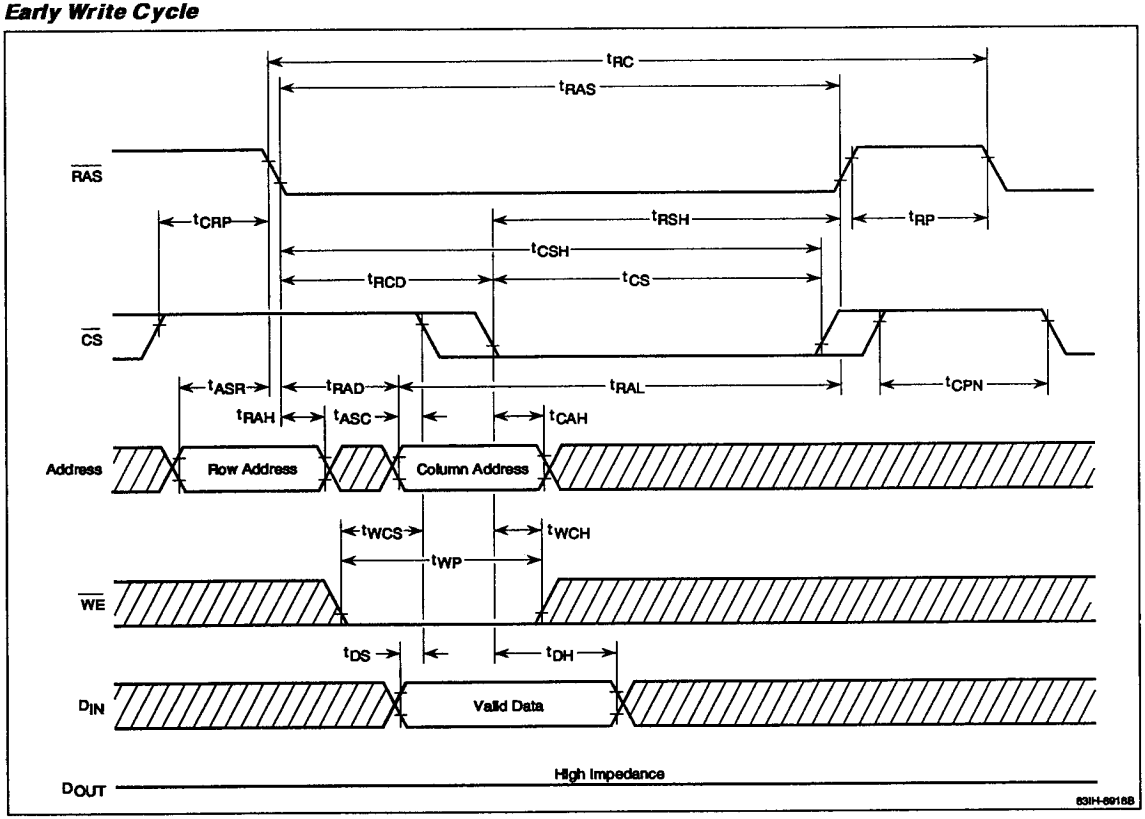
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

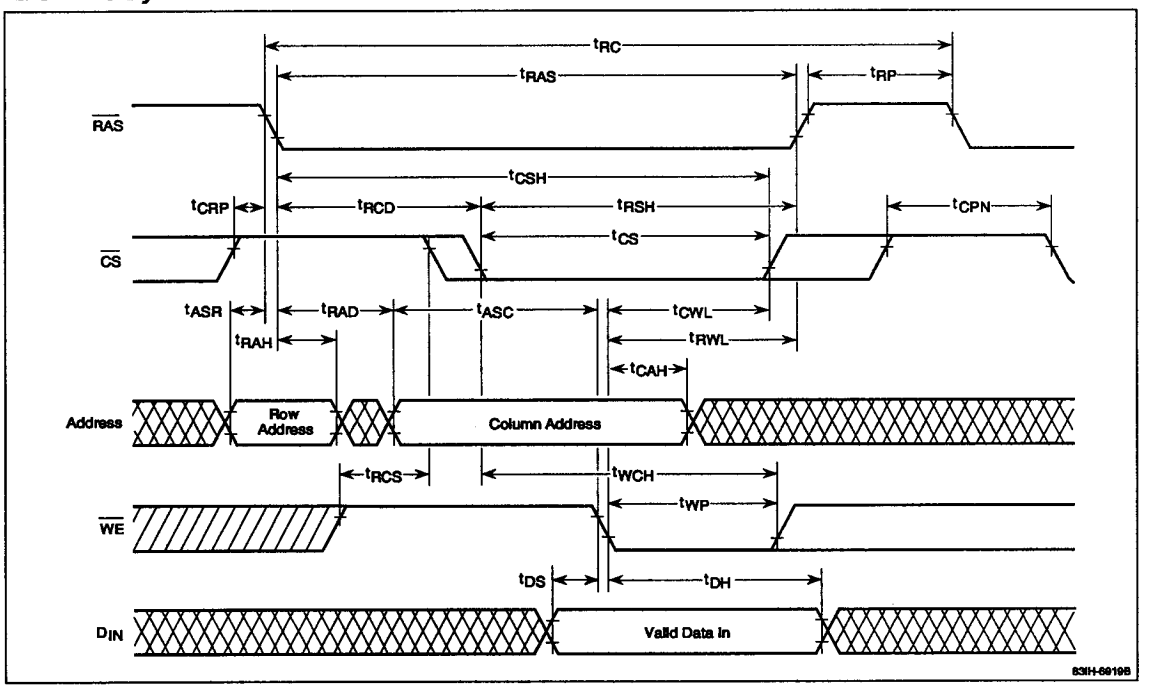
Early Write Cycle



5c

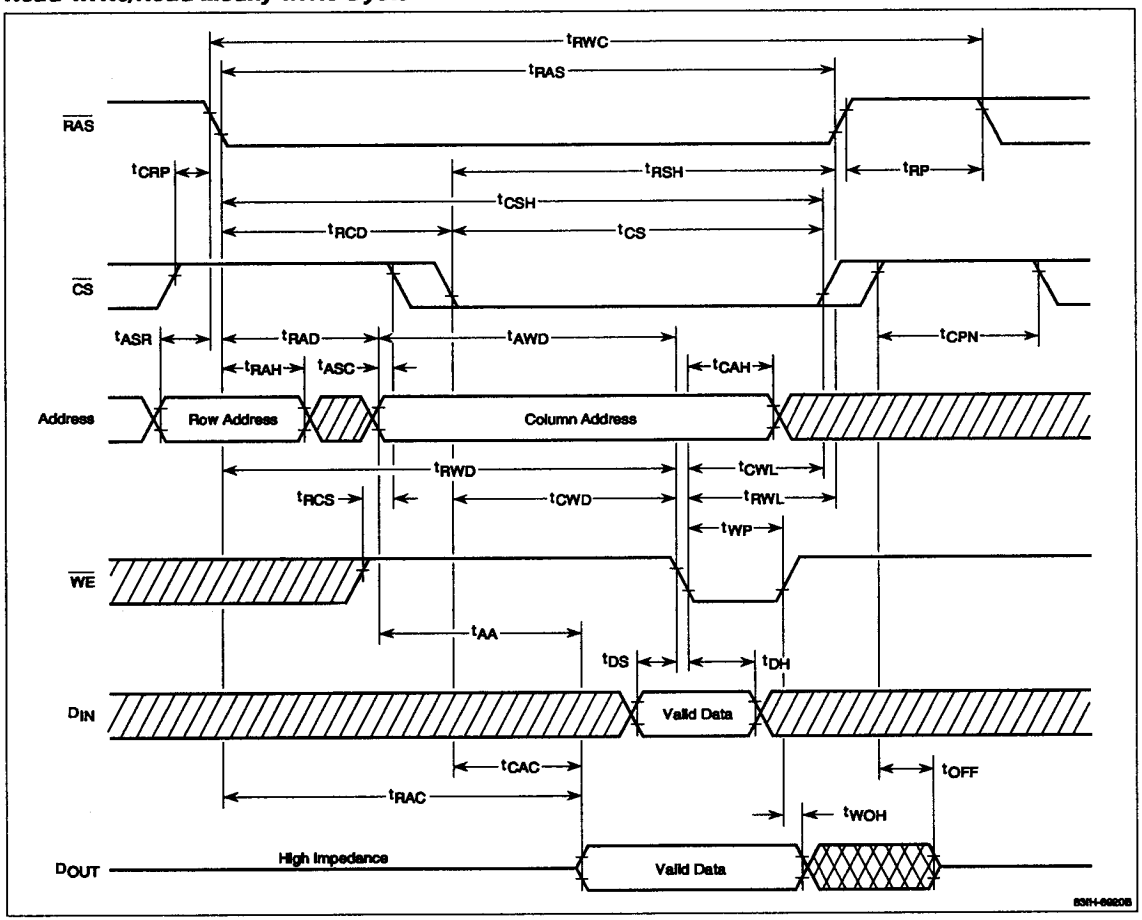
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

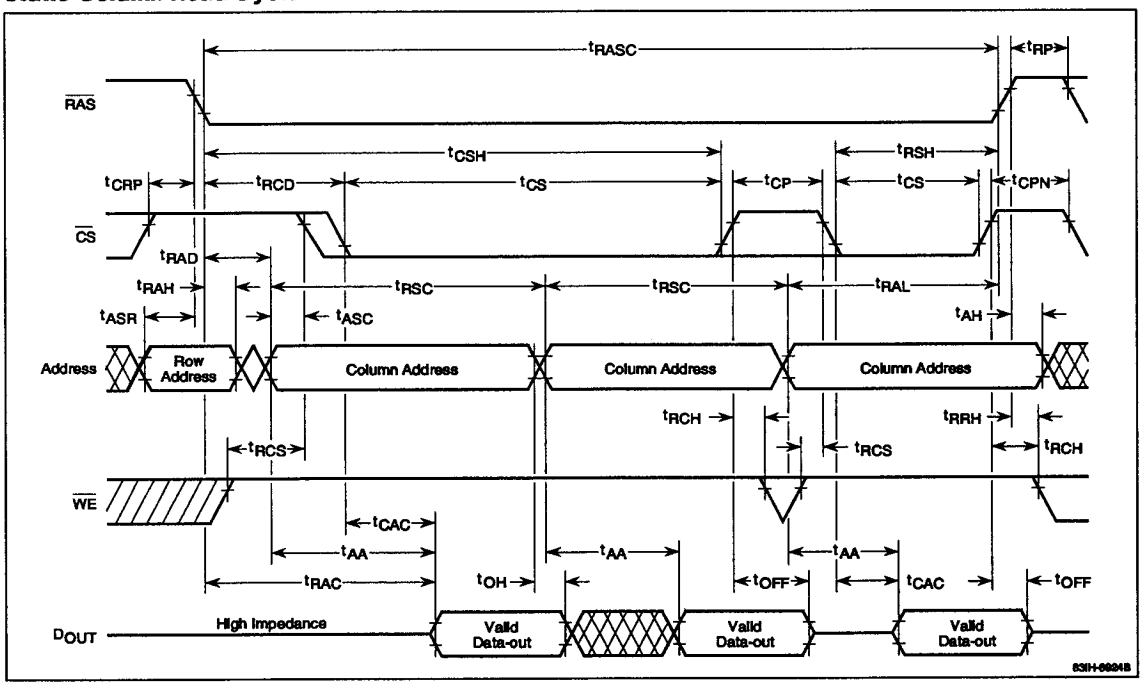
Read-Write/Read-Modify-Write Cycle



5c

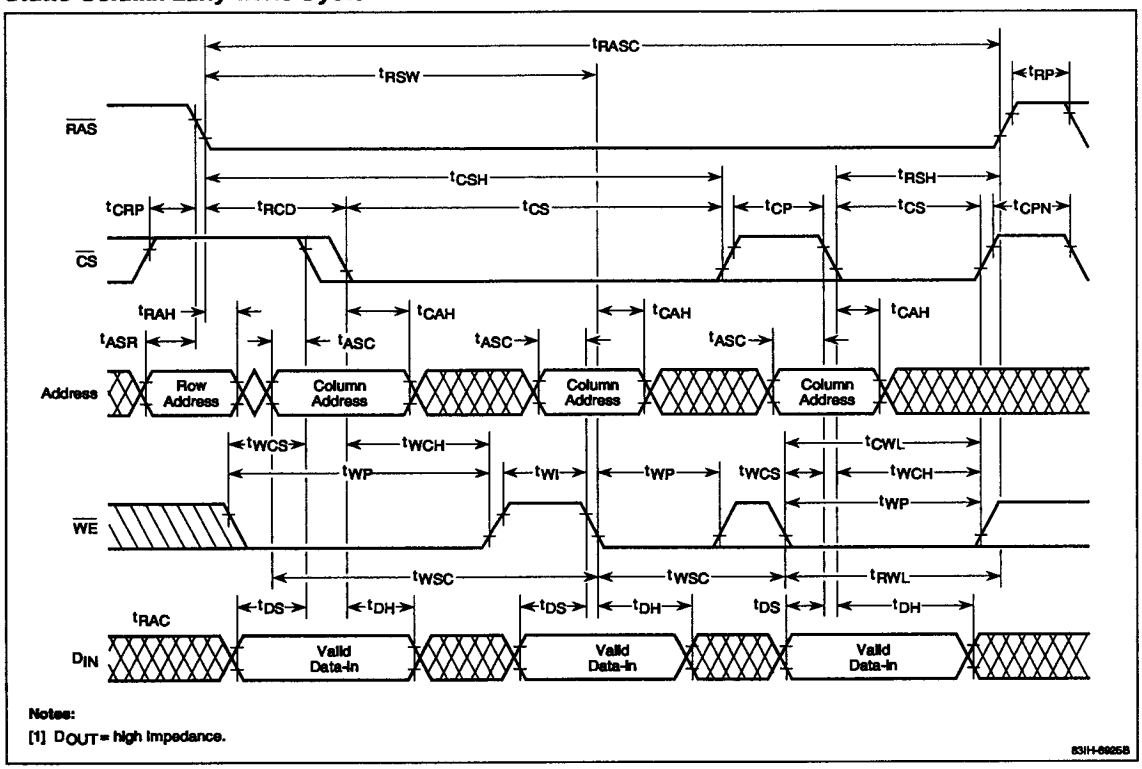
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



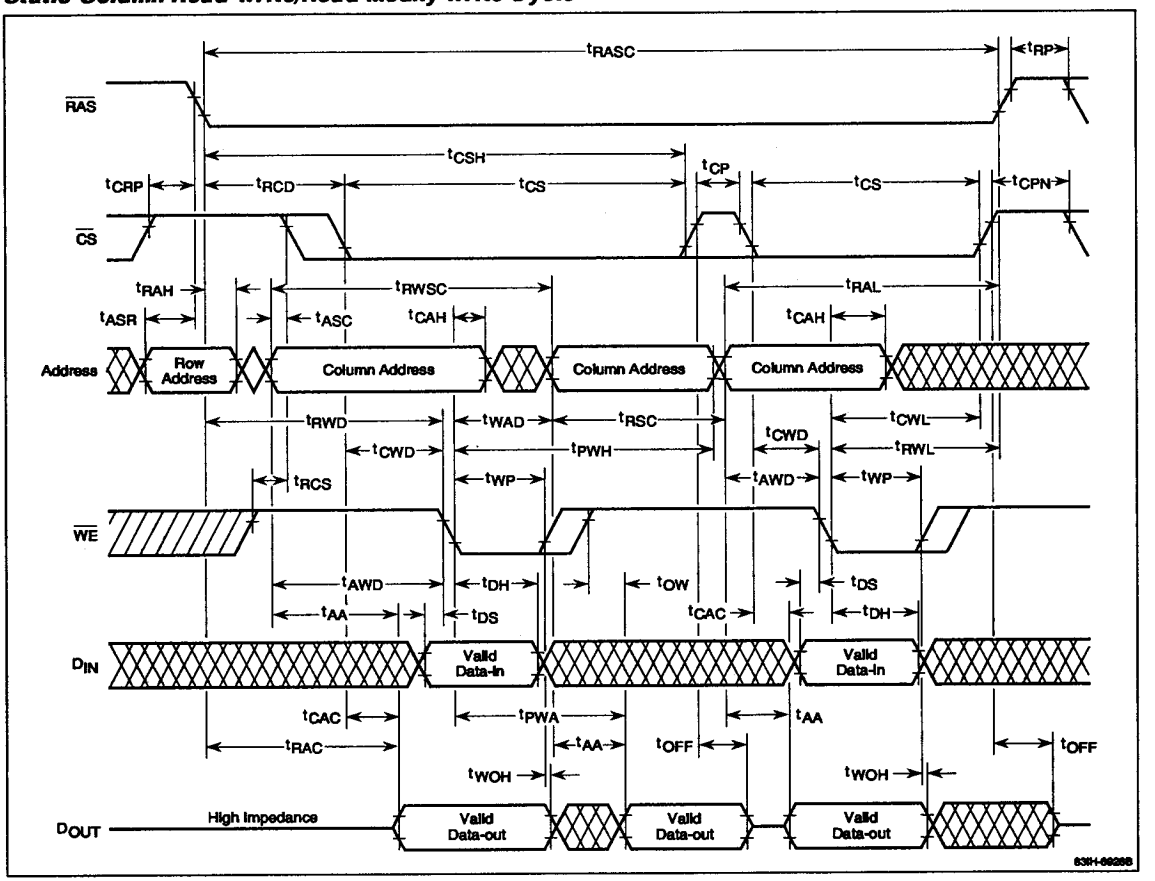
Notes:
[1] D_{OUT} = high impedance.

83IH-6925B

5c

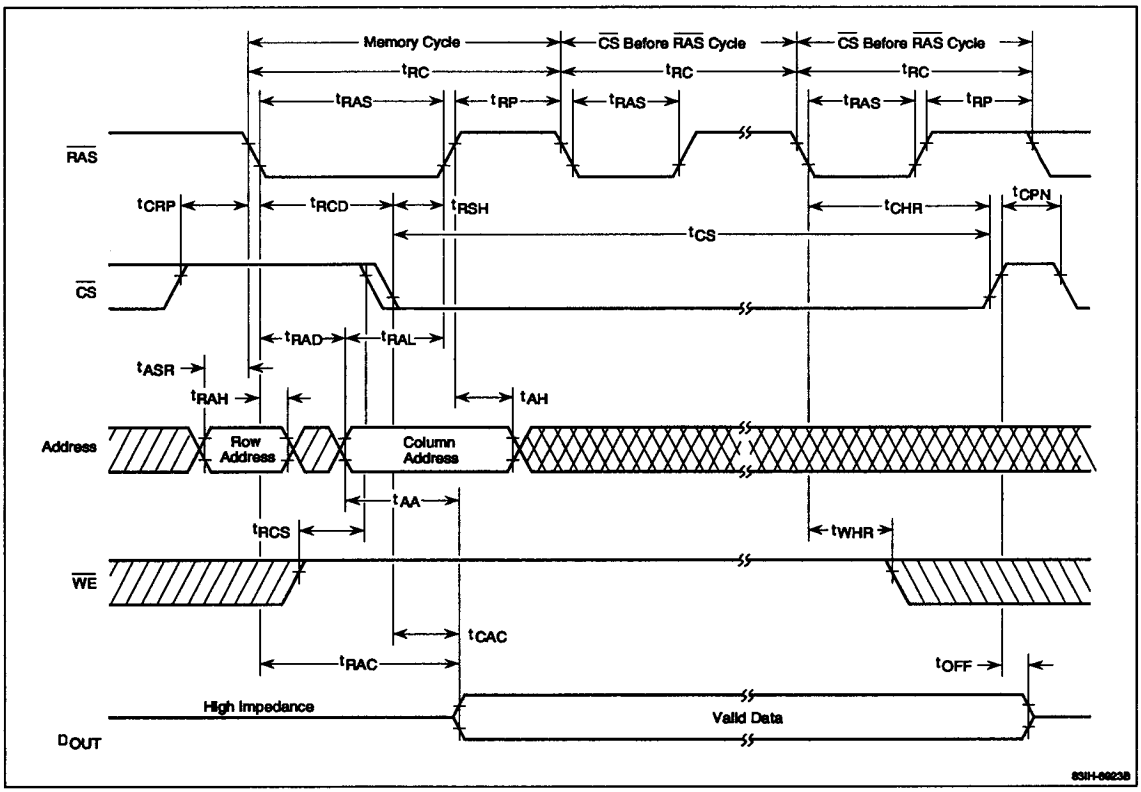
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

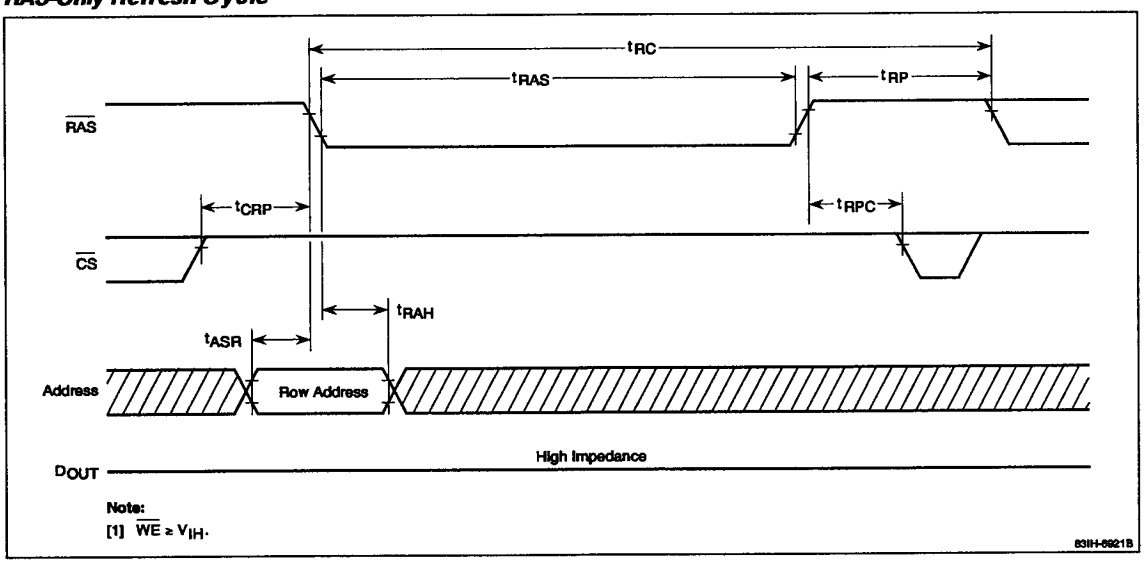
Hidden Refresh Cycle



5c

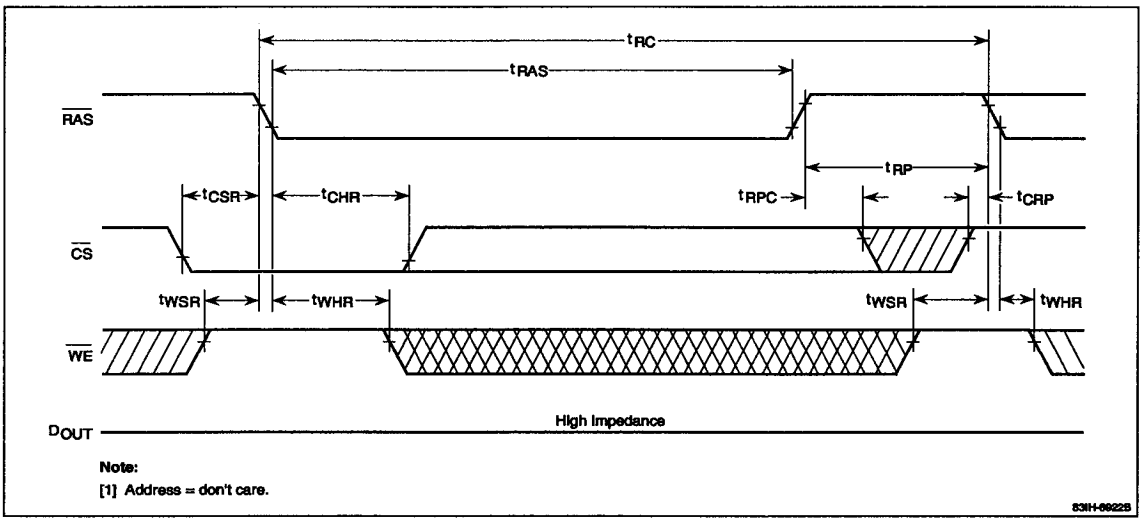
Timing Waveforms (cont)

RAS-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

83H-0922B