

Advance Information

Description

The μPD4216412 and the μPD4217412 are static-column dynamic RAMs with write-per-bit organized as 4,194,304 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by \overline{CS} independent of \overline{RAS} . After a valid read or read-modify-write cycle, data is held on the outputs by maintaining \overline{CS} low. Data outputs return to high impedance when \overline{CS} goes high. Static-column read and write cycles can be executed by cycling \overline{CS} .

Refreshing may be accomplished by means of a \overline{CS} before \overline{RAS} cycle that internally generates the refresh address. Refreshing can also be accomplished by means of \overline{RAS} -only refresh cycles or by normal read or write cycles.

Two versions of the 4,194,304 by 4-bit static-column dynamic RAM with write-per-bit are available. The μPD4216412 version uses 4096 address combinations of $A_0 - A_{11}$ to refresh the memory during a 64-ms refresh period. The μPD4217412 version uses 2048 address combinations of $A_0 - A_{10}$ to refresh the memory during a 32-ms refresh period.

To access the memory during read, write, and read-modify-write cycles, the μPD4216412 uses row address combinations of $A_0 - A_{11}$ and column address combinations of $A_0 - A_9$. The μPD4217412 uses row and column address combinations of $A_0 - A_{10}$.

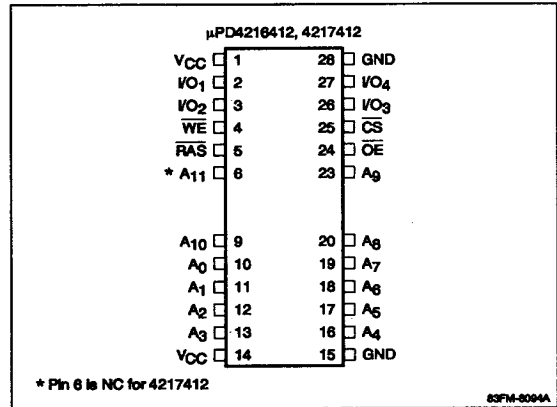
Features

- 4,194,304 by 4-bit organization
- Single +5-volt power supply
- Static-column option with write-per-bit
- Low power dissipation
- \overline{CS} before \overline{RAS} refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance

- 4,096 refresh cycles every 64 ms (4216412); 2048 refresh cycles every 32 ms (4217412)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

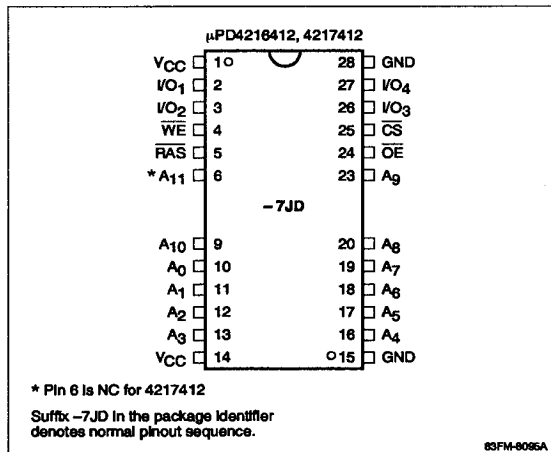
28/24-Pin Plastic SOJ



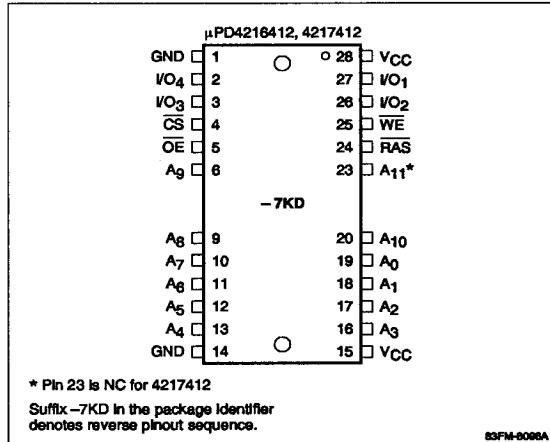
μPD4216412, 4217412

Pin Configurations (cont)

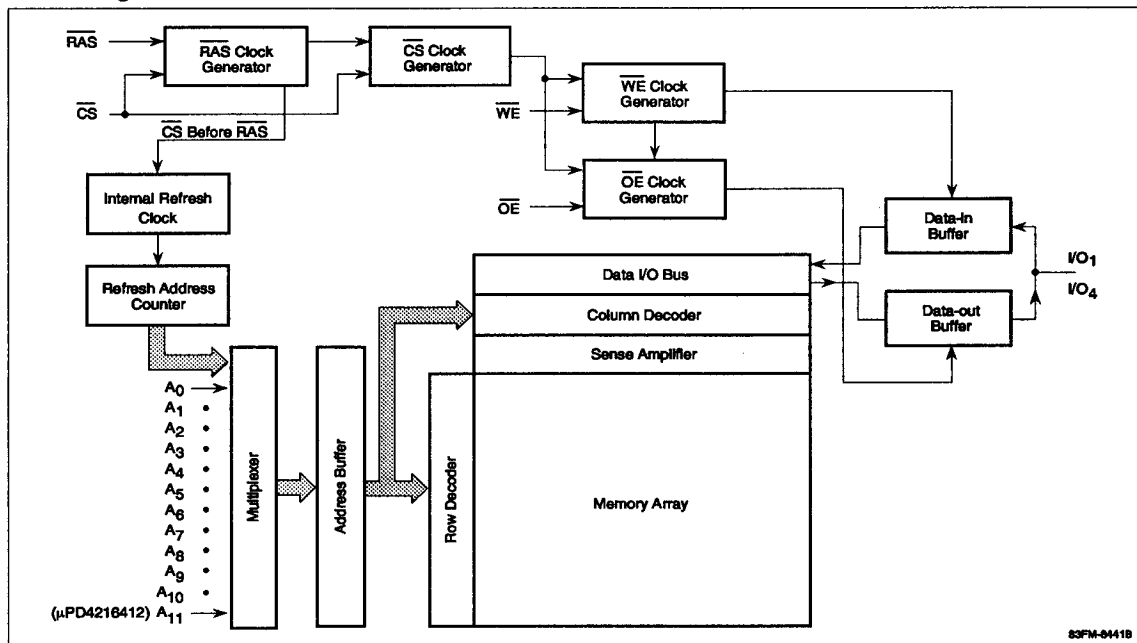
28/24-Pin Plastic TSOP (Normal Pinouts)



28/24-Pin Plastic TSOP (Reverse Pinouts)



Block Diagram



Ordering Information, μPD4216412 (4096 refresh cycles)

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD4216412LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216412V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216412G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216412G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Ordering Information, μPD4217412 (2048 refresh cycles)

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD4217412LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217412V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217412G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217412G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	