

16 Mbit (x8/x16) Concurrent SuperFlash

SST36VF1601G / SST36VF1602G



Data Sheet

FEATURES:

- **Organized as 1M x16 or 2M x8**
- **Dual Bank Architecture for Concurrent Read/Write Operation**
 - 16 Mbit Bottom Sector Protection
 - SST36VF1601G: 4 Mbit + 12 Mbit
 - 16 Mbit Top Sector Protection
 - SST36VF1602G: 12 Mbit + 4 Mbit
- **Single 2.7-3.6V for Read and Write Operations**
- **Superior Reliability**
 - Endurance: 100,000 cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption:**
 - Active Current: 6 mA typical
 - Standby Current: 4 μ A typical
 - Auto Low Power Mode: 4 μ A typical
- **Hardware Sector Protection/WP# Input Pin**
 - Protects the 4 outermost sectors (8 KWord) in the smaller bank by driving WP# low and unprotects by driving WP# high
- **Hardware Reset Pin (RST#)**
 - Resets the internal state machine to reading array data
- **Byte# Pin**
 - Selects 8-bit or 16-bit mode
- **Sector-Erase Capability**
 - Uniform 2 KWord sectors
- **Chip-Erase Capability**
- **Block-Erase Capability**
 - Uniform 32 KWord blocks
- **Erase-Suspend / Erase-Resume Capabilities**
- **Security ID Feature**
 - SST: 128 bits
 - User: 256 Byte
- **Fast Read Access Time**
 - 70 ns
- **Latched Address and Data**
- **Fast Erase and Program (typical):**
 - Sector-Erase Time: 18 ms
 - Block-Erase Time: 18 ms
 - Chip-Erase Time: 35 ms
 - Program Time: 7 μ s
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End-of-Write Detection**
 - Toggle Bit
 - Data# Polling
 - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **Conforms to Common Flash Memory Interface (CFI)**
- **JEDEC Standards**
 - Flash EEPROM Pinouts and command sets
- **Packages Available**
 - 48-ball TFBGA (6mm x 8mm)
 - 48-lead TSOP (12mm x 20mm)
 - 56-ball LFBGA (8mm x 10mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST36VF1601G and SST36VF1602G are 1M x16 or 2M x8 CMOS Concurrent Read/Write Flash Memory manufactured with SST proprietary, high performance CMOS SuperFlash memory technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The devices write (Program or Erase) with a 2.7-3.6V power supply and conform to JEDEC standard pinouts for x8/x16 memories.

Featuring high performance Program, the SST36VF160xG provide a typical Program time of 7 μ sec and use Toggle Bit, Data# Polling, or RY/BY# to detect the completion of the Program or Erase operation. To protect against inadvertent write, the devices have on-chip hardware and Software Data Protection schemes. Designed, manufactured,

and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

These devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST36VF160xG significantly improve performance and reliability, while lowering power consumption. These devices inherently use less energy during Erase and Program than alternative flash technologies, because the total energy consumed is a function of the applied voltage, current, and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time; therefore, the total energy consumed during any Erase or Program operation is less than alternative flash technologies.



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SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high-density, surface-mount requirements, the SST36VF1601G and SST36VF1602G devices are offered in 48-ball TFBGA, 48-lead TSOP, and 56-ball LFBGA packages. See Figures 6, 7, and 8 for pin assignments.

Device Operation

Memory operation functions are initiated using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Auto Low Power Mode

These devices also have the **Auto Lower Power** mode which puts them in a near-standby mode within 500 ns after data has been accessed with a valid Read operation. This reduces the typical I_{DD} active Read current to 4 µA. While CE# is low, the devices exit Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty.

Concurrent Read/Write Operation

The dual bank architecture of these devices allows the Concurrent Read/Write operation whereby the user can read from one bank while programming or erasing in the other bank. For example, reading system code in one bank while updating data in the other bank. See Table 1 below for more information.

TABLE 1: Concurrent Read/Write State

| Bank 1 | Bank 2 |
|--------------|--------------|
| Read | No Operation |
| Read | Write |
| Write | Read |
| Write | No Operation |
| No Operation | Read |
| No Operation | Write |

Note: For the purposes of this table, write means to perform Block- or Sector-Erase or Program operations as applicable to the appropriate bank.

The Read operation of the SST36VF160xG is controlled by CE# and OE#, both of which have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high impedance state when either CE# or OE# is high. Refer to Figure 9, the Read cycle timing diagram, for further details.

Program Operation

These devices are programmed on a word-by-word or byte-by-byte basis depending on the state of the BYTE# pin. Before programming, ensure that the sector which is being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Initiate Software Data Protection using the three-byte load sequence.
2. Load address and data.

During the Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first.

3. Initiate the internal Program operation after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed typically within 7 µs.

See Figures 10 and 11 for WE# and CE# controlled Program operation timing diagrams and Figure 25 for flow-charts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.



Sector-Erase/Block-Erase Operation

The Sector- or Block- Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST36VF160xG offer both Sector-Erase and Block-Erase operations.

The sector architecture is based on a uniform sector size of 2 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (50H) and sector address (SA) in the last bus cycle.

The Block-Erase mode is based on a uniform block size of 32 KWord. Block-Erase is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (50H or 30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse.

Any commands issued during the Sector- or Block-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 15 and 16 for timing waveforms.

Chip-Erase Operation

The SST36VF1601G and SST36VF1602G provide a Chip-Erase operation, which erases the entire memory array to the '1' state. This operation is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid Read is Toggle Bit or Data# Polling. Any commands issued during the Chip-Erase operation are ignored. See Table 6 for the command sequence, Figure 14 for timing diagram, and Figure 29 for the flowchart. When WP# is low, any attempt to Chip-Erase will be ignored.

Erase-Suspend/Erase-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read or programmed into any sector or block that is not engaged in an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode no more than 10 μ s after the Erase-Suspend command had been issued. (T_{ES} maximum latency equals 10 μ s.) Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ₂ toggling and DQ₆ at '1'. While in Erase-Suspend mode, a Program operation is allowed except for the sector or block selected for Erase-Suspend.

To resume a suspended Sector-Erase or Block-Erase operation, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the one-byte sequence.

Write Operation Status Detection

To optimize the system Write cycle time, the SST36VF160xG provide two software means to detect the completion of a Write (Program or Erase) cycle. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system. Therefore, Data# Polling or Toggle Bit maybe be read concurrent with the completion of the write cycle. If this occurs, the system may possibly get an incorrect result from the status detection process. For example, valid data may appear to conflict with either DQ₇ or DQ₆. To prevent false results, upon detection of failures, the software routine should loop to read the accessed location an additional two times. If both reads are valid, then the device has completed the Write cycle, otherwise the failure is valid.



Ready/Busy# (RY/BY#)

The SST36VF160xG include a Ready/Busy# (RY/BY#) output signal. RY/BY# is an open drain output pin that indicates whether an Erase or Program operation is in progress. Since RY/BY# is an open drain output, it allows several devices to be tied in parallel to V_{DD} via an external pull-up resistor. After the rising edge of the final WE# pulse in the command sequence, the RY/BY# status is valid.

When RY/BY# is actively pulled low, it indicates that an Erase or Program operation is in progress. When RY/BY# is high (Ready), the devices may be read or left in standby mode.

Byte/Word (BYTE#)

The device includes a BYTE# pin to control whether the device data I/O pins operate x8 or x16. If the BYTE# pin is at logic "1" (V_{IH}) the device is in x16 data configuration: all data I/O pins DQ₀-DQ₁₅ are active and controlled by CE# and OE#.

If the BYTE# pin is at logic '0', the device is in x8 data configuration -- only data I/O pins DQ₀-DQ₇ are active and controlled by CE# and OE#. The remaining data pins DQ₈-DQ₁₄ are at Hi-Z, while pin DQ₁₅ is used as the address input A₋₁ for the Least Significant Bit of the address bus.

Data# Polling (DQ₇)

When the SST36VF160xG are in an internal Program operation, any attempt to read DQ₇ will produce the complement of true data. Once the Program operation is completed, DQ₇ will produce valid data.

During internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 12 for Data# Polling (DQ₇) timing diagram and Figure 26 for a flowchart.

Toggle Bits (DQ₆ and DQ₂)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating '1's and '0's, i.e., toggling between '1' and '0'. When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling, and the device is then ready for the next operation. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ₆) is valid after the rising edge of sixth WE# (or CE#) pulse. DQ₆ will be set to '1' if a Read operation is attempted on an Erase-Suspended Sector or Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ₆ will toggle.

An additional Toggle Bit is available on DQ₂, which can be used in conjunction with DQ₆ to check whether a particular sector or block is being actively erased or erase-suspended. Table 2 shows detailed bit status information. The Toggle Bit (DQ₂) is valid after the rising edge of the last WE# (or CE#) pulse of Write operation. See Figure 13 for Toggle Bit timing diagram and Figure 26 for a flowchart.

TABLE 2: Write Operation Status

| Status | | DQ ₇ | DQ ₆ | DQ ₂ | RY/BY# |
|--------------------|--|-------------------|-----------------|-----------------|--------|
| Normal Operation | Standard Program | DQ ₇ # | Toggle | No Toggle | 0 |
| | Standard Erase | 0 | Toggle | Toggle | 0 |
| Erase-Suspend Mode | Read From Erase Suspended Sector/Block | 1 | 1 | Toggle | 1 |
| | Read From Non-Erase Suspended Sector/Block | Data | Data | Data | 1 |
| | Program | DQ ₇ # | Toggle | N/A | 0 |

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Note: DQ₇, DQ₆, and DQ₂ require a valid address when reading status information. The address must be in the bank where the operation is in progress in order to read the operation status. If the address is pointing to a different bank (not busy), the device will output array data.



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Data Protection

The SST36VF160xG provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST36VF1601G and SST36VF1602G provide hardware block protection which protects the outermost 8 KWord in the smaller bank. The block is protected when WP# is held low. See Figures 2, 3, 4, and 5 for Block-Protection location.

Block protection is disabled by driving WP# high. This allows data to be erased or programmed into the protected sectors. WP# must be held high prior to issuing the Write command and remain stable until after the entire Write operation has completed. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the devices to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place. See Figures 22 and 21 for more information.

The interrupted Erase or Program operation must be re-initiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST36VF160xG devices implement the JEDEC approved Software Data Protection (SDP) scheme for all data alteration operations, such as Program and Erase. These devices are shipped with the Software Data Protection permanently enabled. See Table 6 for the specific software command codes.

All Program operations require the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations. SDP for Erase operations is similar to Program, but a six-byte load sequence is required for Erase operations.

During SDP command sequence, invalid commands will abort the device to read mode within T_{RC}. The contents of DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

Common Flash Memory Interface (CFI)

These devices contain Common Flash Memory Interface (CFI) information that describes the characteristics of the device. In order to enter the CFI Query mode, the system must write a three-byte sequence, using the CFI Query command, to address BKx555H in the last byte sequence. The system can also use the one-byte sequence with address BKx55H and Data Bus 98H to enter this mode. See Figure 18 for CFI Entry and Read timing diagram. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 7 through 9.

The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Security ID

The SST36VF160xG offer a 136-word Security ID space. The Secure ID space is divided into two segments — one 128-bit, factory-programmed, segment and one 256-Byte, user programmed segment. The first segment is programmed and locked at SST and contains a 128 bit Unique ID which uniquely identifies the device. The user segment is left un-programmed for the customer to program as desired.

The user segment of the Security ID can be programmed using the Security ID Program command. End-of-Write status is checked by reading the toggle bits. Data# Polling is not used for Security ID End-of-Write detection.

Once the programming is complete, lock the Sec ID by issuing the User Sec ID Program Lock-Out command. Locking the Sec ID disables any corruption of this space. Note that regardless of whether or not the Sec ID is locked, the Sec ID segments can not be erased.

The Secure ID space can be queried by executing a three-byte command sequence with Query Sec ID command (88H) at address 555H in the last byte sequence. See Figure 20 for timing diagram. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 6 for more details.



Product Identification

The Product Identification mode identifies the devices as SST36VF1601G or SST36VF1602G and the manufacturer as SST. For details, see Table 3 for software operation, Figure 17 for the Software ID Entry and Read timing diagram, and Figure 27 for the Software ID Entry command sequence flowchart.

The addresses A_{19} and A_{18} indicate a bank address. When the addressed bank is switched to Product Identification mode, it is possible to read another address from the same bank without issuing a new Software ID Entry command.

Product Identification Mode Exit/CFI Mode Exit

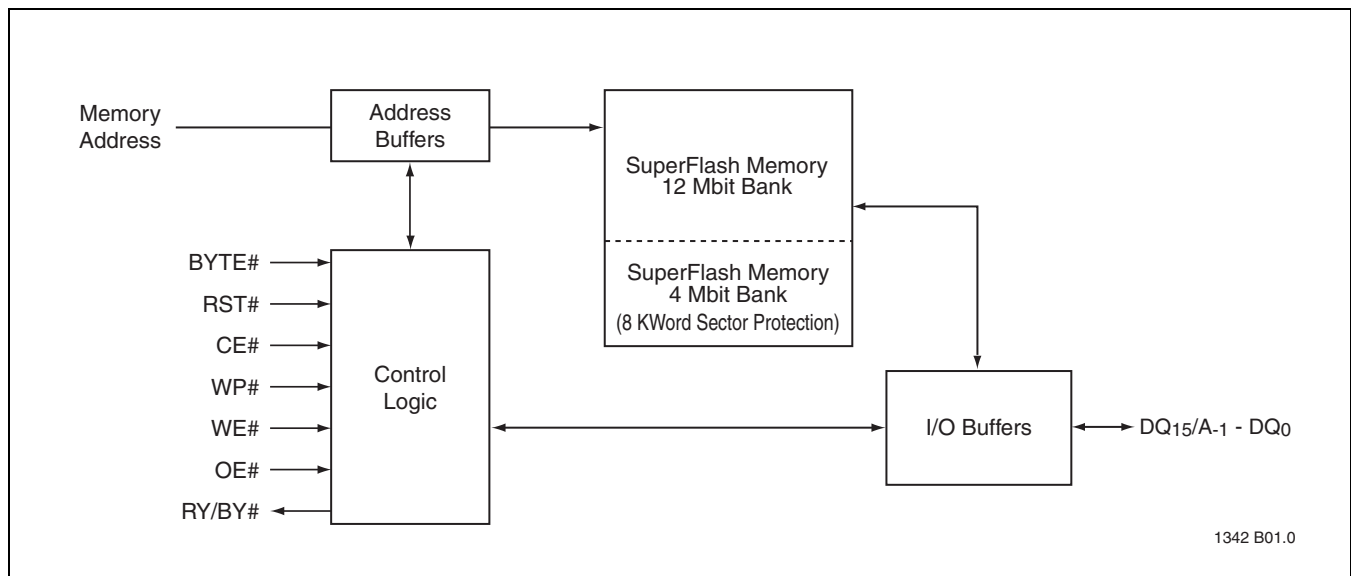
In order to return to the standard Read mode, the Software Product Identification mode must be exited. The exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that causes the device to behave abnormally. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 6 for the software command code, Figure 19 for timing waveform and Figure 28 for a flowchart.

TABLE 3: Product Identification

| | Address | Data |
|-------------------|---------|-------|
| Manufacturer's ID | BK0000H | 00BFH |
| Device ID | | |
| SST36VF1601G | BK0001H | 7343H |
| SST36VF1602G | BK0001H | 7344H |

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Note: BK = Bank Address (A_{19} - A_{18})



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FIGURE 1: Functional Block Diagram

Bottom Sector Protection; 32 KWord Blocks; 2 KWord Sectors

| | | |
|--------|----------|--------|
| FFFFFH | Block 31 | Bank 2 |
| F8000H | | |
| F7FFFH | Block 30 | |
| F0000H | | |
| FFFFFH | Block 29 | |
| E8000H | | |
| E7FFFH | Block 28 | |
| E0000H | | |
| FFFFFH | Block 27 | |
| D8000H | | |
| D7FFFH | Block 26 | |
| D0000H | | |
| FFFFFH | Block 25 | |
| C8000H | | |
| C7FFFH | Block 24 | |
| C0000H | | |
| BFFFFH | Block 23 | |
| B8000H | | |
| B7FFFH | Block 22 | |
| B0000H | | |
| AFFFFH | Block 21 | |
| A8000H | | |
| A7FFFH | Block 20 | |
| A0000H | | |
| 9FFFFH | Block 19 | |
| 98000H | | |
| 97FFFH | Block 18 | |
| 90000H | | |
| 8FFFFH | Block 17 | |
| 88000H | | |
| 87FFFH | Block 16 | |
| 80000H | | |
| 7FFFFH | Block 15 | |
| 78000H | | |
| 77FFFH | Block 14 | |
| 70000H | | |
| 6FFFFH | Block 13 | |
| 68000H | | |
| 67FFFH | Block 12 | |
| 60000H | | |
| 5FFFFH | Block 11 | |
| 58000H | | |
| 57FFFH | Block 10 | |
| 50000H | | |
| 4FFFFH | Block 9 | |
| 48000H | | |
| 47FFFH | Block 8 | |
| 40000H | | |
| 3FFFFH | Block 7 | |
| 38000H | | |
| 37FFFH | Block 6 | |
| 30000H | | |
| 2FFFFH | Block 5 | |
| 28000H | | |
| 27FFFH | Block 4 | |
| 20000H | | |
| 1FFFFH | Block 3 | |
| 18000H | | |
| 17FFFH | Block 2 | |
| 10000H | | |
| 0FFFFH | Block 1 | |
| 08000H | | |
| 07FFFH | Block 0 | |
| 02000H | | |
| 01FFFH | | |
| 00000H | | |

8 KWord Sector Protection
(4-2 KWord Sectors)

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Note: The address input range in x16 mode (BYTE#=V_{IH}) is A₁₉-A₀

FIGURE 2: SST36VF1601G, 1M x16 Concurrent SuperFlash Dual-Bank Memory Organization



Bottom Sector Protection; 64 KByte Blocks; 4 KByte Sectors

| | | | |
|----------------------|----------|--------|--------|
| 1FFFFFFH 1F0000H | Block 31 | Bank 2 | |
| 1EFFFFFFH 1E0000H | Block 30 | | |
| 1DFFFFFFH 1D0000H | Block 29 | | |
| 1CFFFFFFH 1C0000H | Block 28 | | |
| 1BFFFFFFH 1B0000H | Block 27 | | |
| 1AFFFFFFH 1A0000H | Block 26 | | |
| 19FFFFFFH 190000H | Block 25 | | |
| 18FFFFFFH 180000H | Block 24 | | |
| 17FFFFFFH 170000H | Block 23 | | |
| 16FFFFFFH 160000H | Block 22 | | |
| 15FFFFFFH 150000H | Block 21 | | |
| 14FFFFFFH 140000H | Block 20 | | |
| 13FFFFFFH 130000H | Block 19 | | |
| 12FFFFFFH 120000H | Block 18 | | |
| 11FFFFFFH 110000H | Block 17 | | |
| 10FFFFFFH 100000H | Block 16 | | |
| 0FFFFFFFH 0F0000H | Block 15 | | |
| 0EFFFFFFH 0E0000H | Block 14 | | |
| 0DFFFFFFH 0D0000H | Block 13 | | |
| 0CFFFFFFH 0C0000H | Block 12 | | |
| 0BFFFFFFH 0B0000H | Block 11 | | |
| 0AFFFFFFH 0A0000H | Block 10 | | |
| 09FFFFFFH 090000H | Block 9 | | |
| 08FFFFFFH 080000H | Block 8 | | |
| 07FFFFFFH 070000H | Block 7 | | Bank 1 |
| 06FFFFFFH 060000H | Block 6 | | |
| 05FFFFFFH 050000H | Block 5 | | |
| 04FFFFFFH 040000H | Block 4 | | |
| 03FFFFFFH 030000H | Block 3 | | |
| 02FFFFFFH 020000H | Block 2 | | |
| 01FFFFFFH 010000H | Block 1 | | |
| 00FFFFFFH 004000H | Block 0 | | |
| 003FFFFH | | | |
| 000000H | | | |

16 KByte Sector Protection
(4-4 KByte Sectors)

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Note: The address input range in x8 mode (BYTE#=V_{IL}) is A₁₉-A₁

FIGURE 3: SST36VF1601G, 2M x8 Concurrent SuperFlash Dual-Bank Memory Organization

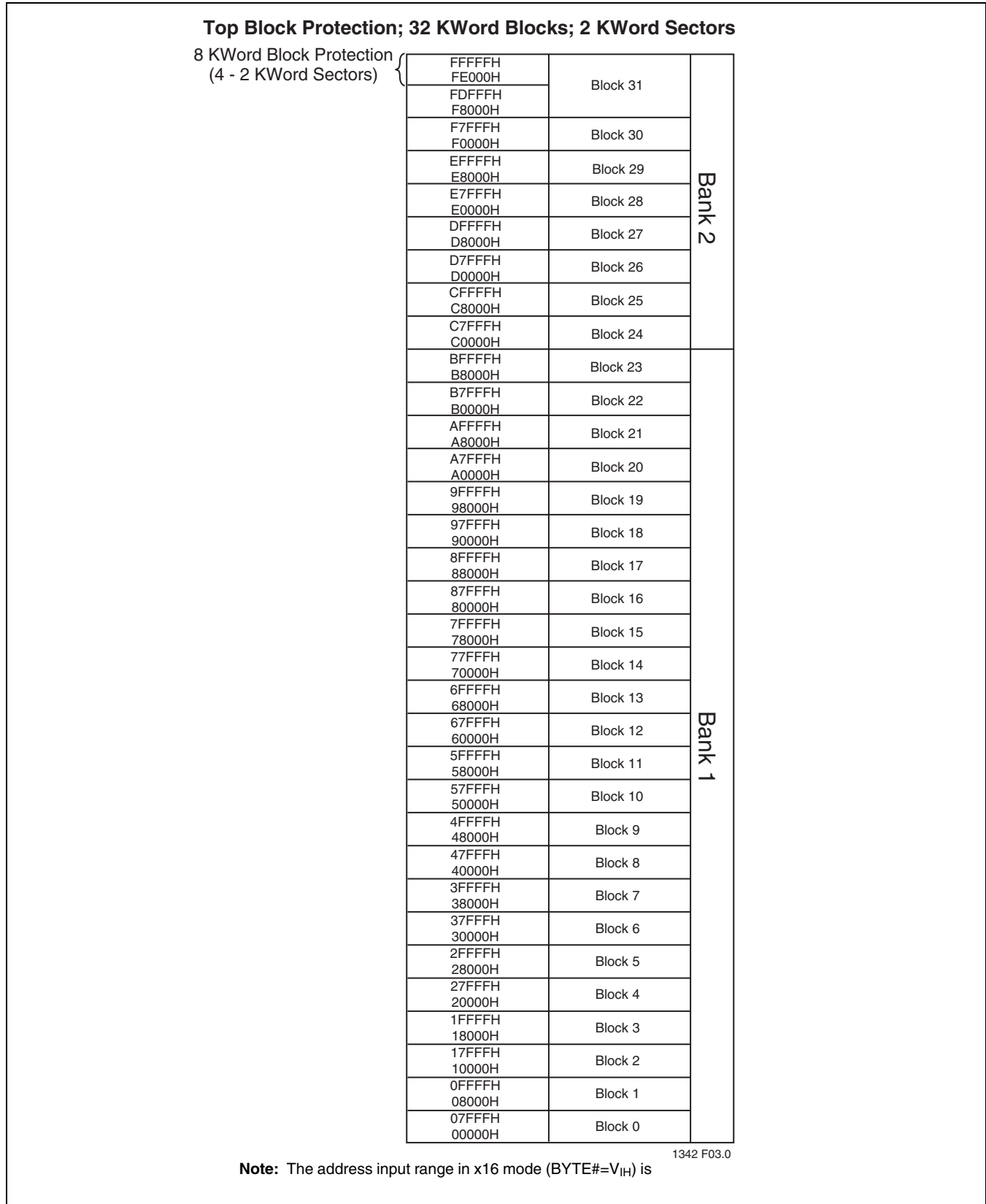


FIGURE 4: SST36VF1602G, 1M x16 Concurrent SuperFlash Dual-Bank Memory Organization



Top Block Protection; 64 KByte Blocks; 4 KByte Sectors

16 KByte Block Protection
(4 - 4 KByte Sectors)

| | | |
|---------------------|----------|--------|
| 1FFFFFFH 1FC000H | Block 31 | Bank 2 |
| 1FBFFFFH 1F0000H | | |
| 1EFFFFH 1E0000H | Block 30 | |
| 1DFFFFH 1D0000H | Block 29 | |
| 1CFFFFH 1C0000H | Block 28 | |
| 1BFFFFH 1B0000H | Block 27 | |
| 1AFFFFH 1A0000H | Block 26 | |
| 19FFFFH 190000H | Block 25 | |
| 18FFFFH 180000H | Block 24 | |
| 17FFFFH 170000H | Block 23 | |
| 16FFFFH 160000H | Block 22 | |
| 15FFFFH 150000H | Block 21 | |
| 14FFFFH 140000H | Block 20 | |
| 13FFFFH 130000H | Block 19 | |
| 12FFFFH 120000H | Block 18 | |
| 11FFFFH 110000H | Block 17 | |
| 10FFFFH 100000H | Block 16 | |
| 0FFFFFH 0F0000H | Block 15 | |
| 0EFFFFH 0E0000H | Block 14 | |
| 0DFFFFH 0D0000H | Block 13 | |
| 0CFFFFH 0C0000H | Block 12 | |
| 0BFFFFH 0B0000H | Block 11 | |
| 0AFFFFH 0A0000H | Block 10 | |
| 09FFFFH 090000H | Block 9 | |
| 08FFFFH 080000H | Block 8 | |
| 07FFFFH 070000H | Block 7 | |
| 06FFFFH 060000H | Block 6 | |
| 05FFFFH 050000H | Block 5 | |
| 04FFFFH 040000H | Block 4 | |
| 03FFFFH 030000H | Block 3 | |
| 02FFFFH 020000H | Block 2 | |
| 01FFFFH 010000H | Block 1 | |
| 00FFFFH 000000H | Block 0 | Bank 1 |

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Note: The address input range in x8 mode (BYTE#=V_{IL}) is A₁₉-A₁

FIGURE 5: SST36VF1602G, 2M x8 Concurrent SuperFlash Dual-Bank Memory Organization

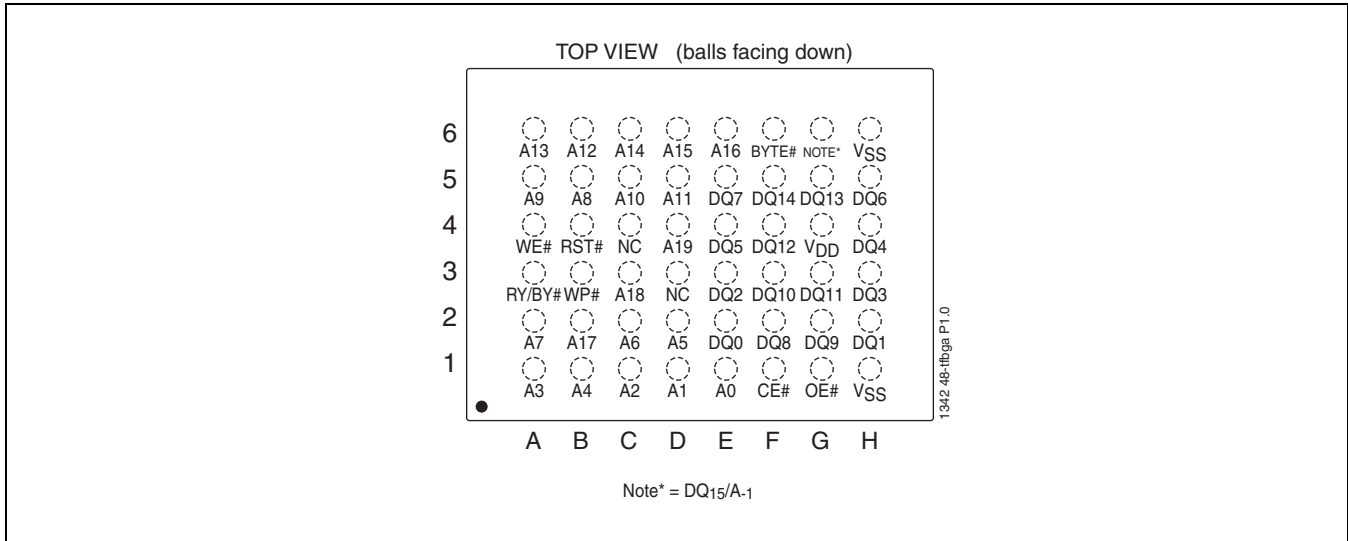


FIGURE 6: Pin Assignments for 48-ball TFBGA (6mm x 8mm)

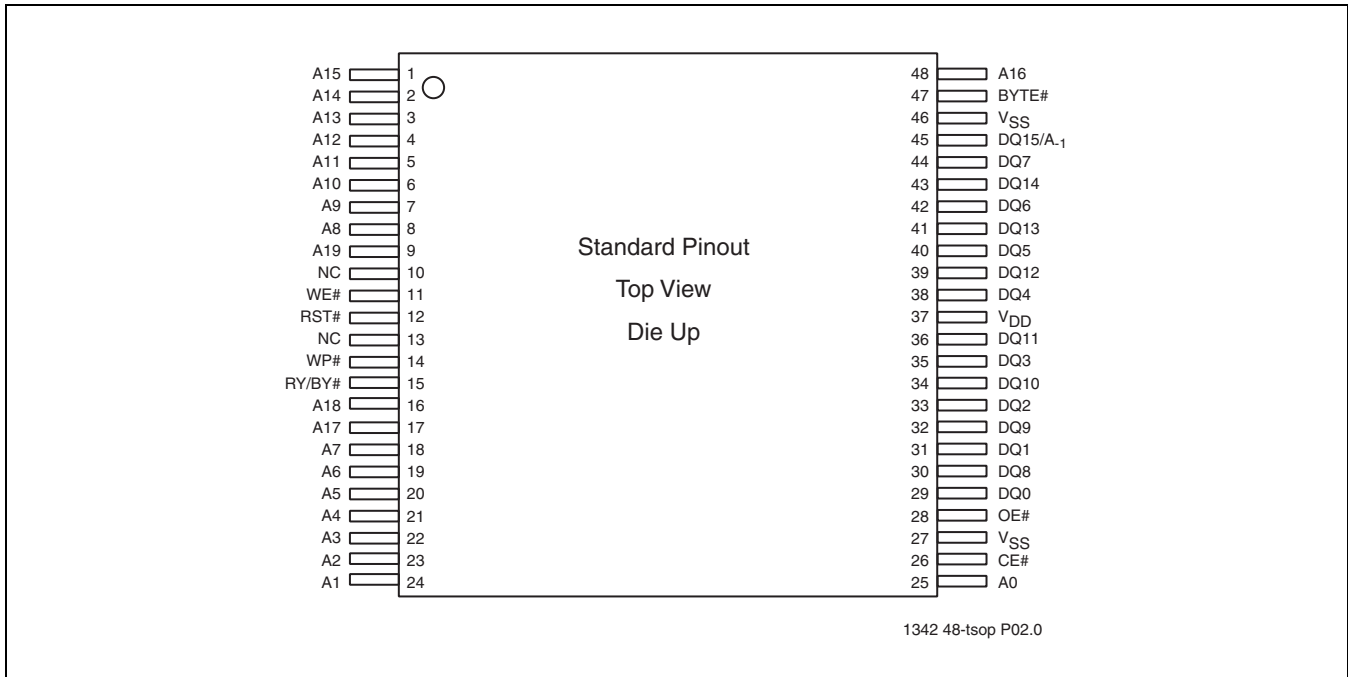


FIGURE 7: Pin Assignments for 48-lead TSOP (12mm x 20mm)



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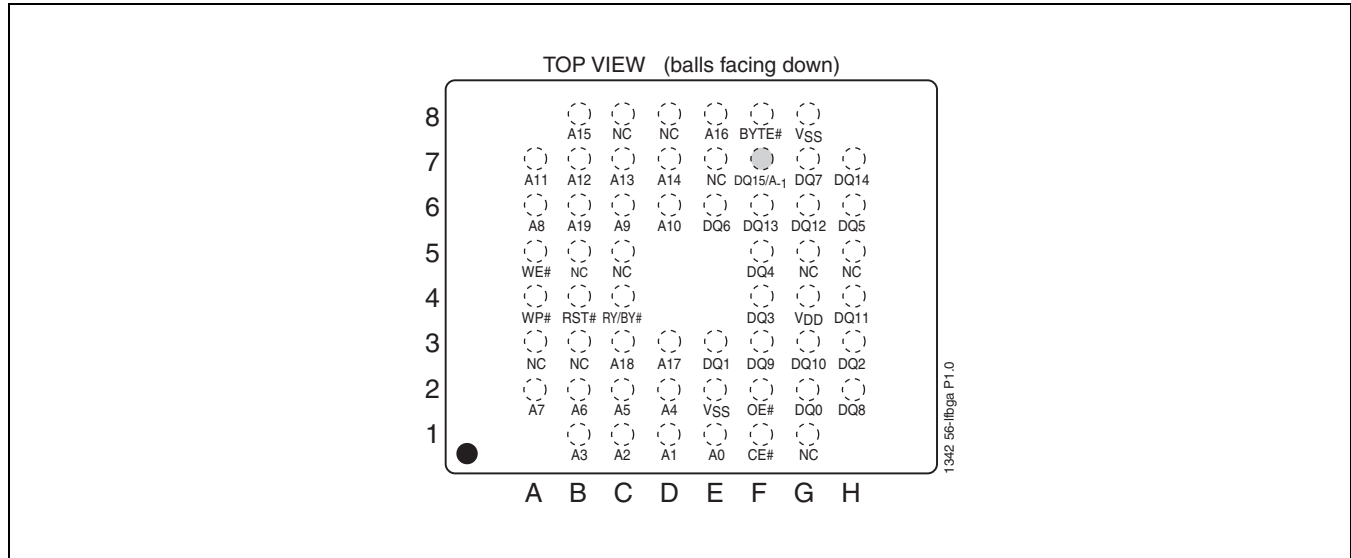


FIGURE 8: Pin Assignments for 56-lead LFBGA (8mm x 10mm)

TABLE 4: Pin Description

| Symbol | Name | Functions |
|-----------------------------------|-----------------------------------|--|
| A ₁₉ -A ₀ | Address Inputs | To provide memory addresses. During Sector-Erase and Hardware Sector Protection, A ₁₉ -A ₁₁ address lines will select the sector. During Block-Erase A ₁₉ -A ₁₅ address lines will select the block. |
| DQ ₁₄ -DQ ₀ | Data Input/Output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high. |
| DQ ₁₅ /A ₋₁ | Data Input/Output and LBS Address | DQ ₁₅ is used as data I/O pin when in x16 mode (BYTE# = "1") A ₋₁ is used as the LSB address pin when in x8 mode (BYTE# = "0") |
| CE# | Chip Enable | To activate the device when CE# is low. |
| OE# | Output Enable | To gate the data output buffers |
| WE# | Write Enable | To control the Write operations |
| RST# | Hardware Reset | To reset and return the device to Read mode |
| RY/BY# | Ready/Busy# | To output the status of a Program or Erase operation RY/BY# is an open drain output, so a 10KΩ - 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read. |
| WP# | Write Protect | To protect and unprotect top or bottom 8 KWord (4 outermost sectors) from Erase or Program operation. |
| BYTE# | Word/Byte Configuration | To select 8-bit or 16-bit mode. |
| V _{DD} | Power Supply | To provide 2.7-3.6V power supply voltage |
| V _{SS} | Ground | |
| NC | No Connection | Unconnected pins |

T4.0 1342

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Data Sheet

TABLE 5: Operation Modes Selection

| Mode ¹ | CE# | OE# | WE# | DQ ₇ -DQ ₀ | DQ ₁₅ -DQ ₈ | | Address |
|---------------------------|------------------|-----------------|-----------------|----------------------------------|-----------------------------------|--|--|
| | | | | | BYTE# = V _{IH} | BYTE# = V _{IL} | |
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} | D _{OUT} | DQ ₁₄ -DQ ₈ = High Z | A _{IN} |
| Program | V _{IL} | V _{IH} | V _{IL} | D _{IN} | D _{IN} | DQ ₁₅ = A ₋₁ | A _{IN} |
| Erase | V _{IL} | V _{IH} | V _{IL} | X ² | X | High Z | Sector or Block address, 555H for Chip-Erase |
| Standby | V _{IHC} | X | X | High Z | High Z | High Z | X |
| Write Inhibit | X | V _{IL} | X | High Z / D _{OUT} | High Z / D _{OUT} | High Z | X |
| | X | X | V _{IH} | High Z / D _{OUT} | High Z / D _{OUT} | High Z | X |
| Product Identification | | | | | | | |
| Software Mode | V _{IL} | V _{IL} | V _{IH} | Manufacturer's ID (BFH) | Manufacturer's ID (00H) | High Z | See Table 6 |
| | | | | Device ID ³ | Device ID ³ | High Z | |

T5.2 1342

1. RST# = V_{IH} for all described operation modes
2. X can be V_{IL} or V_{IH}, but no other value.
3. Device ID =
 SST36VF1601G = 7343H,
 SST36VF1602G = 7344H



TABLE 6: Software Command Sequence

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|--|-------------------------------------|-------------------|---------------------|-------------------|--------------------------------------|-------------------|---------------------|-------------------|---------------------|-------------------|------------------------------|-------------------|
| | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² |
| Program | 555H | AAH | 2AAH | 55H | 555H | A0H | WA ³ | Data | | | | |
| Sector-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | SA _X ⁴ | 50H |
| Block-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BA _X ⁴ | 30H |
| Chip-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| Erase-Suspend | XXXXH | B0H | | | | | | | | | | |
| Erase-Resume | XXXXH | 30H | | | | | | | | | | |
| Query Sec ID ⁵ | 555H | AAH | 2AAH | 55H | 555H | 88H | | | | | | |
| User Security ID Program | 555H | AAH | 2AAH | 55H | 555H | A5H | SIWA ⁶ | Data | | | | |
| User Security ID Program Lock-out ⁷ | 555H | AAH | 2AAH | 55H | 555H | 85H | XXH | 0000H | | | | |
| Software ID Entry ⁸ | 555H | AAH | 2AAH | 55H | BK _X ⁹ 555H | 90H | | | | | | |
| CFI Query Entry | 555H | AAH | 2AAH | 55H | BK _X ⁹ 555H | 98H | | | | | | |
| CFI Query Entry | BK _X ⁹ 55H | 98H | | | | | | | | | | |
| Software ID Exit/ CFI Exit/ Sec ID Exit ^{10,11} | 555H | AAH | 2AAH | 55H | 555H | F0H | | | | | | |
| Software ID Exit/ CFI Exit/ Sec ID Exit ^{10,11} | XXH | F0H | | | | | | | | | | |

T6.0 1342

- Address format A₁₀-A₀ (Hex), Addresses A₁₉-A₁₁ can be V_{IL} or V_{IH}, but no other value, for the command sequence when in x16 mode. When in x8 mode, Addresses A₁₉-A₁₂, Address A₁ and DQ₁₄-DQ₈ can be V_{IL} or V_{IH}, but no other value, for the command sequence.
- DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, for the command sequence
- WA = Program word/byte address
- SA_X for Sector-Erase; uses A₁₉-A₁₁ address lines
BA_X for Block-Erase; uses A₁₉-A₁₅ address lines
- For SST36VF1601G,
SST ID is read with A₃ = 0 (Address range = 00000H to 00007H),
User ID is read with A₃ = 1 (Address range = 00008H to 00087H).
Lock Status is read with A₇-A₀ = 000FFH. Unlocked: DQ₃ = 1 / Locked: DQ₃ = 0.
For SST36VF1602G,
SST ID is read with A₃ = 0 (Address range = C0000H to C0007H),
User ID is read with A₃ = 1 (Address range = C0008H to C0087H).
Lock Status is read with A₇-A₀ = C00FFH. Unlocked: DQ₃ = 1 / Locked: DQ₃ = 0.
- SIWA = User Security ID Program word/byte address
For SST36VF1601G, valid Word-Addresses for User Sec ID are from 00008H to 00087H.
For SST36VF1602G, valid Word-Addresses for User Sec ID are from C0008H to C0087H.
All 4 cycles of User Security ID Program and Program Lock-out must be completed before going back to Read-Array mode.
- The User Security ID Program Lock-out command must be executed in x16 mode (BYTE#=V_{IH}).
- The device does not remain in Software Product Identification mode if powered down.
- A₁₉ and A₁₈ = BK_X (Bank Address): address of the bank that is switched to Software ID/CFI Mode
With A₁₇-A₁ = 0; SST Manufacturer's ID = 00BFH, is read with A₀ = 0
SST36VF1601G Device ID = 7343H, is read with A₀ = 1
SST36VF1602G Device ID = 7344H, is read with A₀ = 1
- Both Software ID Exit operations are equivalent
- If users never lock after programming, User Sec ID can be programmed over the previously unprogrammed bits (data=1) using the User Sec ID mode again (the programmed "0" bits cannot be reversed to "1").
For SST36VF1601G, valid Word-Addresses for User Sec ID are from 00008H to 00087H.
For SST36VF1602G, valid Word-Addresses for User Sec ID are from C0008H to C0087H.



TABLE 7: CFI Query Identification String¹

| Address x16 Mode | Address x8 Mode | Data ² | Description |
|---------------------|--------------------|-------------------------|--|
| 10H 11H 12H | 20H 22H 24H | 0051H 0052H 0059H | Query Unique ASCII string "QRY" |
| 13H 14H | 26H 28H | 0002H 0000H | Primary OEM command set |
| 15H 16H | 2AH 2CH | 0000H 0000H | Address for Primary Extended Table |
| 17H 18H | 2EH 30H | 0000H 0000H | Alternate OEM command set (00H = none exists) |
| 19H 1AH | 32H 34H | 0000H 0000H | Address for Alternate OEM extended Table (00H = none exists) |

T7.0 1342

1. Refer to CFI publication 100 for more details.
2. In x8 mode, only the lower byte of data is output.

TABLE 8: System Interface Information

| Address x16 Mode | Address x8 Mode | Data ¹ | Description |
|---------------------|--------------------|-------------------|--|
| 1BH | 36H | 0027H | V _{DD} Min (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts |
| 1CH | 38H | 0036H | V _{DD} Max (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts |
| 1DH | 3AH | 0000H | V _{PP} min (00H = no V _{PP} pin) |
| 1EH | 3CH | 0000H | V _{PP} max (00H = no V _{PP} pin) |
| 1FH | 3EH | 0004H | Typical time out for Program 2 ^N μs (2 ⁴ = 16 μs) |
| 20H | 40H | 0000H | Typical time out for min size buffer program 2 ^N μs (00H = not supported) |
| 21H | 42H | 0004H | Typical time out for individual Sector/Block-Erase 2 ^N ms (2 ⁴ = 16 ms) |
| 22H | 44H | 0006H | Typical time out for Chip-Erase 2 ^N ms (2 ⁶ = 64 ms) |
| 23H | 46H | 0001H | Maximum time out for Program 2 ^N times typical (2 ¹ x 2 ⁴ = 32 μs) |
| 24H | 48H | 0000H | Maximum time out for buffer program 2 ^N times typical |
| 25H | 4AH | 0001H | Maximum time out for individual Sector-/Block-Erase 2 ^N times typical (2 ¹ x 2 ⁴ = 32 ms) |
| 26H | 4CH | 0001H | Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x 2 ⁶ = 128 ms) |

T8.0 1342

1. In x8 mode, only the lower byte of data is output.



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TABLE 9: Device Geometry Information

| Address x16 Mode | Address x8 Mode | Data ¹ | Description |
|------------------|-----------------|-------------------|---|
| 27H | 4EH | 0015H | Device size = 2^N Bytes (15H = 21; 2^{21} = 2 MByte) |
| 28H | 50H | 0002H | Flash Device Interface description; 0002H = x8/x16 asynchronous interface |
| 29H | 52H | 0000H | |
| 2AH | 54H | 0000H | Maximum number of bytes in multi-byte write = 2^N (00H = not supported) |
| 2BH | 56H | 0000H | |
| 2CH | 58H | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH | 5AH | 00FFH | Sector Information (y + 1 = Number of sectors; z x 256B = sector size) |
| 2EH | 5CH | 0001H | |
| 2FH | 5EH | 0010H | y = 511 + 1 = 512 sectors (01FFH = 512) |
| 30H | 60H | 0000H | |
| 31H | 62H | 001FH | Block Information (y + 1 = Number of blocks; z x 256B = block size) |
| 32H | 64H | 0000H | |
| 33H | 66H | 0000H | y = 31 + 1 = 32 blocks (001FH = 31) |
| 34H | 68H | 0001H | |
| | | | z = 256 x 256 Bytes = 64 KByte/block (0100H = 256) |

T9.1 1342

1. In x8 mode, only the lower byte of data is output.



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Data Sheet

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias -55°C to +125°C
 Storage Temperature -65°C to +150°C
 D. C. Voltage on Any Pin to Ground Potential -0.5V to V_{DD}+0.5V
 Transient Voltage (<20 ns) on Any Pin to Ground Potential -2.0V to V_{DD}+2.0V
 Package Power Dissipation Capability (T_A = 25°C) 1.0W
 Surface Mount Solder Reflow Temperature 260°C for 10 seconds
 Output Short Circuit Current 50 mA

Operating Range:

| Range | Ambient Temp | V _{DD} |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C | 2.7-3.6V |
| Industrial | -40°C to +85°C | 2.7-3.6V |

AC Conditions of Test

| | |
|-----------------------|------------------------|
| Input Rise/Fall Time | 5 ns |
| Output Load | C _L = 30 pF |
| See Figures 23 and 24 | |



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Data Sheet

TABLE 10: DC Operating Characteristics $V_{DD} = 2.7-3.6V$

| Symbol | Parameter | Freq | Limits | | | Test Conditions |
|------------|--|--------------|--------------|---------|---|---------------------------------|
| | | | Min | Max | Units | |
| I_{DD}^1 | Active V_{DD} Current Read | 5 MHz | | 15 | mA | $CE\#=V_{IL}, WE\#=OE\#=V_{IH}$ |
| | | 1 MHz | | 4 | mA | |
| | Program and Erase Concurrent Read/Write | | | 30 | mA | $CE\#=WE\#=V_{IL}, OE\#=V_{IH}$ |
| | | 5 MHz | | 45 | mA | $CE\#=V_{IL}, OE\#=V_{IH}$ |
| | | 1 MHz | | 35 | mA | |
| I_{SB} | Standby V_{DD} Current | | 20 | μA | $CE\#, RST\#=V_{DD}\pm 0.3V$ | |
| I_{ALP} | Auto Low Power V_{DD} Current | | 20 | μA | $CE\#=0.1V, V_{DD}=V_{DD} \text{ Max}$ $WE\#=V_{DD}-0.1V$ Address inputs=0.1V or $V_{DD}-0.1V$ | |
| I_{RT} | Reset V_{DD} Current | | 20 | μA | $RST\#=GND$ | |
| I_{LI} | Input Leakage Current | | 1 | μA | $V_{IN} = GND \text{ to } V_{DD}, V_{DD}=V_{DD} \text{ Max}$ | |
| I_{LIW} | Input Leakage Current on WP# pin and RST# pin | | 10 | μA | $WP\#=GND \text{ to } V_{DD}, V_{DD}=V_{DD} \text{ Max}$ $RST\#=GND \text{ to } V_{DD}, V_{DD}=V_{DD} \text{ Max}$ | |
| I_{LO} | Output Leakage Current | | 1 | μA | $V_{OUT} = GND \text{ to } V_{DD}, V_{DD}=V_{DD} \text{ Max}$ | |
| V_{IL} | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD} \text{ Min}$ | |
| V_{ILC} | Input Low Voltage (CMOS) | | 0.3 | V | $V_{DD}=V_{DD} \text{ Max}$ | |
| V_{IH} | Input High Voltage | $0.7 V_{DD}$ | $V_{DD}+0.3$ | V | $V_{DD}=V_{DD} \text{ Max}$ | |
| V_{IHC} | Input High Voltage (CMOS) | $V_{DD}-0.3$ | $V_{DD}+0.3$ | V | $V_{DD}=V_{DD} \text{ Max}$ | |
| V_{OL} | Output Low Voltage | | 0.2 | V | $I_{OL}=100 \mu A, V_{DD}=V_{DD} \text{ Min}$ | |
| V_{OH} | Output High Voltage | $V_{DD}-0.2$ | | V | $I_{OH}=-100 \mu A, V_{DD}=V_{DD} \text{ Min}$ | |

T10.1 1342

1. Address input = $V_{ILT}/V_{IHT}, V_{DD}=V_{DD} \text{ Max}$ (See Figure 23)

TABLE 11: Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|------------------|-----------------------------|---------|---------|
| $T_{PU-READ}^1$ | Power-up to Read Operation | 100 | μs |
| $T_{PU-WRITE}^1$ | Power-up to Write Operation | 100 | μs |

T11.0 1342

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: Capacitance ($T_A = 25^\circ C, f=1 \text{ Mhz}$, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------|---------------------|----------------|---------|
| $C_{I/O}^1$ | I/O Pin Capacitance | $V_{I/O} = 0V$ | 10 pF |
| C_{IN}^1 | Input Capacitance | $V_{IN} = 0V$ | 10 pF |

T12.0 1342

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|-------------|----------------|-----------------------|--------|---------------------|
| N_{END}^1 | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| T_{DR}^1 | Data Retention | 100 | Years | JEDEC Standard A103 |
| I_{LTH}^1 | Latch Up | $100 + I_{DD}$ | mA | JEDEC Standard 78 |

T13.0 1342

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 14: Read Cycle Timing Parameters $V_{DD} = 2.7-3.6V$

| Symbol | Parameter | Min | Max | Units |
|----------------|---------------------------------|-----|-----|---------|
| T_{RC} | Read Cycle Time | 70 | | ns |
| T_{CE} | Chip Enable Access Time | | 70 | ns |
| T_{AA} | Address Access Time | | 70 | ns |
| T_{OE} | Output Enable Access Time | | 35 | ns |
| T_{CLZ}^1 | CE# Low to Active Output | 0 | | ns |
| T_{OLZ}^1 | OE# Low to Active Output | 0 | | ns |
| T_{CHZ}^1 | CE# High to High-Z Output | | 16 | ns |
| T_{OHZ}^1 | OE# High to High-Z Output | | 16 | ns |
| T_{OH}^1 | Output Hold from Address Change | 0 | | ns |
| T_{RP}^1 | RST# Pulse Width | 500 | | ns |
| T_{RHR}^1 | RST# High before Read | 50 | | ns |
| $T_{RY}^{1,2}$ | RST# Pin Low to Read Mode | | 20 | μs |

T14.1 1342

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
This parameter does not apply to Chip-Erase operations.

TABLE 15: Program/Erase Cycle Timing Parameters

| Symbol | Parameter | Min | Max | Units |
|----------------|----------------------------------|-----|-----|---------|
| T_{BP} | Program Time | | 10 | μs |
| T_{AS} | Address Setup Time | 0 | | ns |
| T_{AH} | Address Hold Time | 40 | | ns |
| T_{CS} | WE# and CE# Setup Time | 0 | | ns |
| T_{CH} | WE# and CE# Hold Time | 0 | | ns |
| T_{OES} | OE# High Setup Time | 0 | | ns |
| T_{OEH} | OE# High Hold Time | 10 | | ns |
| T_{CP} | CE# Pulse Width | 40 | | ns |
| T_{WP} | WE# Pulse Width | 40 | | ns |
| T_{WPH}^1 | WE# Pulse Width High | 30 | | ns |
| T_{CPH}^1 | CE# Pulse Width High | 30 | | ns |
| T_{DS} | Data Setup Time | 30 | | ns |
| T_{DH}^1 | Data Hold Time | 0 | | ns |
| T_{IDA}^1 | Software ID Access and Exit Time | | 150 | ns |
| T_{SE} | Sector-Erase | | 25 | ms |
| T_{BE} | Block-Erase | | 25 | ms |
| T_{SCE} | Chip-Erase | | 50 | ms |
| T_{ES} | Erase-Suspend Latency | | 10 | μs |
| $T_{BY}^{1,2}$ | RY/BY# Delay Time | 90 | | ns |
| T_{BR}^1 | Bus Recovery Time | | 0 | μs |

T15.1 1342

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
This parameter does not apply to Chip-Erase operations.

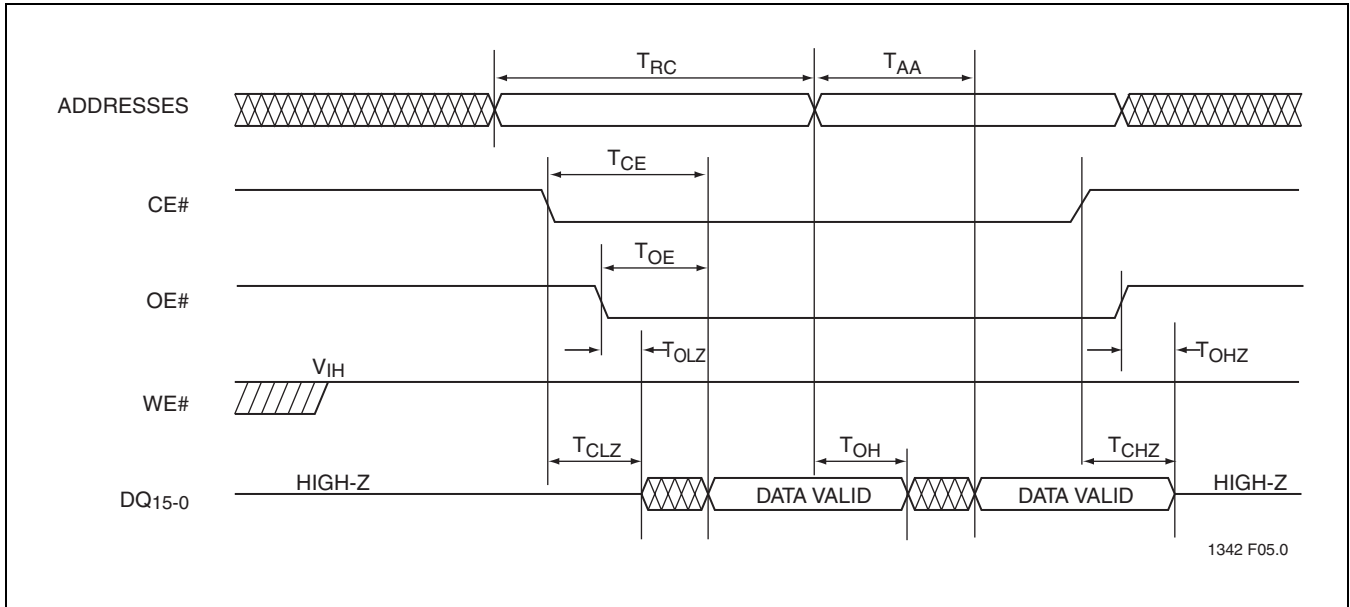
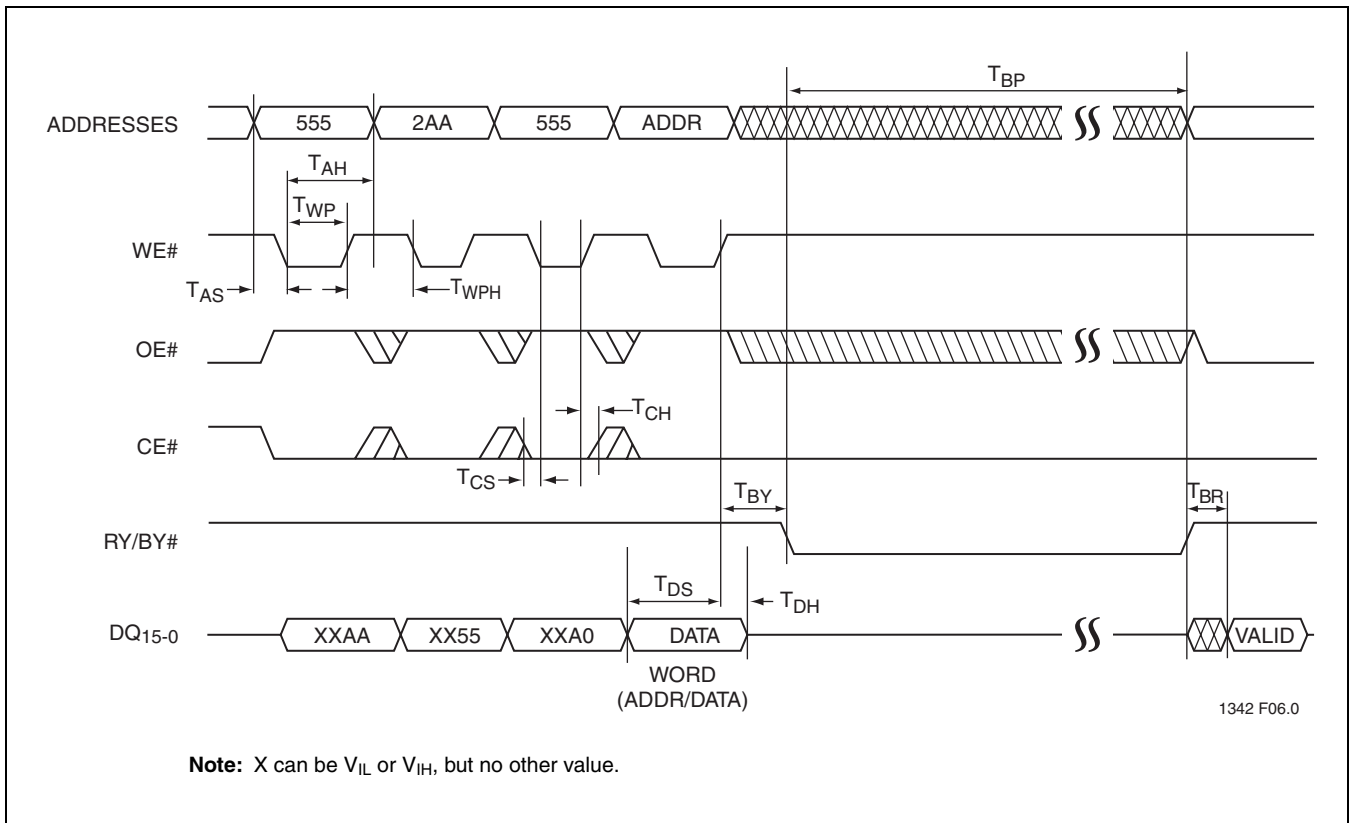


FIGURE 9: Read Cycle Timing Diagram



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 10: WE# Controlled Program Cycle Timing Diagram

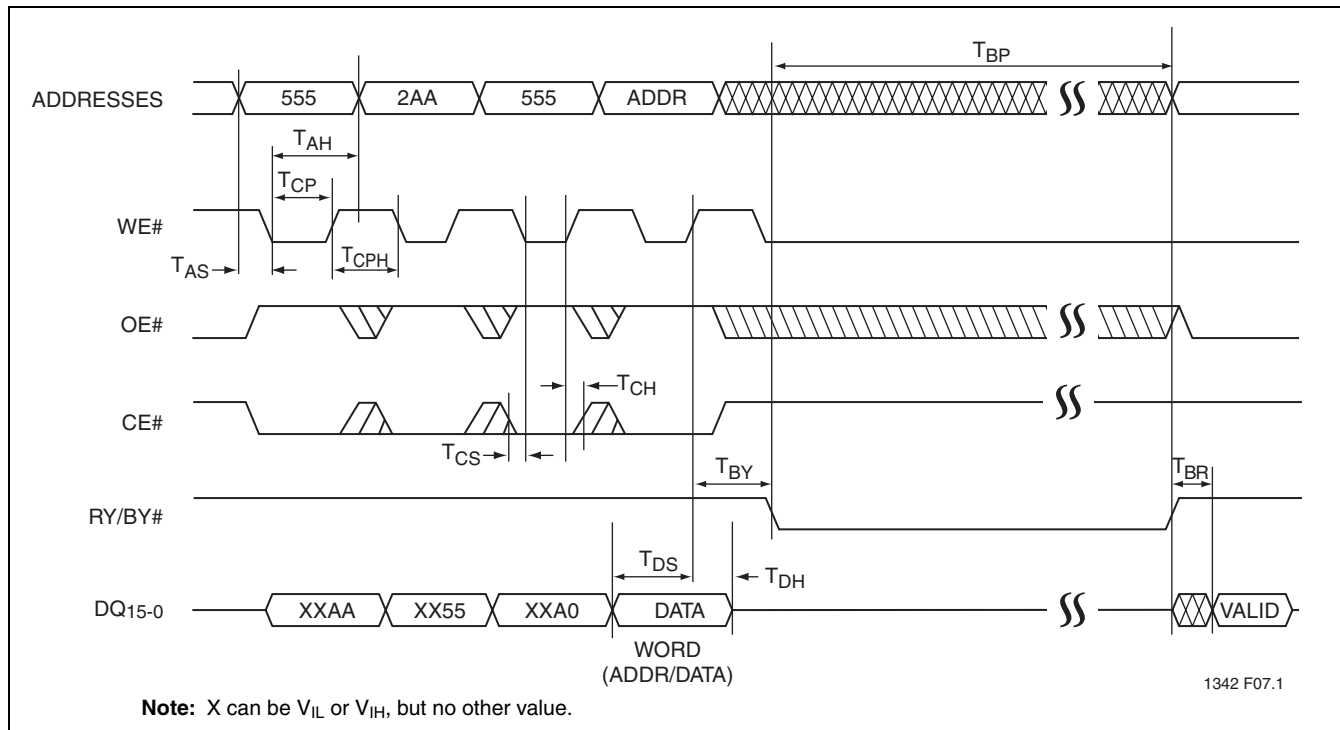


FIGURE 11: CE# Controlled Program Cycle Timing Diagram

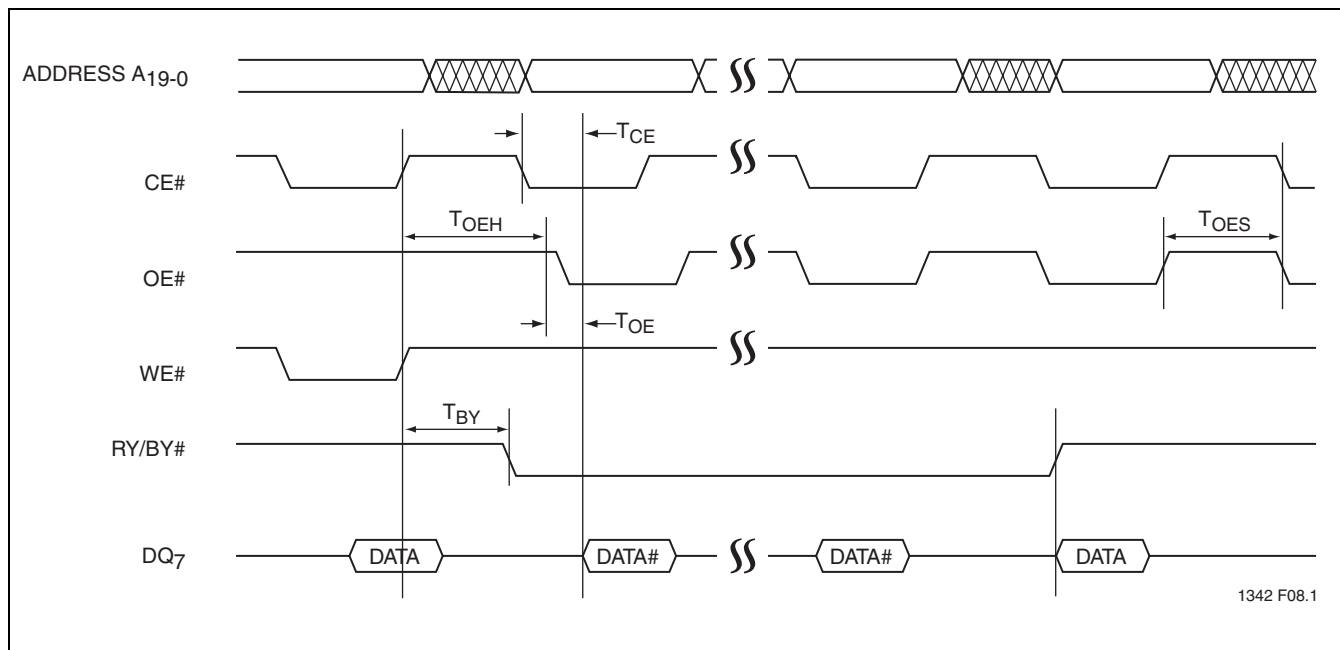


FIGURE 12: Data# Polling Timing Diagram

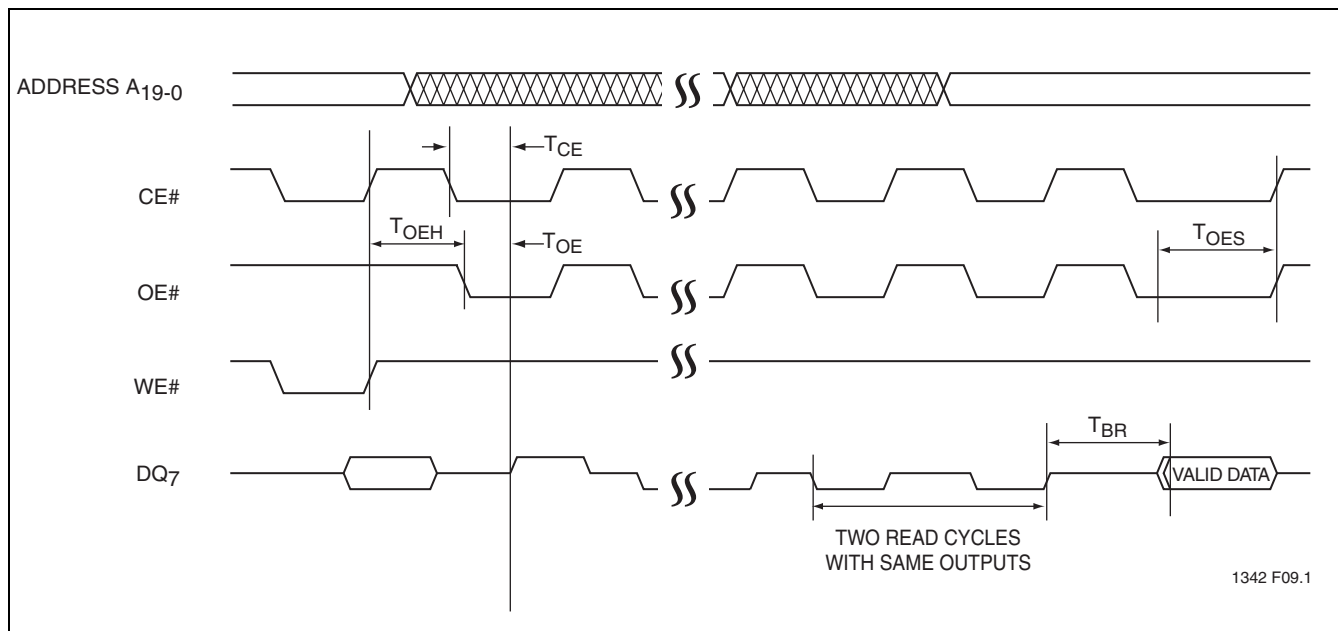


FIGURE 13: Toggle Bit Timing Diagram

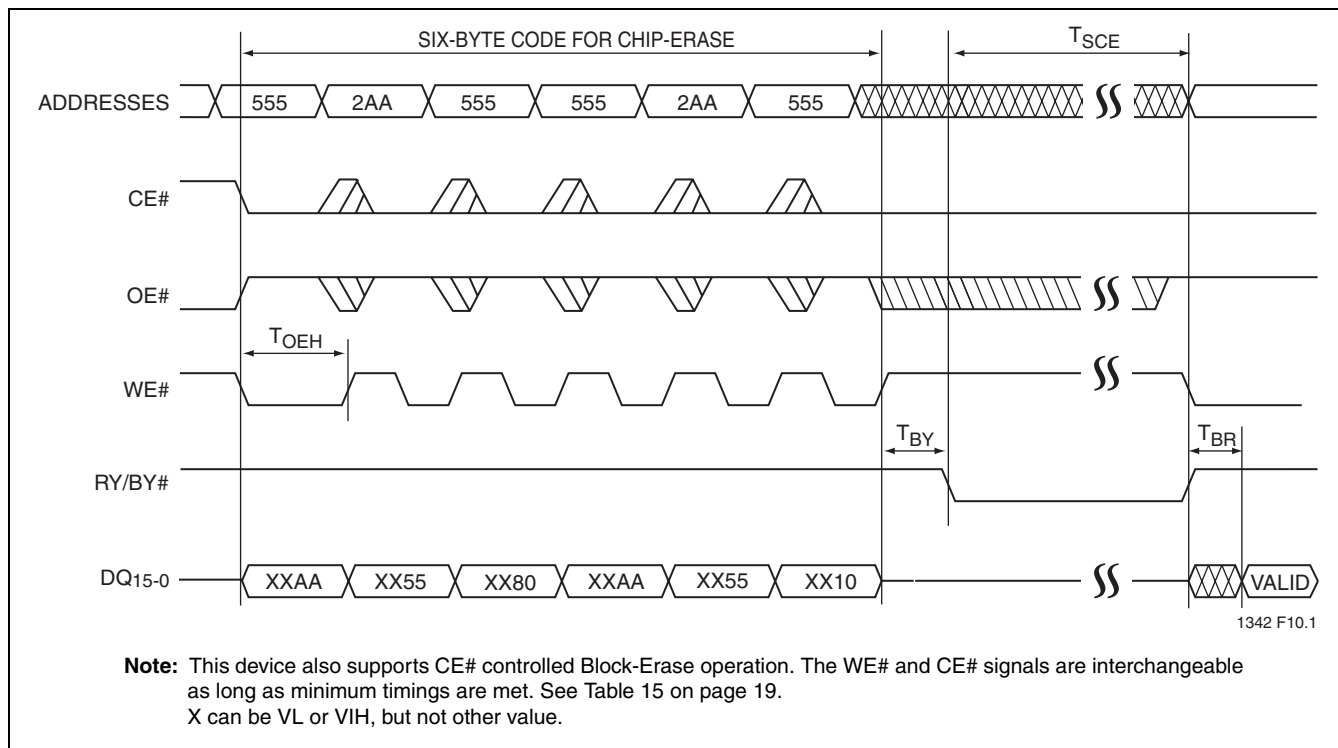


FIGURE 14: WE# Controlled Chip-Erase Timing Diagram

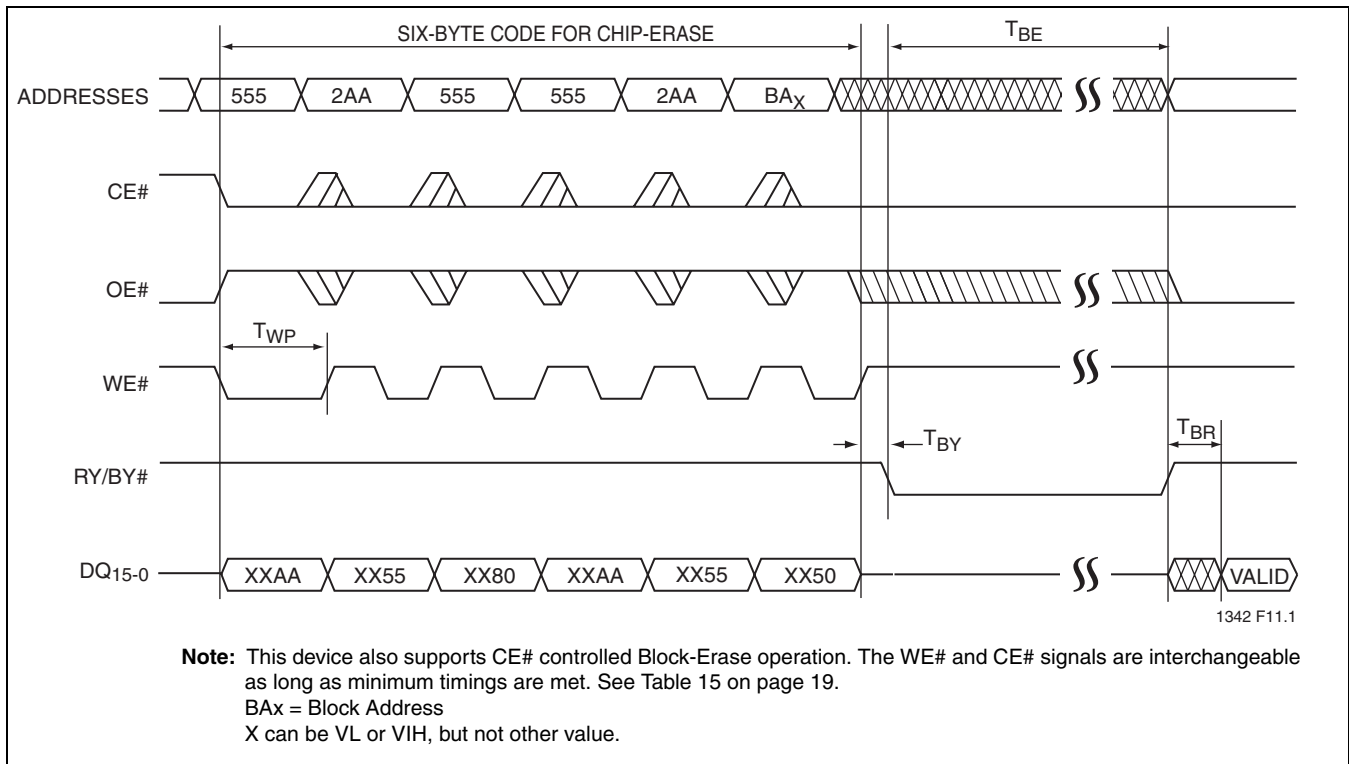


FIGURE 15: WE# Controlled Block-Erase Timing Diagram

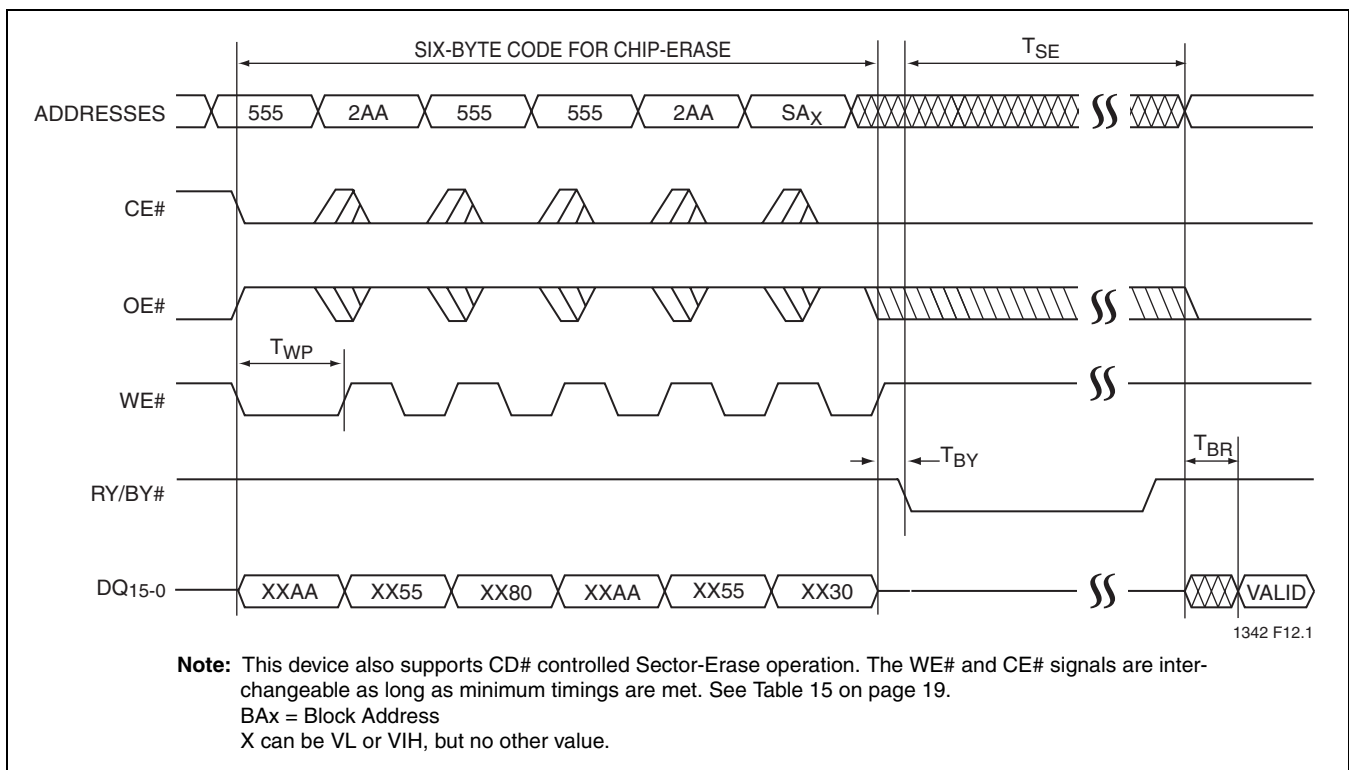


FIGURE 16: WE# Controlled Sector-Erase Timing Diagram

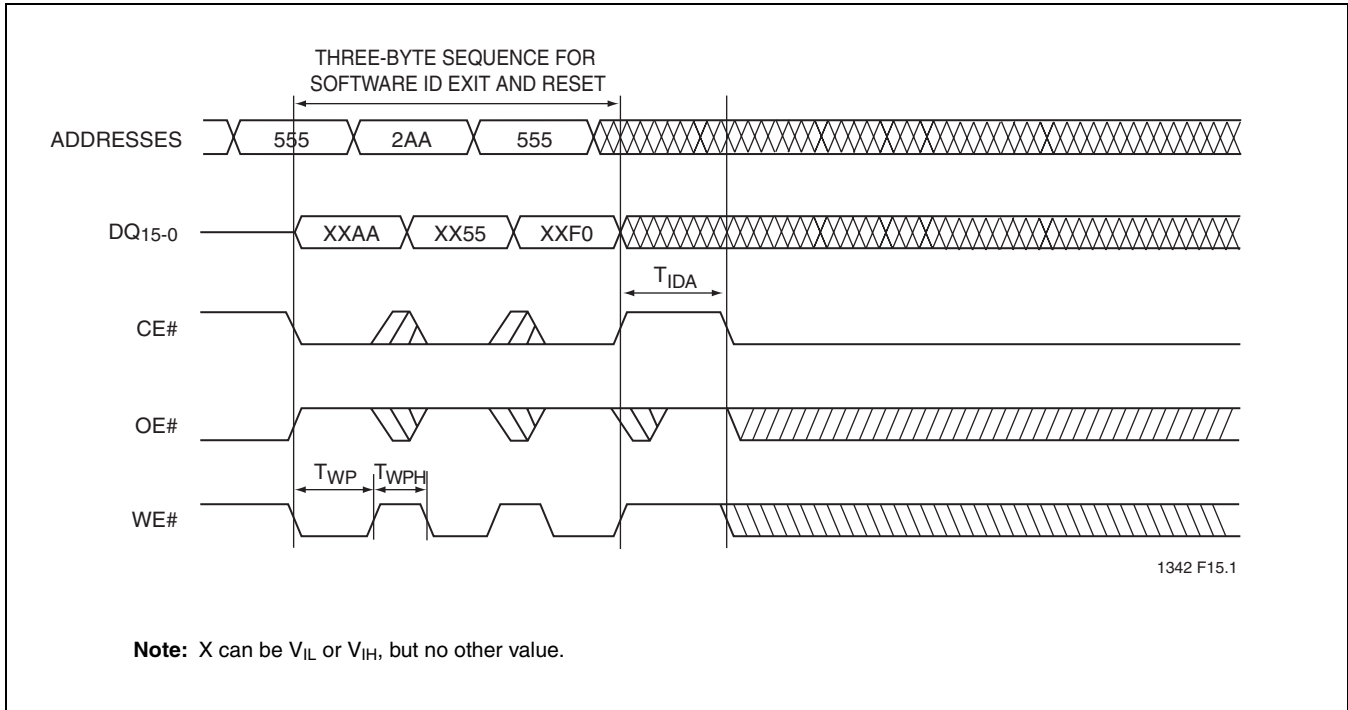


FIGURE 19: Software ID Exit/CFI Exit

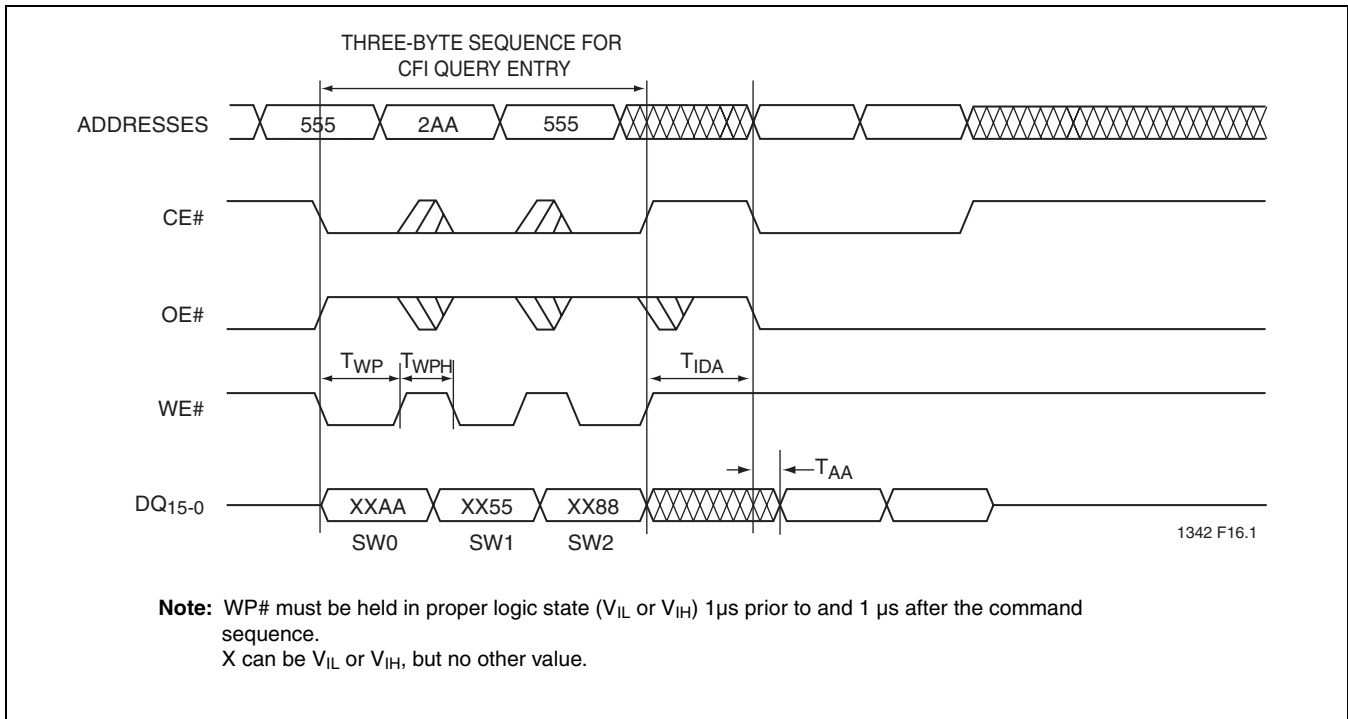


FIGURE 20: Sec ID Entry

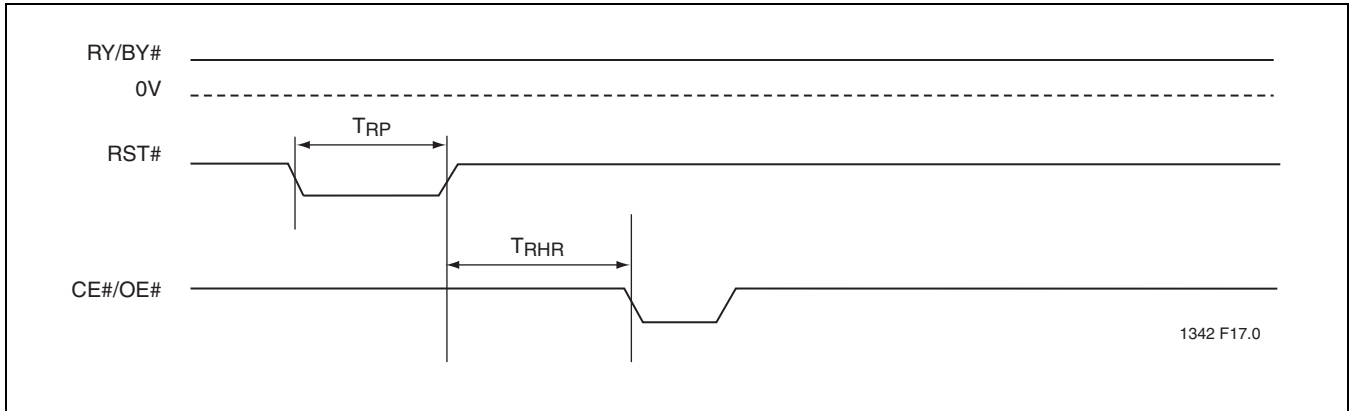


FIGURE 21: RST# Timing Diagram (When no internal operation is in progress)

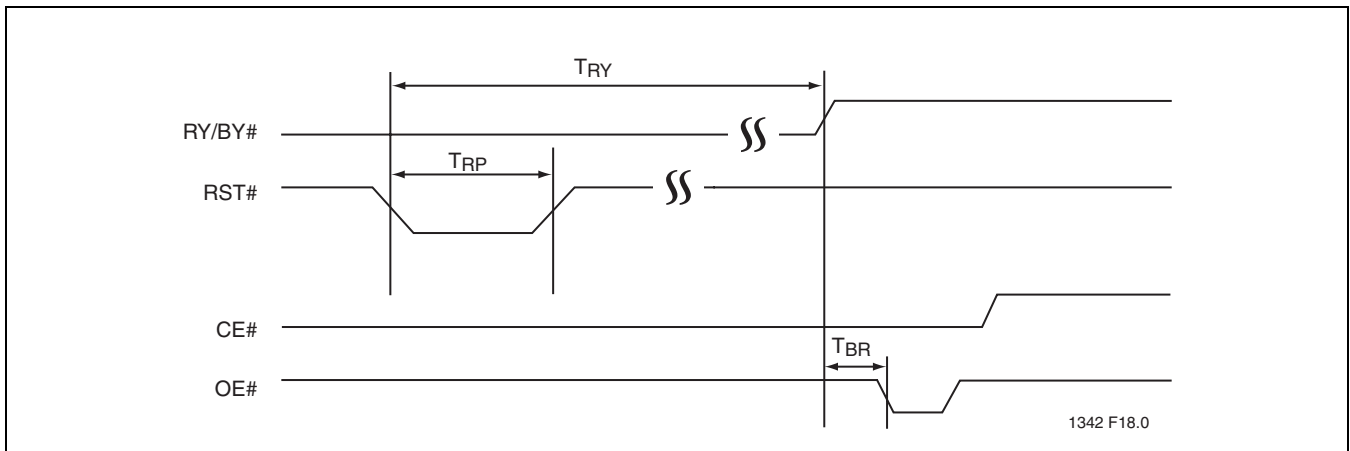


FIGURE 22: RST# Timing Diagram (During Sector- or Block-Erase operation)

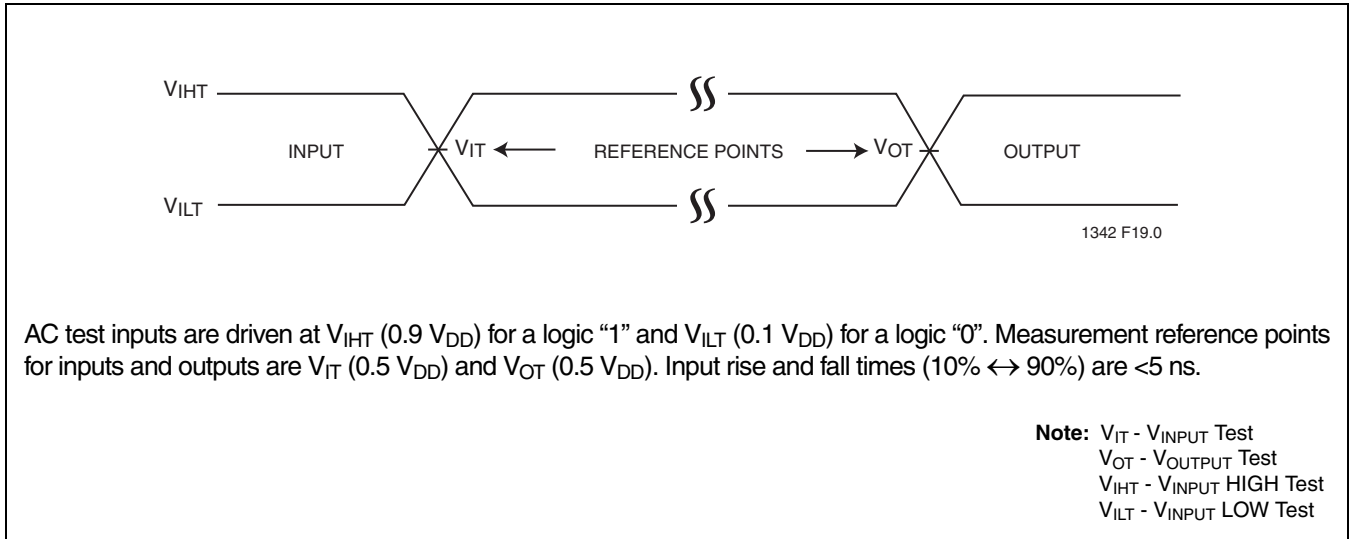


FIGURE 23: AC Input/Output Reference Waveforms

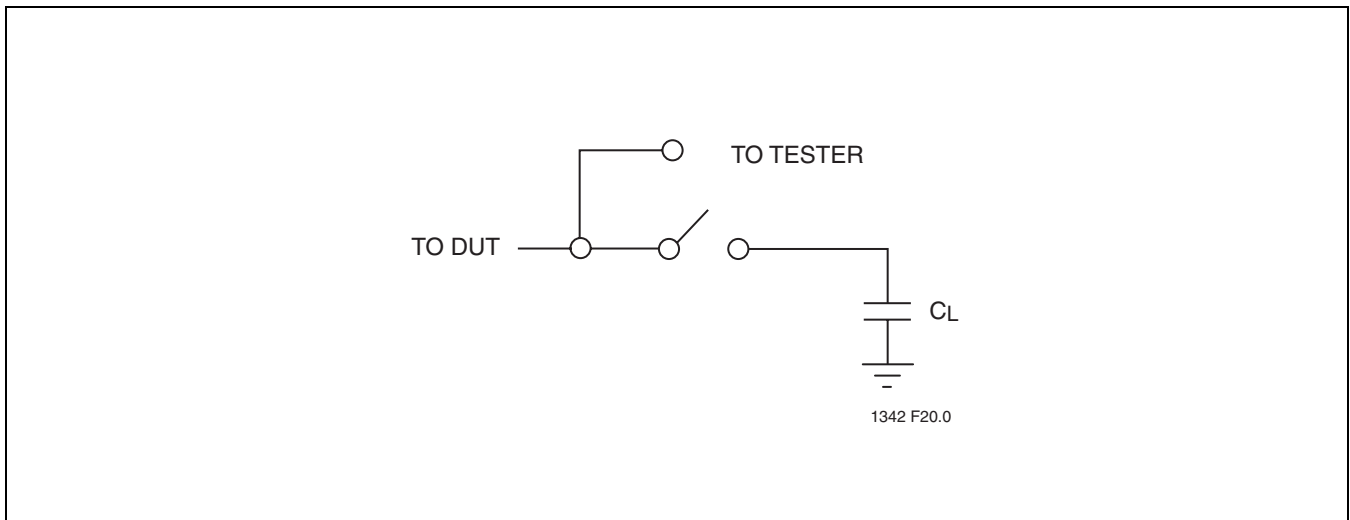


FIGURE 24: A Test Load Example

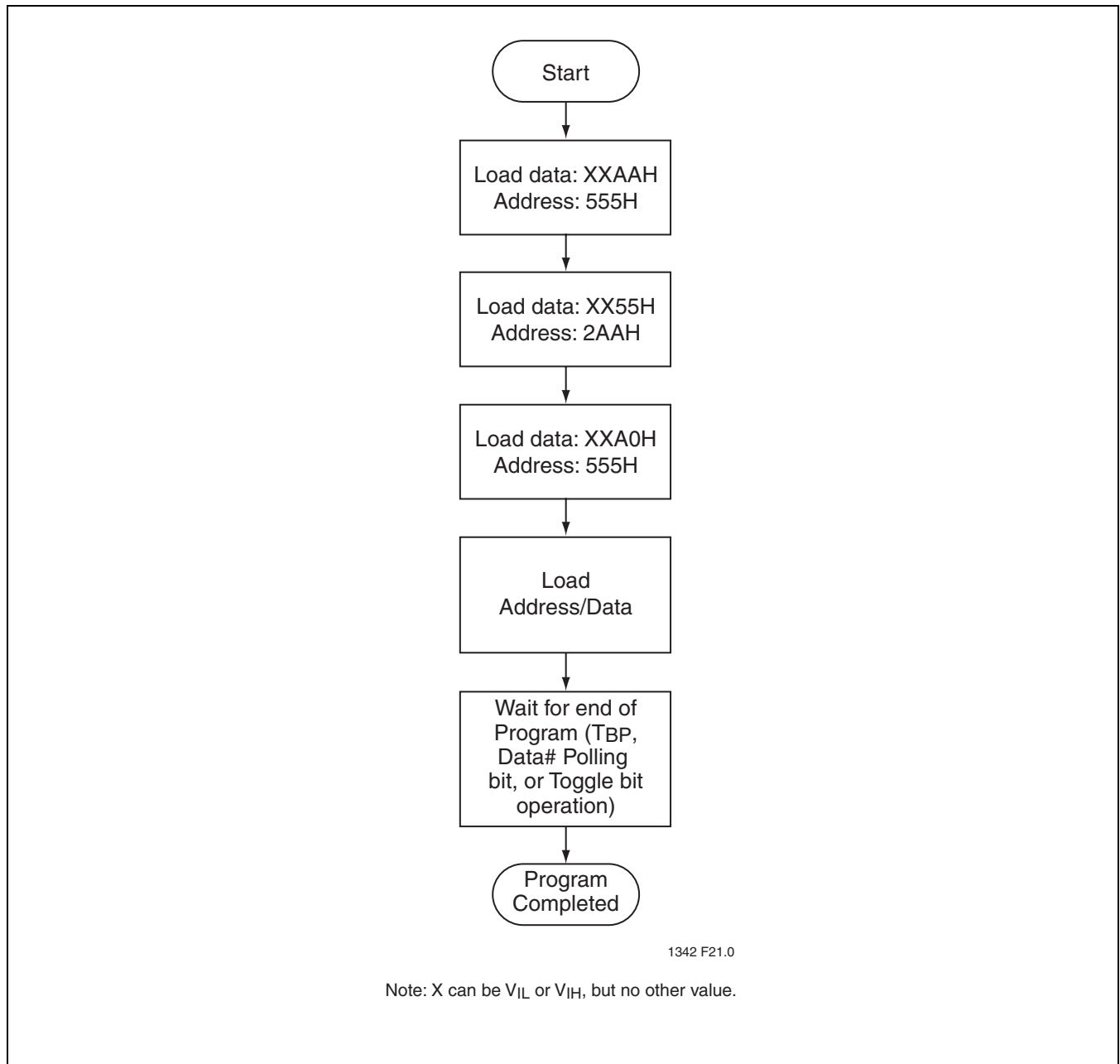


FIGURE 25: Program Algorithm

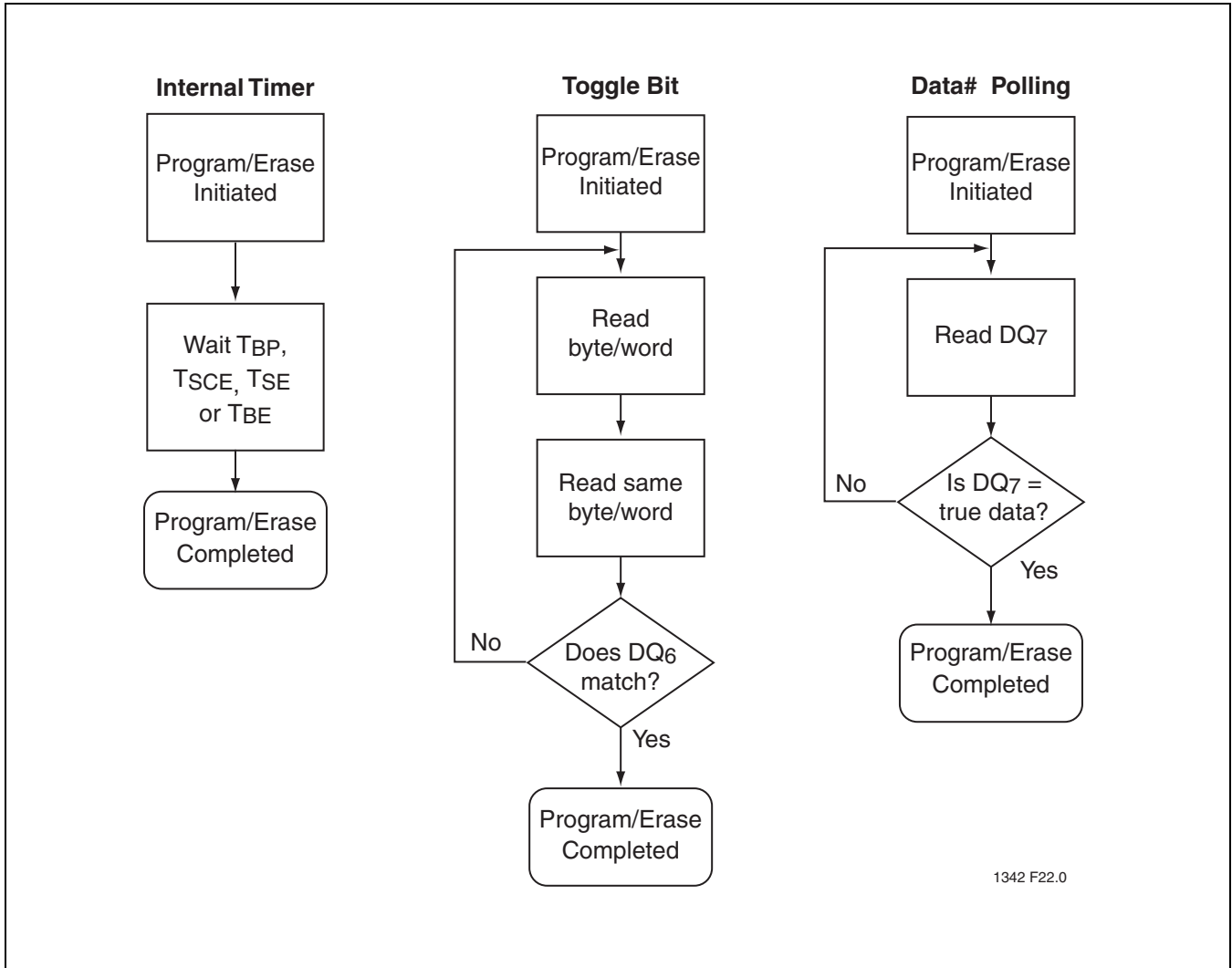


FIGURE 26: Wait Options

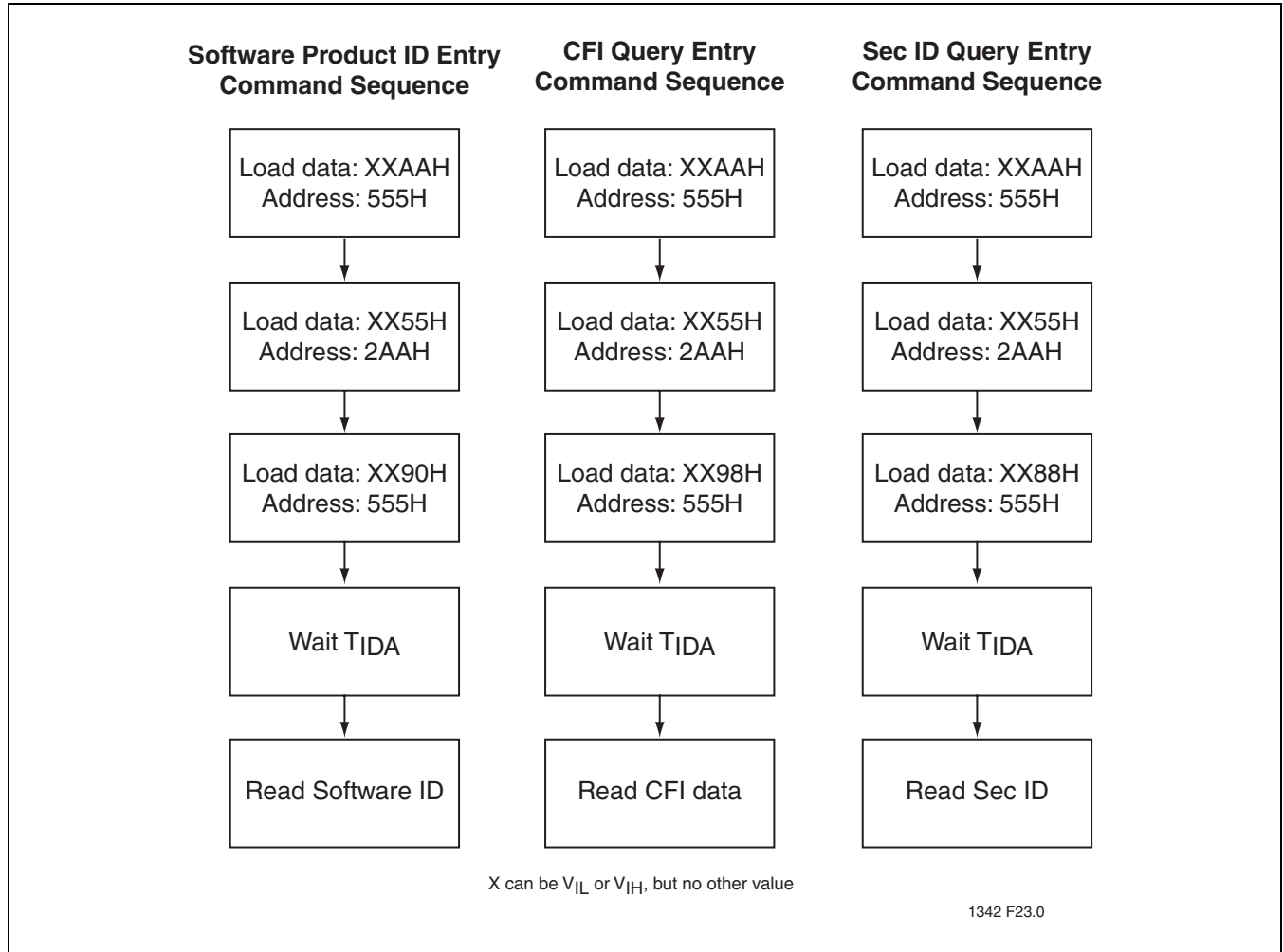


FIGURE 27: Software Product ID/CFI/Sec ID Entry Command Flowcharts

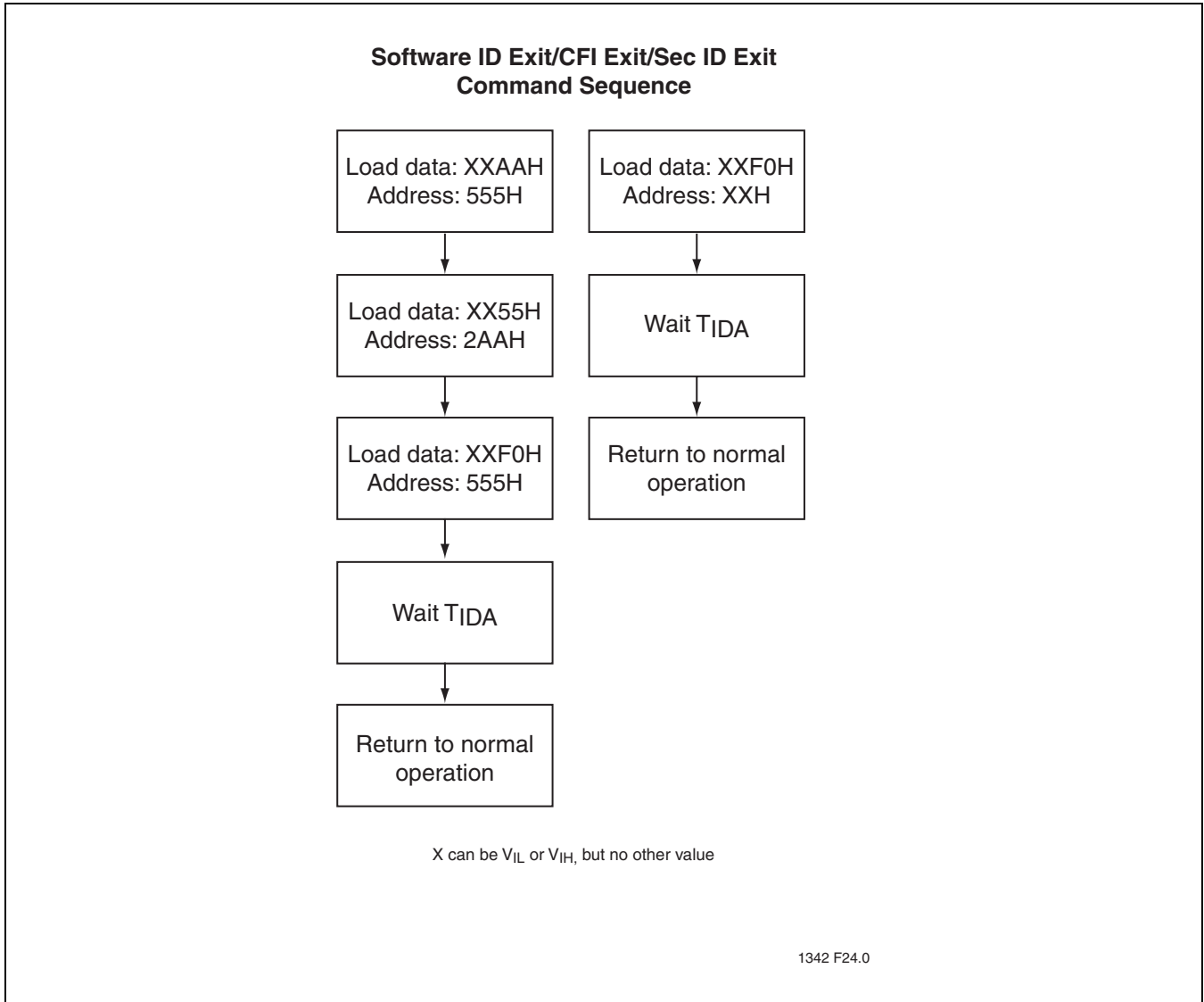


FIGURE 28: Software Product ID/CFI/Sec ID Exit Command Flowcharts

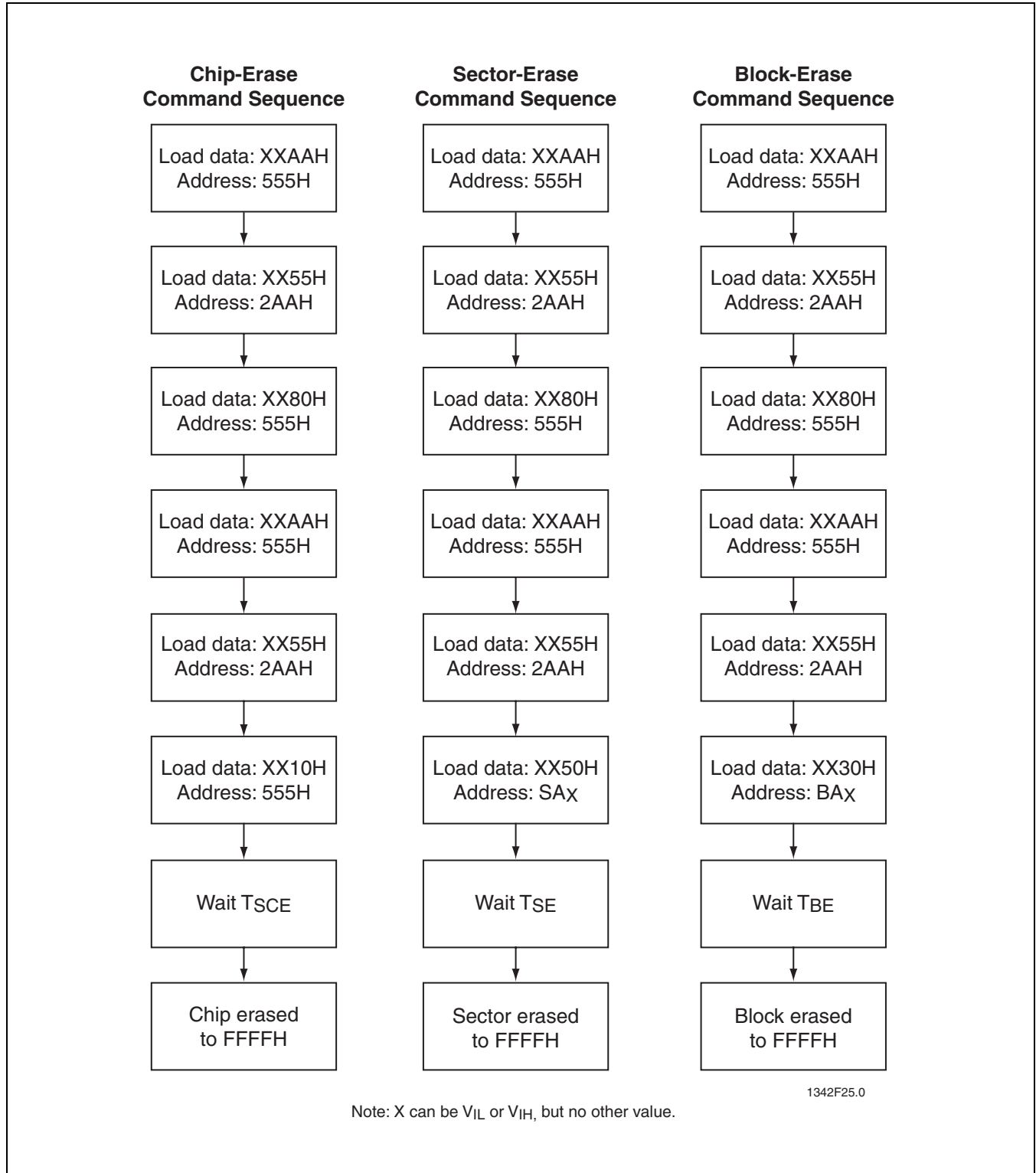


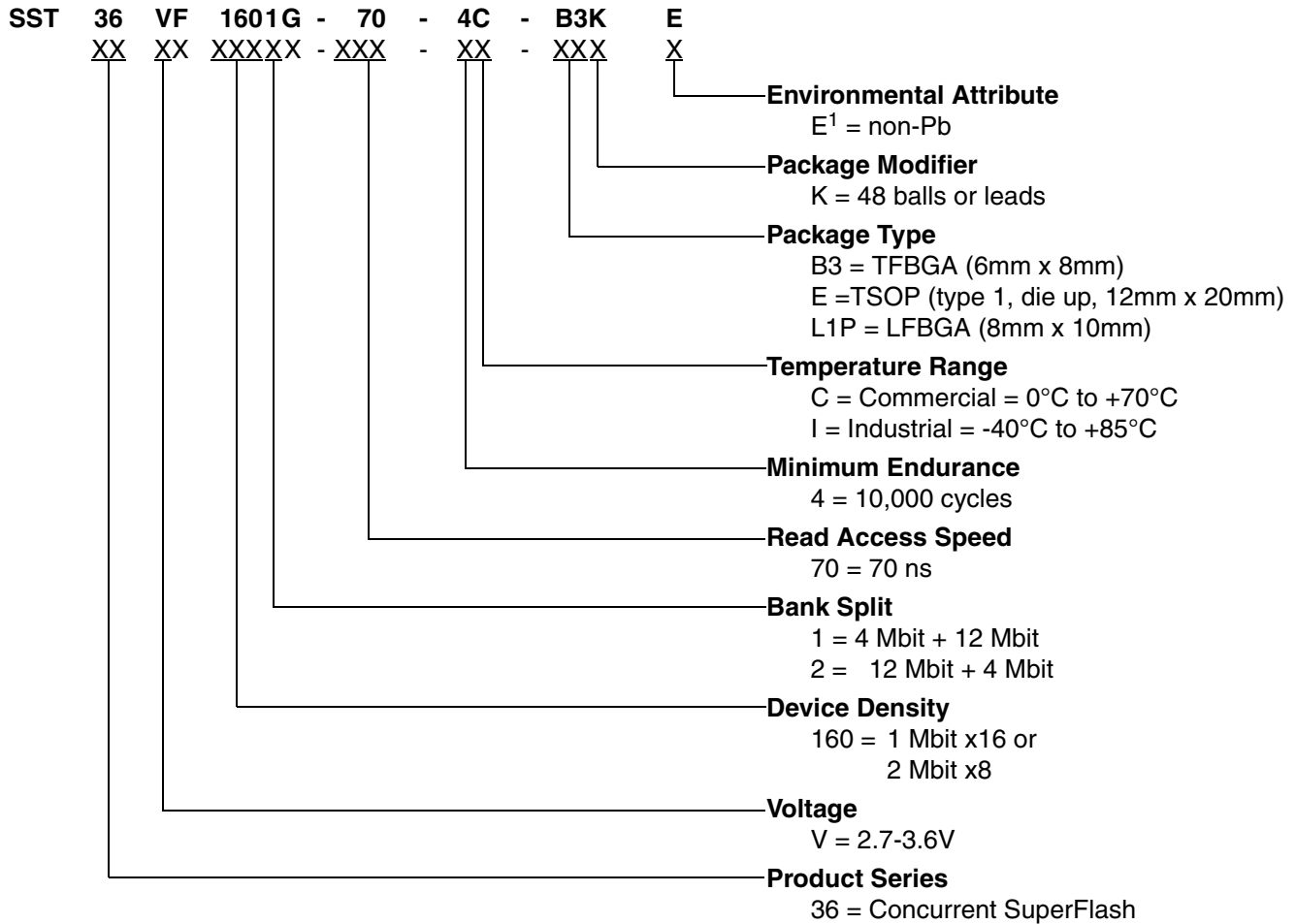
FIGURE 29: Erase Command Sequence

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PRODUCT ORDERING INFORMATION



1. Environmental suffix "E" denotes non-Pb solder.
SST non-Pb solder devices are "RoHS Compliant".

Valid combinations for SST36VF1601G

| | | |
|-------------------------|------------------------|-------------------------|
| SST36VF1601G-70-4C-B3KE | SST36VF1601G-70-4C-EKE | SST36VF1601G-70-4C-L1PE |
| SST36VF1601G-70-4I-B3KE | SST36VF1601G-70-4I-EKE | SST36VF1601G-70-4I-L1PE |

Valid combinations for SST36VF1602G

| | | |
|-------------------------|------------------------|-------------------------|
| SST36VF1602G-70-4C-B3KE | SST36VF1602G-70-4C-EKE | SST36VF1602G-70-4C-L1PE |
| SST36VF1602G-70-4I-B3KE | SST36VF1602G-70-4I-EKE | SST36VF1602G-70-4I-L1PE |

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



PACKAGING DIAGRAMS

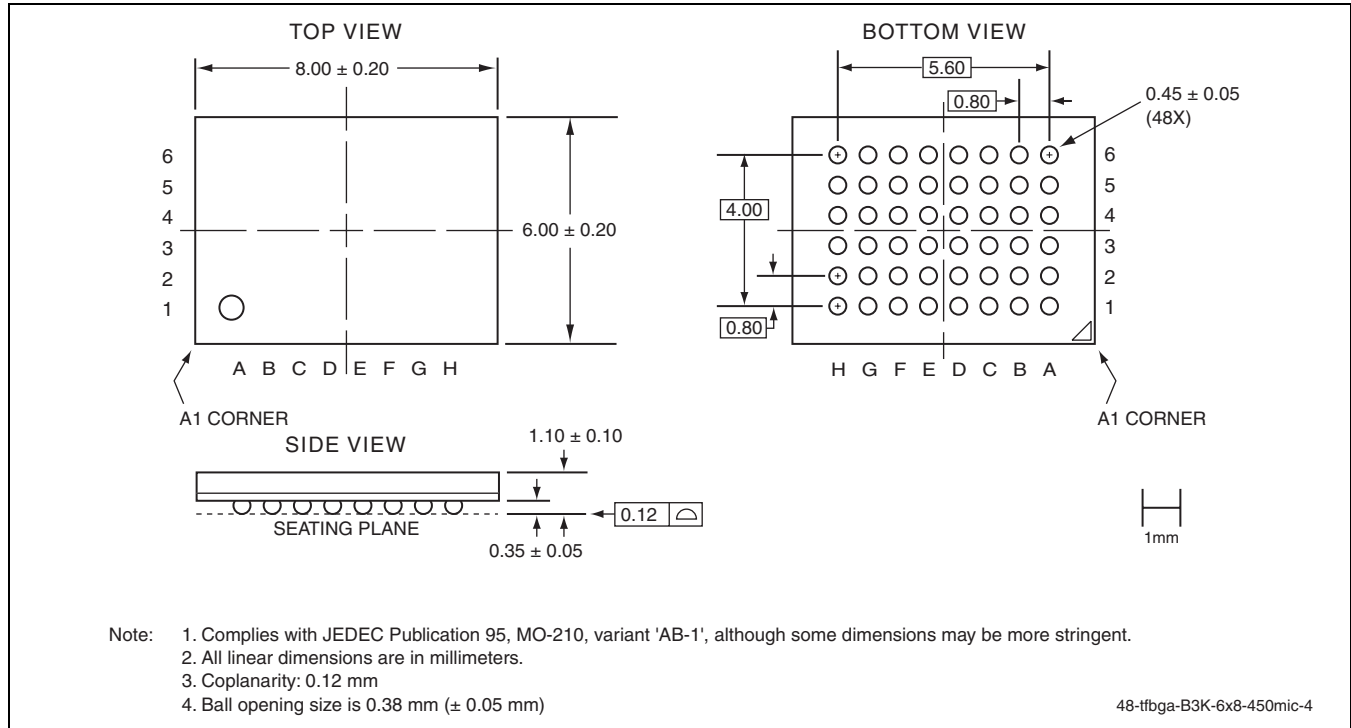


FIGURE 30: 48-ball Thin-profile, Fine-pitch Ball Grid Array (TFBGA) 6mm x 8mm
SST Package Code: B3K

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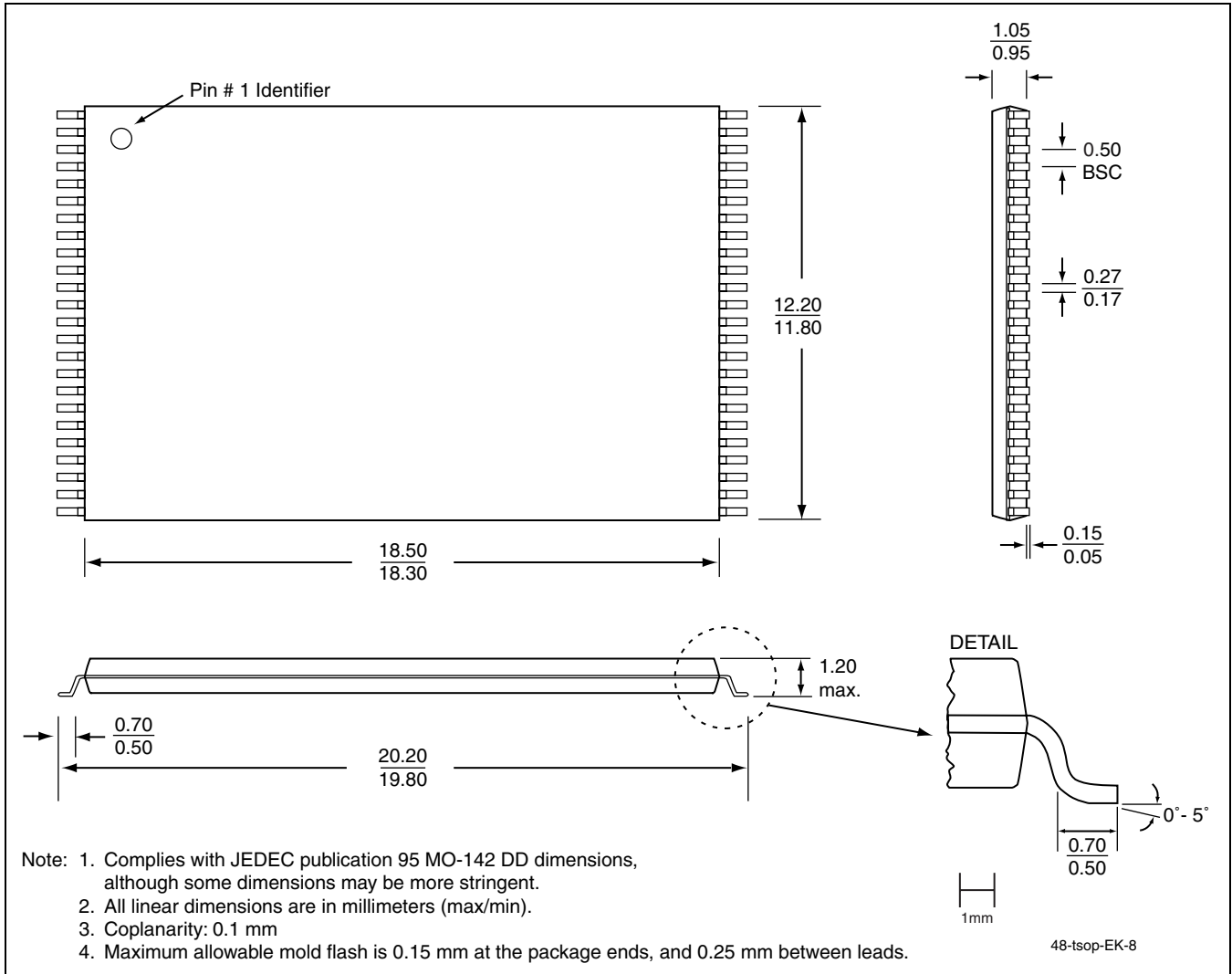
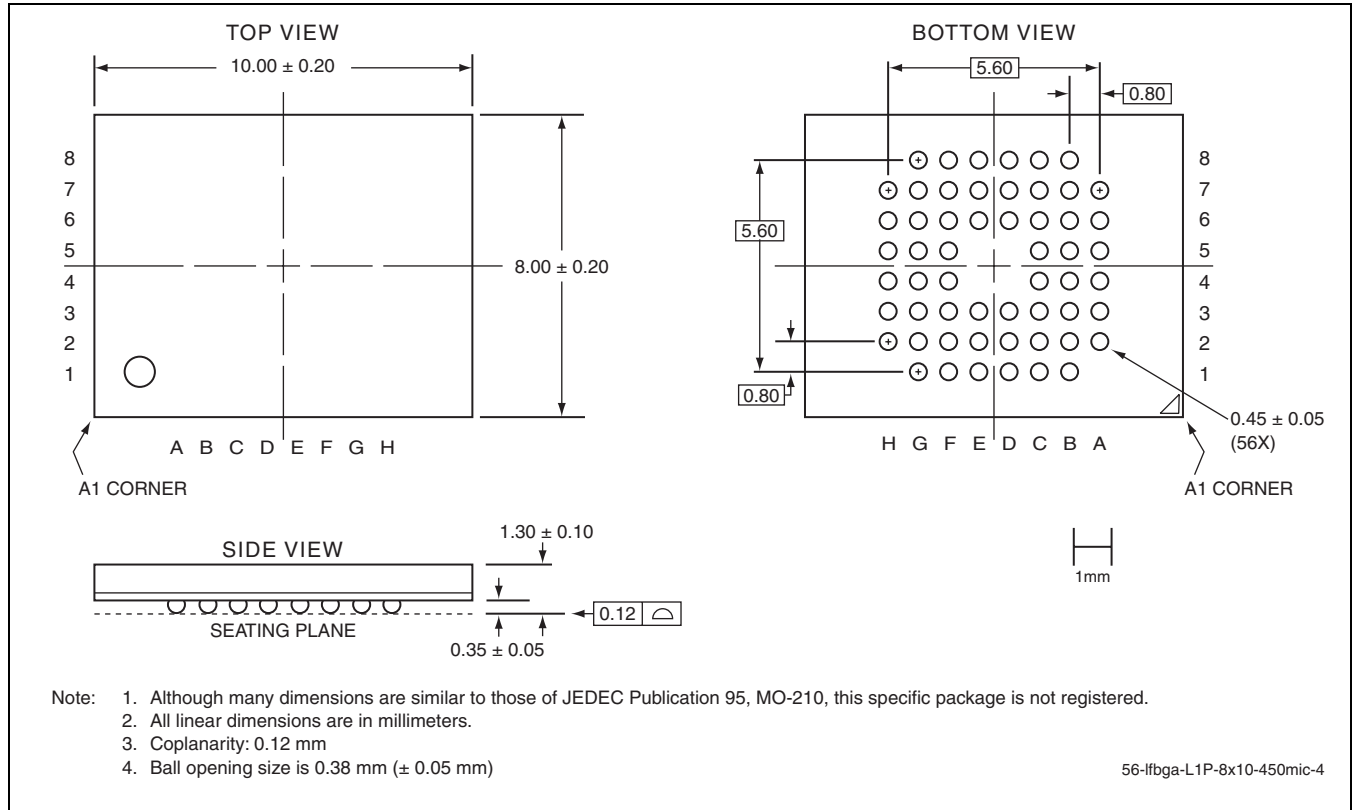


FIGURE 31: 48-lead Thin Small Outline Package (TSOP) 12mm x 20mm
SST Package Code: EK



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**FIGURE 32: 56-Ball, Low-Profile, Fine-Pitch Ball Grid Array (LFBGA) 8mm x 10mm
SST Package Code: L1P**

TABLE 16: Revision History

| Number | Description | Date |
|--------|---------------------------------|----------|
| 00 | • Initial release of data sheet | Dec 2006 |