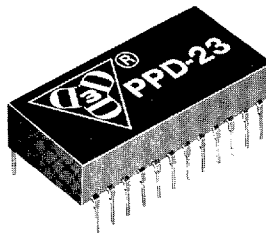


Programmable Pulse Discriminator

SERIES: PPD-23
(3 BIT) TTL Interfaced

data
delay
devices, inc.



Features:

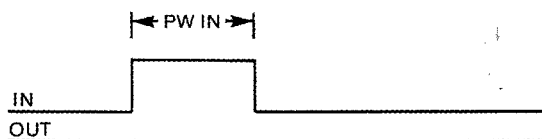
- Discriminates against precisely programmed pulse widths.
- 3-bit address.
- 24 pins DIP.
- Low profile.

Specifications:

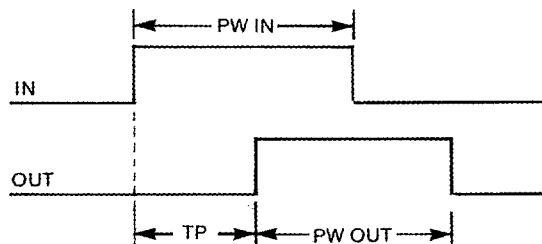
- Inherent pulse width (PW_0): 5 ns typ.
- Supply voltage: 5 Vdc $\pm$ 5%.
- Operating temperatures: 0°C to 70°C.
- Temperature coefficient: 100 PPM/°C.
- Power Dissipation: 850 mw max.
- DC parameters: See TTL-Standard Schottky Logic Table on Page 6.

PW_{IN} = Input pulse width
 PW_{OUT} = Output pulse $\approx PW_{IN} - 4$ ns
 TP = Propagation delay $\approx PW_{Programmed} + 6$ ns

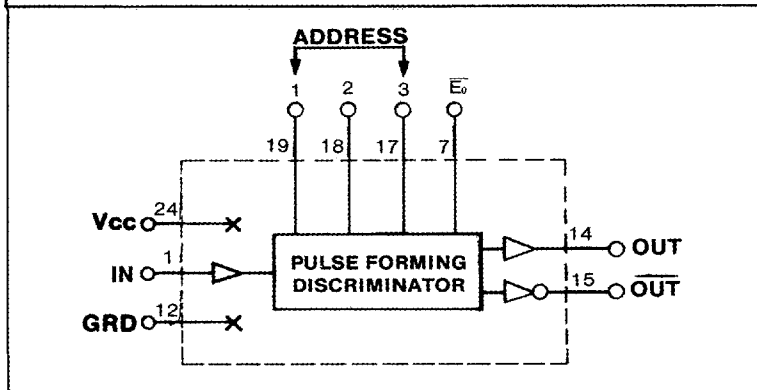
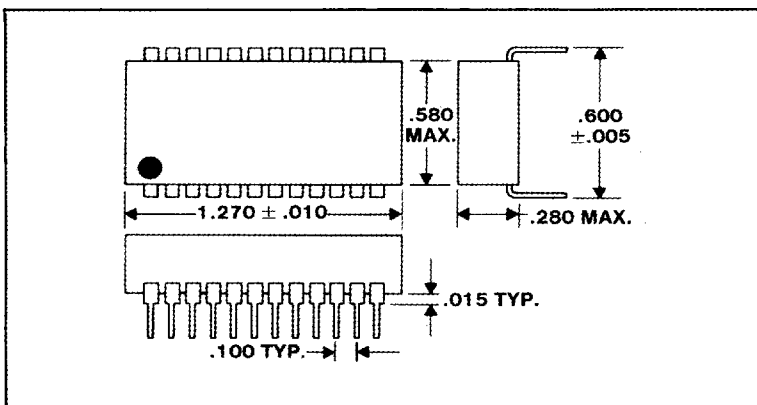
* **CONDITION A:** ($PW_{IN} \leq \text{PROGRAMMED } PW$)



* **CONDITION B:** ($PW_{IN} \geq \text{PROGRAMMED } PW$)



*See page vi for details timing.



Part Number	Incremental Pulse Width Per Step (ns)	Total Programmed Pulse Width (ns)
PPD-23-1	1 $\pm$.4	7
PPD-23-2	2 $\pm$.4	14
PPD-23-3	3 $\pm$.5	21
PPD-23-5	5 $\pm$.6	35
PPD-23-10	10 $\pm$ 1.0	70
PPD-23-15	15 $\pm$ 1.3	105
PPD-23-20	20 $\pm$ 1.5	140
PPD-23-40	40 $\pm$ 2.0	280
PPD-23-50	50 $\pm$ 2.5	350

Contact us for specific requirements. We customize.

2644382 0001066 295

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