

OPA234
OPA2234
OPA4234

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Low Power, Precision SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

FEATURES

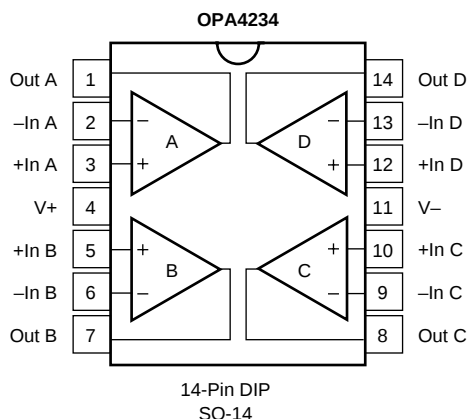
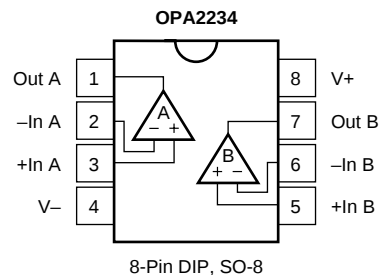
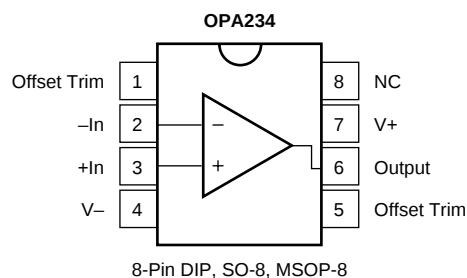
- **WIDE SUPPLY RANGE:**
Single Supply: $V_S = +2.7V$ to $+36V$
Dual Supply: $V_S = \pm 1.35V$ to $\pm 18V$
- **GUARANTEED PERFORMANCE:**
 $\pm 2.7V$, $+5V$, and $\pm 15V$
- **LOW QUIESCENT CURRENT:** $250\mu A/\text{amp}$
- **LOW INPUT BIAS CURRENT:** $25nA$ max
- **LOW OFFSET VOLTAGE:** $100\mu V$ max
- **HIGH CMRR, PSRR, and A_{OL}**
- **SINGLE, DUAL, and QUAD VERSIONS**

DESCRIPTION

The OPA234 series low cost op amps are ideal for single supply, low voltage, low power applications. The series provides lower quiescent current than older "1013"-type products and comes in current industry-standard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power supply rejection, and a wide supply range provides excellent accuracy and versatility. Single, dual, and quad versions have identical specifications for maximum design flexibility. These general purpose op amps are ideal for portable and battery powered applications.

OPA234 series op amps operate from either single or dual supplies. In single supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA234 series ideal for demanding applications, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

Single version packages are DIP-8, SO-8 surface-mount, and a space-saving MSOP-8 surface-mount. Dual packages are DIP-8 and SO-8 surface-mount. Quad packages are DIP-14 and SO-14 surface-mount. All are specified for $-40^\circ C$ to $+85^\circ C$ operation.



SPECIFICATIONS: $V_S = +5V$

At $T_A = 25^\circ\text{C}$, $V_S = +5V$, $R_L = 10k\Omega$ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITION	OPA234P, U, E OPA2234P, U			OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage OPA234E, EA vs Temperature ⁽¹⁾ vs Power Supply vs Time Channel Separation (Dual, Quad)	V_{OS} dV_{OS}/dT PSRR $V_S = +2.7V$ to $+30V$, $V_{CM} = 1.7V$		± 40 ± 100 ± 0.5 3 0.2 0.3	± 100 ± 150 ± 3 10		*	± 250 ± 350 *	μV μV $\mu V/^\circ\text{C}$ $\mu V/V$ $\mu V/mo$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	I_B I_{OS} $V_{CM} = 2.5V$ $V_{CM} = 2.5V$		-15 ± 1	-30 ± 5		*	-50 *	nA nA
NOISE Input Voltage Noise Density Current Noise Density	$f = 1\text{kHz}$ V_n i_n		25 80			*		$nV/\sqrt{\text{Hz}}$ $fA/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection	CMRR $V_{CM} = -0.1V$ to $4V$	-0.1 91	106	(V+) -1	*	*	*	V dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = 2.5V$		$10^7 \parallel 5$ $10^{10} \parallel 6$			*		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_O = 0.25V$ to $4V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	108 86	120 96		100 86	*	*	dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	GBW SR $C_L = 100pF$ $G = 1$, 3V Step, $C_L = 100pF$ $G = 1$, 3V Step, $C_L = 100pF$ (V_{IN}) (Gain) = V_S		0.35 0.2 15 25 16			*	*	MHz V/ μs μs μs μs
OUTPUT Voltage Output: Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation) ⁽³⁾	$R_L = 10k\Omega$ to $V_S/2$ $R_L = 10k\Omega$ to $V_S/2$ $R_L = 10k\Omega$ to Ground $R_L = 10k\Omega$ to Ground $G = +1$	(V+) -1 0.25 (V+) -1 0.1	(V+) -0.65 0.05 (V+) -0.65 0.05 ± 11 1000		*	*	*	V V V V mA pF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	I_Q $I_Q = 0$	+2.7	+5 250	+36 300	*	*	*	V V μA
TEMPERATURE RANGE Specified Range Operating Range Storage Thermal Resistance 8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount	θ_{JA}	-40 -40 -55		+85 +125 +125	*	*	*	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$

* Specifications same as OPA234P,U,E.

NOTES: (1) Guaranteed by wafer-level test to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See "Small-Signal Overshoot vs Load Capacitance" typical curve.

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SPECIFICATIONS: $V_S = +2.7V$

At $T_A = 25^\circ C$, $V_S = +2.7V$, $R_L = 10k\Omega$ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITION	OPA234P, U, E OPA2234P, U			OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage OPA234E, EA vs Temperature ⁽¹⁾ vs Power Supply vs Time Channel Separation (Dual, Quad)	V_{OS} dV_{OS}/dT PSRR $V_S = +2.7V$ to $+30V$, $V_{CM} = 1.7V$		± 40 ± 100 ± 0.5 3 0.2 0.3	± 100 ± 150 ± 3 10		*	± 250 ± 350 *	μV μV $\mu V/^\circ C$ $\mu V/V$ $\mu V/mo$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	I_B I_{OS} $V_{CM} = 1.35V$ $V_{CM} = 1.35V$		-15 ± 1	-30 ± 5		*	-50 *	nA n
NOISE Input Voltage Noise Density Current Noise Density	$f = 1kHz$ V_n i_n		25 80			*		$nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection	CMRR $V_{CM} = -0.1V$ to $1.7V$	-0.1 91	106	(V+) -1	*	*	*	V dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = 1.35V$		$10^7 \parallel 5$ $10^{10} \parallel 6$			*	*	$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_O = 0.25V$ to $1.7V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	108 86	125 96		100 86	*	*	dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	GBW SR $C_L = 100pF$ $G = 1$, 1V Step, $C_L = 100pF$ $G = 1$, 1V Step, $C_L = 100pF$ (V_{IN}) (Gain) = V_S		0.35 0.2 6 16 8			*	*	MHz V/ μs μs μs μs
OUTPUT Voltage Output: Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation) ⁽³⁾	$R_L = 10k\Omega$ to $V_S/2$ $R_L = 10k\Omega$ to $V_S/2$ $R_L = 10k\Omega$ to Ground $R_L = 10k\Omega$ to Ground $G = +1$	(V+) -1 0.25 (V+) -1 0.1	(V+) -0.6 0.05 (V+) -0.65 0.05 ± 8 1000		*	*	*	V V V V mA pF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	I_Q $I_Q = 0$	+2.7	+2.7 250	+36 300	*	*	*	V V μA
TEMPERATURE RANGE Specified Range Operating Range Storage Thermal Resistance 8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount	θ_{JA}	-40 -40 -55		+85 +125 +125	*	*	*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

* Specifications same as OPA234P,U,E.

NOTES: (1) Guaranteed by wafer-level test to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See "Small-Signal Overshoot vs Load Capacitance" typical curve.

SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = 25^\circ C$, $V_S = \pm 15V$, $R_L = 10k\Omega$ connected to ground, unless otherwise noted.

PARAMETER	CONDITION	OPA234P, U, E OPA2234P, U			OPA234PA, UA, EA OPA2234PA, UA OPA4234PA, UA, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage V_{OS} OPA4234U Model vs Temperature ⁽¹⁾ dV_{OS}/dT vs Power Supply PSRR vs Time Channel Separation (Dual, Quad)	$V_{CM} = 0V$ Operating Temperature Range $V_S = \pm 1.35V$ to $\pm 18V$, $V_{CM} = 0V$		± 70 ± 0.5 3 0.2 0.3	± 250 ± 5 10		* ± 70 * * *	± 500 ± 250 * 20	μV μV $\mu V/^\circ C$ $\mu V/V$ $\mu V/mo$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ I_B Input Offset Current I_{OS}	$V_{CM} = 0V$ $V_{CM} = 0V$		-12 ± 1	-25 ± 5		* *	-50 *	nA nA
NOISE Input Voltage Noise Density V_n Current Noise Density i_n	$f = 1kHz$		25 80			* *		$nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection CMRR	$V_{CM} = -15V$ to $14V$	(V-) 91	106	(V+) -1	* 86	* *	* *	V dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = 0V$		$10^7 \parallel 5$ $10^{10} \parallel 6$			* *		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain A_{OL}	$V_O = -14.5V$ to $14V$	110	120		100	*		dB
FREQUENCY RESPONSE Gain-Bandwidth Product GBW Slew Rate SR Settling Time: 0.1% 0.01% Overload Recovery Time	$C_L = 100pF$ $G = 1$, 10V Step, $C_L = 100pF$ $G = 1$, 10V Step, $C_L = 100pF$ (V_{IN}) (Gain) = V_S		0.35 0.2 41 47 22			* * * * *		MHz V/ μs μs μs μs
OUTPUT Voltage Output: Positive Negative Short-Circuit Current I_{SC} Capacitive Load Drive (Stable Operation) ⁽³⁾	$G = +1$	(V+) -1 (V-) +0.5	(V+) -0.7 (V-) +0.15 ± 22 1000		* *	* * * *		V V mA pF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier) I_Q	$I_O = 0$	± 1.35	± 15 ± 275	± 18 ± 350	* *	* *	* *	V V μA
TEMPERATURE RANGE Specified Range Operating Range Storage Thermal Resistance θ_{JA} 8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount		-40 -40 -55	100 150 220 80 110	+85 +125 +125	* * *		* * *	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

* Specifications same as OPA234P,U,E.

NOTES: (1) Guaranteed by wafer-level test to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See "Small-Signal Overshoot vs Load Capacitance" typical curve.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage (V–) –0.7V to (V+) +0.7V	
Output Short-Circuit ⁽¹⁾	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Short-circuit to ground, one amplifier per package.

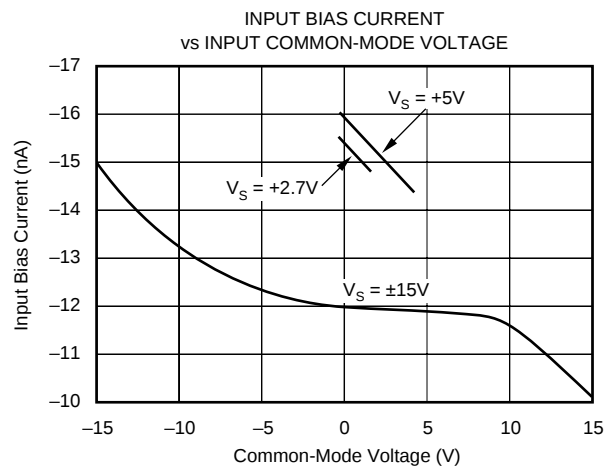
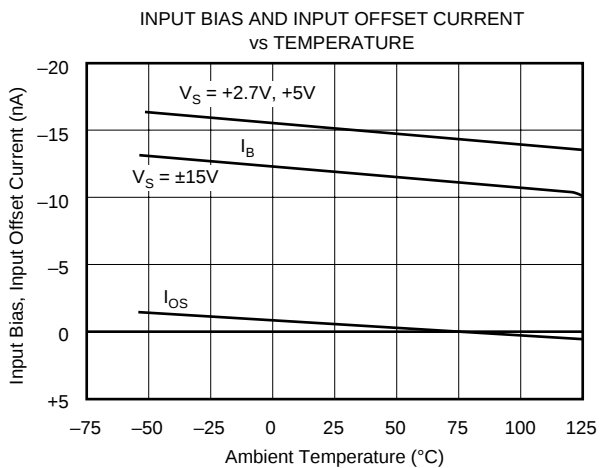
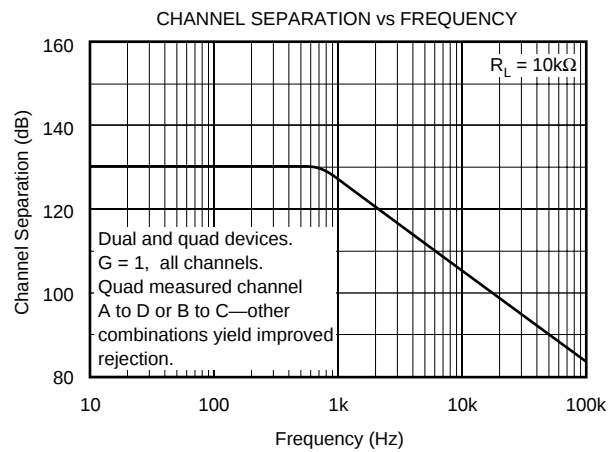
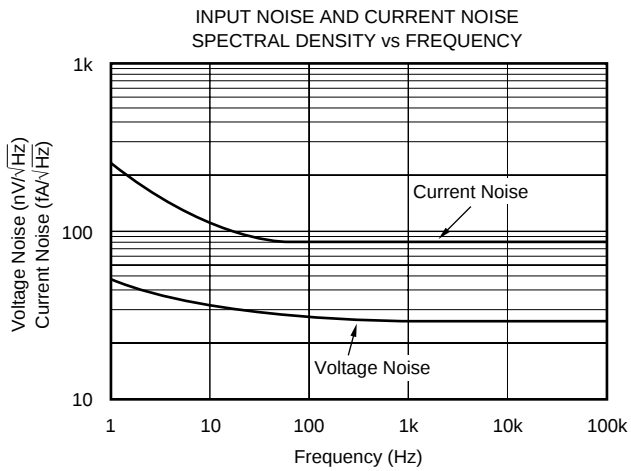
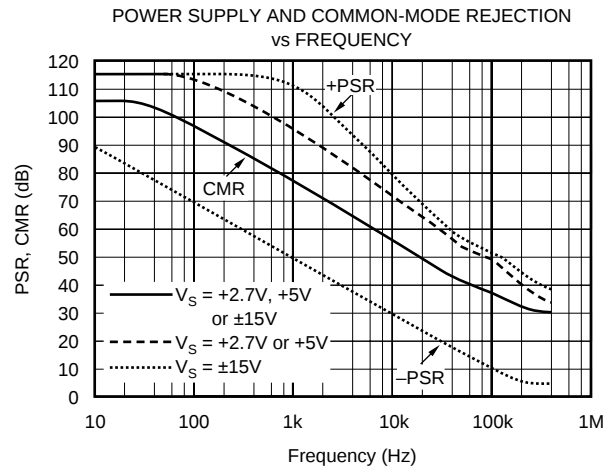
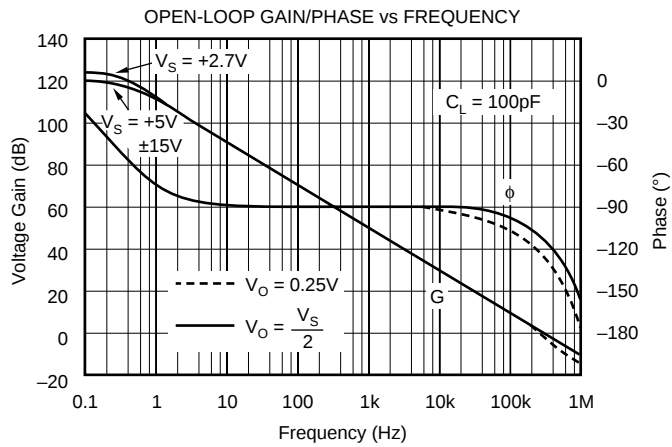
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
Single						
OPA234EA	MSOP-8 Surface-Mount	337	–40°C to +85°C	A34 ⁽²⁾	OPA234EA/250	Tape and Reel
OPA234E	MSOP-8 Surface-Mount	337	–40°C to +85°C	A34 ⁽²⁾	OPA234EA/2K5	Tape and Reel
OPA234PA	Plastic DIP-8	006	–40°C to +85°C	OPA234PA	OPA234E/250	Tape and Reel
OPA234P	SO-8 Surface-Mount	182	–40°C to +85°C	OPA234P	OPA234E/2K5	Tape and Reel
OPA234UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA234UA	OPA234PA	Rails
OPA234U	SO-8 Surface-Mount	182	–40°C to +85°C	OPA234UA	OPA234P	Rails
				OPA234UA	OPA234UA	Rails
				OPA234U	OPA234U	Rails
Dual						
OPA2234PA	Plastic DIP-8	006	–40°C to +85°C	OPA2234PA	OPA2234PA	Rails
OPA2234P	SO-8 Surface-Mount	182	–40°C to +85°C	OPA2234P	OPA2234P	Rails
OPA2234UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA2234UA	OPA2234UA	Rails
OPA2234U	SO-8 Surface-Mount	182	–40°C to +85°C	OPA2234U	OPA2234U	Rails
Quad						
OPA4234PA	Plastic DIP-8	006	–40°C to +85°C	OPA4234PA	OPA4234PA	Rails
OPA4234P	SO-8 Surface-Mount	182	–40°C to +85°C	OPA4234P	OPA4234P	Rails
OPA4234UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA4234UA	OPA4234UA	Rails
OPA4234U	SO-8 Surface-Mount	182	–40°C to +85°C	OPA4234U	OPA4234U	Rails

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA234E//2K5" will get a single 2500-piece Tape and Reel. (2) The grade will be marked on the Reel.

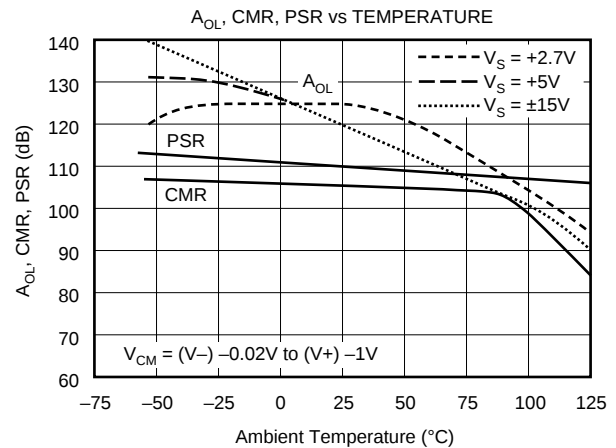
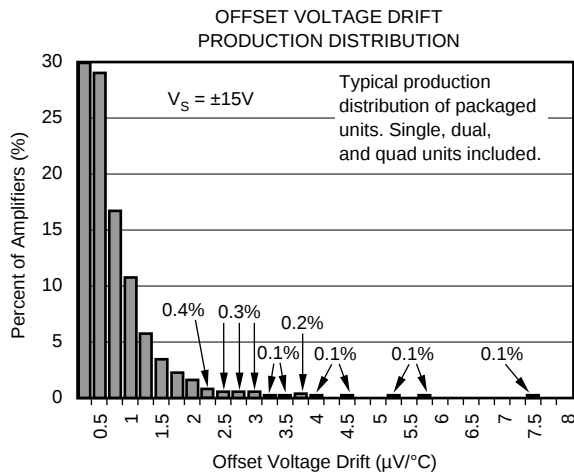
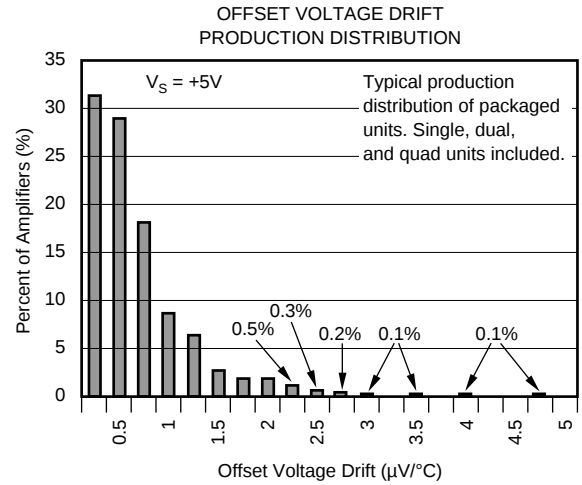
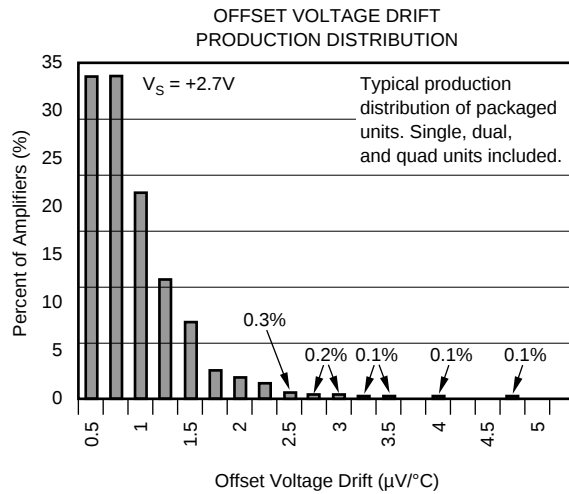
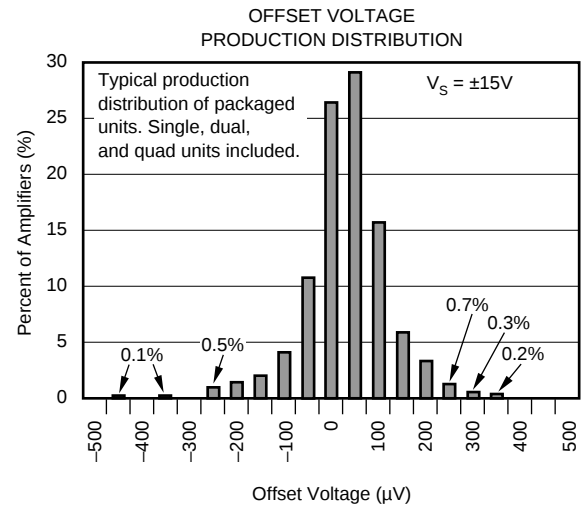
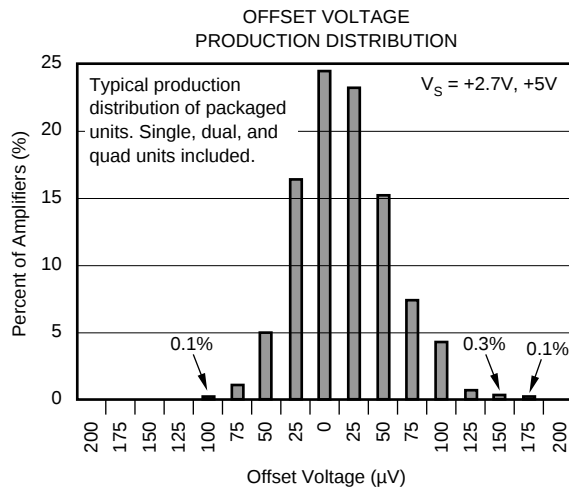
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$ and $R_L = 10\text{k}\Omega$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Cont.)

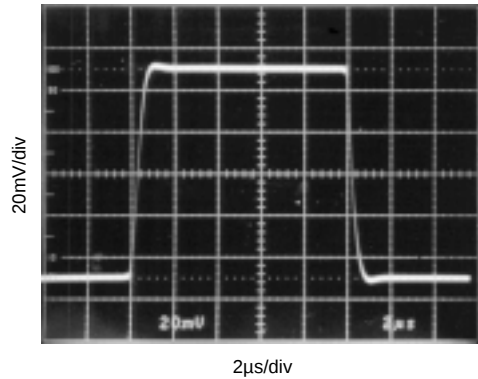
At $T_A = +25^\circ\text{C}$ and $R_L = 10\text{k}\Omega$ unless otherwise noted.



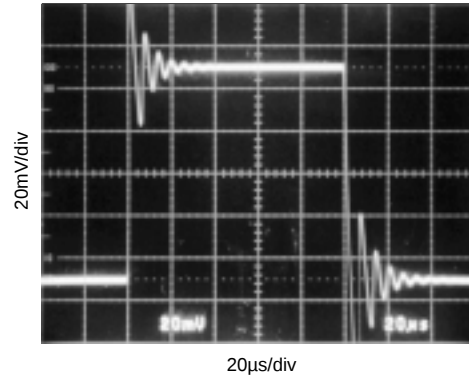
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$ and $R_L = 10\text{k}\Omega$ unless otherwise noted.

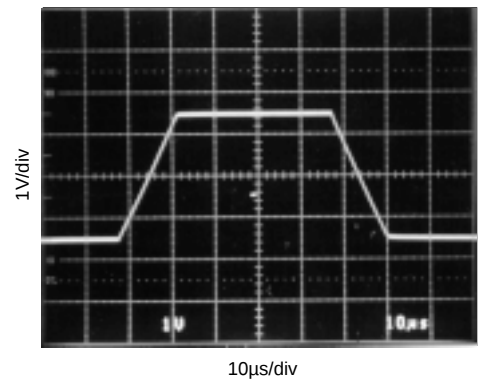
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$, $V_S = +5\text{V}$



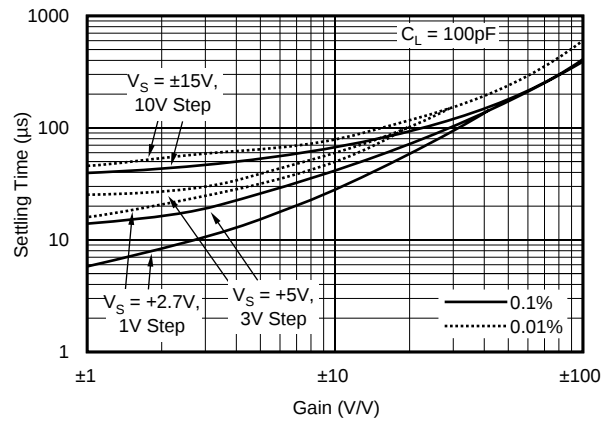
SMALL-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 10,000\text{pF}$, $V_S = +5\text{V}$



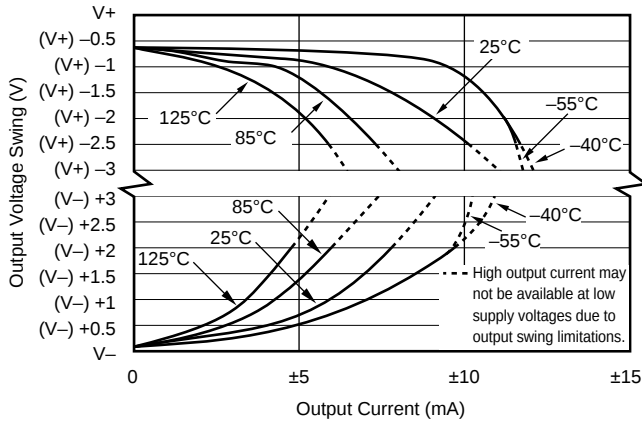
LARGE-SIGNAL STEP RESPONSE
 $G = 1$, $C_L = 100\text{pF}$, $V_S = +5\text{V}$



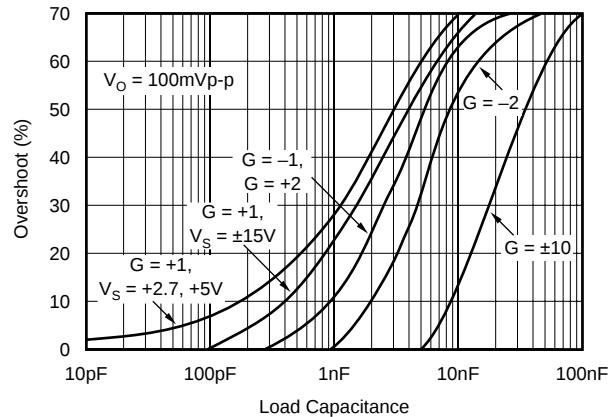
SETTLING TIME vs CLOSED-LOOP GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

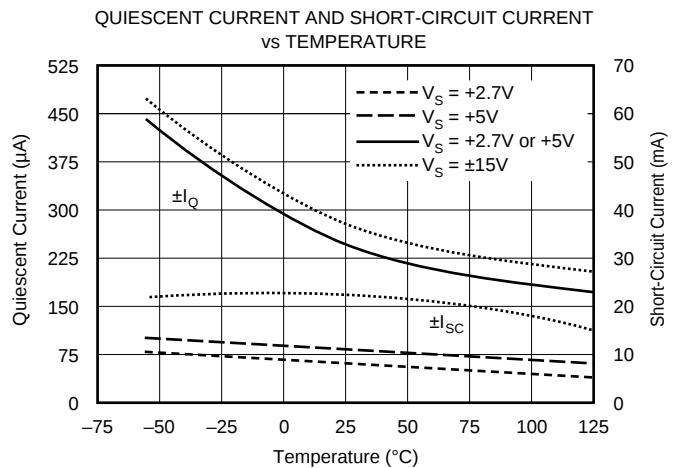
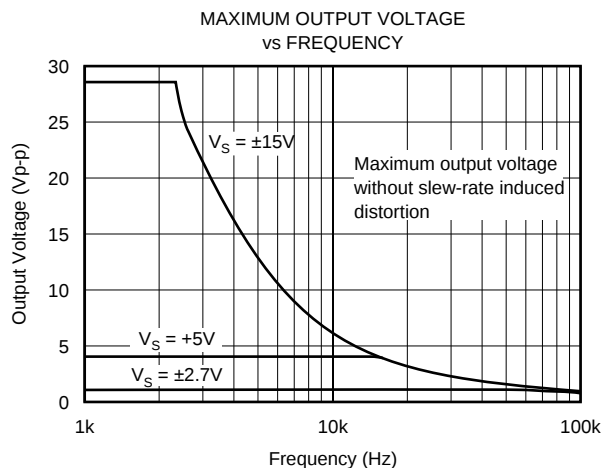


SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$ and $R_L = 10\text{k}\Omega$ unless otherwise noted.



APPLICATIONS INFORMATION

OPA234 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors.

OPERATING VOLTAGE

OPA234 series op amps operate from single (+2.7V to +36V) or dual ($\pm 1.35\text{V}$ to $\pm 18\text{V}$) supplies with excellent performance. Specifications are production tested with +2.7V, +5V, and $\pm 15\text{V}$ supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA234 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA234 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

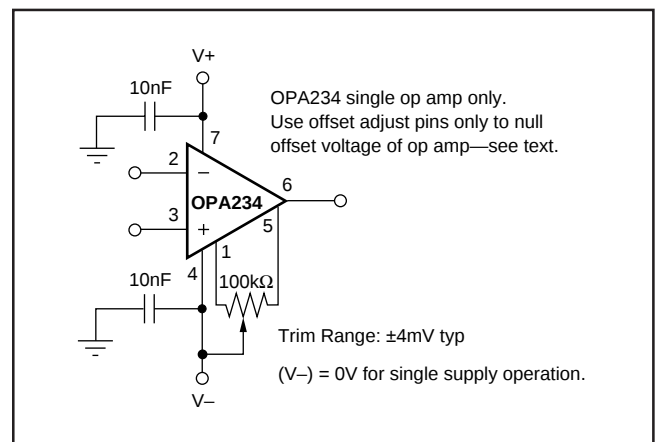


FIGURE 1. OPA234 Offset Voltage Trim Circuit.

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Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

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