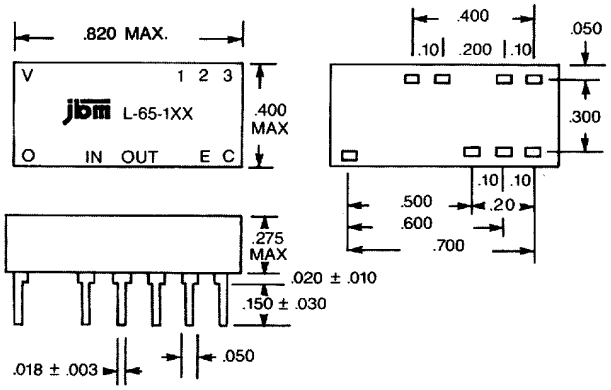
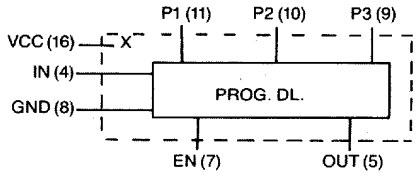
T-47-17

L-65-100 SERIES

TTL 3 Bit Programmables





DELAY LINE CHARACTERISTICS

Input Characteristics:

V_{IH} Logic "1" Input Voltage . . . . . 2.0V Min.
V_{IL} Logic "0" Input Voltage . . . . . .8V Max.
I_{IH} Logic "1" Input Current . . . . . 17mA Max.
I_{IL} Logic "0" Input Current . . . . . −5mA Max.

Output Characteristics:

V_{OH} Logic "1" Output Voltage . . . . . 2.4V Min.
V_{OL} Logic "0" Output Voltage . . . . . .4V Max.
I_{CC} . . . . . 45mA Max.
V_{CC} . . . . . 4.75 - 5.25 Volts

Environment:

Operating temperature . . . . . 0°C to 70°C
Storage temperature . . . . . −55°C to +125°C

Test Conditions:

Delays at 25°C with PWI @ 2× Programmed Delay with 5.0 VDC

DELAY SPECIFICATIONS IN (ns) NANOSECONDS													
Program Pins	3	0	0	0	0	1	1	1	1	Tol. of	Delay Time	Delay Time	Maximum Delay
Part	2	0	0	1	1	0	0	1	1	Prog.	Per	Step	Nominal
Number	1	0	1	0	1	0	1	0	1	Delay	Step	Tol.	Ref. IN
L-65-121	7 ± 1 ns	1	2	3	4	5	6	7	± .5 ns	1 ns	± .3 ns	14 ns
L-65-122	7 ± 1 ns	2	4	6	8	10	12	14	± .6 ns	2 ns	± .4 ns	21 ns
L-65-123	7 ± 1 ns	3	6	9	12	15	18	21	± .7 ns	3 ns	± .5 ns	28 ns
L-65-124	7 ± 1 ns	4	8	12	16	20	24	28	± .9 ns	4 ns	± .5 ns	35 ns
L-65-125	7 ± 1 ns	5	10	15	20	25	30	35	± 1 ns	5 ns	± .5 ns	42 ns
L-65-126	7 ± 1 ns	6	12	18	24	30	36	42	± 1.2 ns	6 ns	± .6 ns	49 ns
L-65-127	7 ± 1 ns	7	14	21	28	35	42	49	± 1.4 ns	7 ns	± .7 ns	56 ns
L-65-128	7 ± 1 ns	8	16	24	32	40	48	56	± 1.6 ns	8 ns	± .8 ns	63 ns
L-65-129	7 ± 1 ns	9	18	27	36	45	54	63	± 1.8 ns	9 ns	± .9 ns	70 ns
L-65-130	7 ± 1 ns	10	20	30	40	50	60	70	± 2.0 ns	10 ns	± 1 ns	77 ns
L-65-131	7 ± 1 ns	12	24	36	48	60	72	84	± 2.0 ns	12 ns	± 1.2 ns	91 ns

*Steps 1 to 7 Reference to Zero