



# FAST CMOS OCTAL TRANSCEIVER/ REGISTER (3-STATE)

**IDT54/74FCT646T/AT/CT**

## FEATURES:

- Std., A, and C grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - $V_{OH} = 3.3V$  (typ.)
  - $V_{OL} = 0.3V$  (typ.)
- High Drive outputs (-15mA  $I_{OH}$ , 64mA  $I_{OL}$ )
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Power off disable outputs permit "live insertion"
- Available in the following packages:
  - Industrial: SOIC, SSOP, QSOP
  - Military: CERDIP, LCC

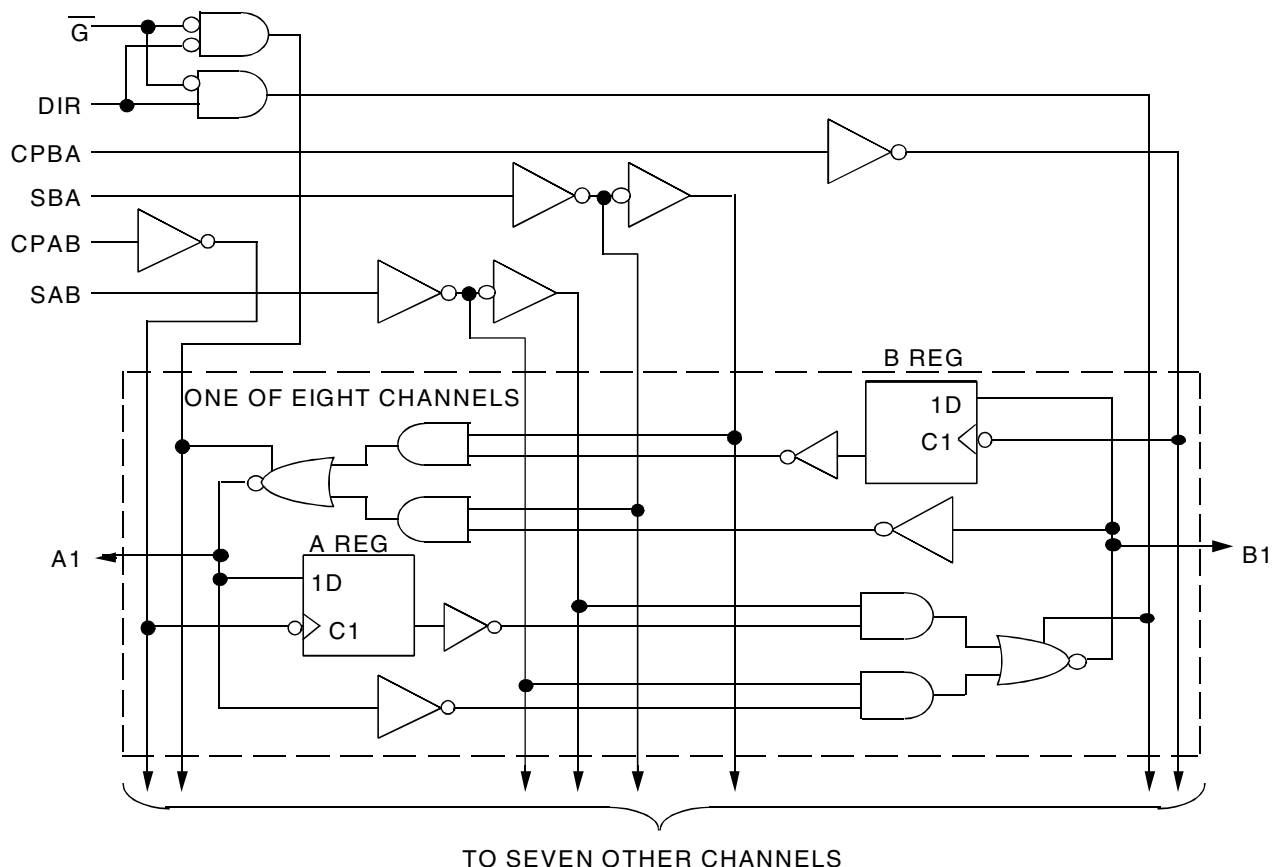
## DESCRIPTION:

The FCT646T consists of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The FCT646T utilizes the enable control ( $\bar{G}$ ) and direction (DIR) pins to control the transceiver functions.

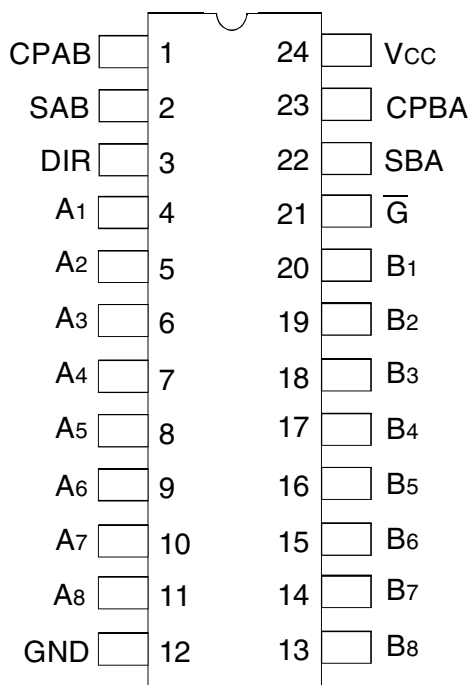
SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

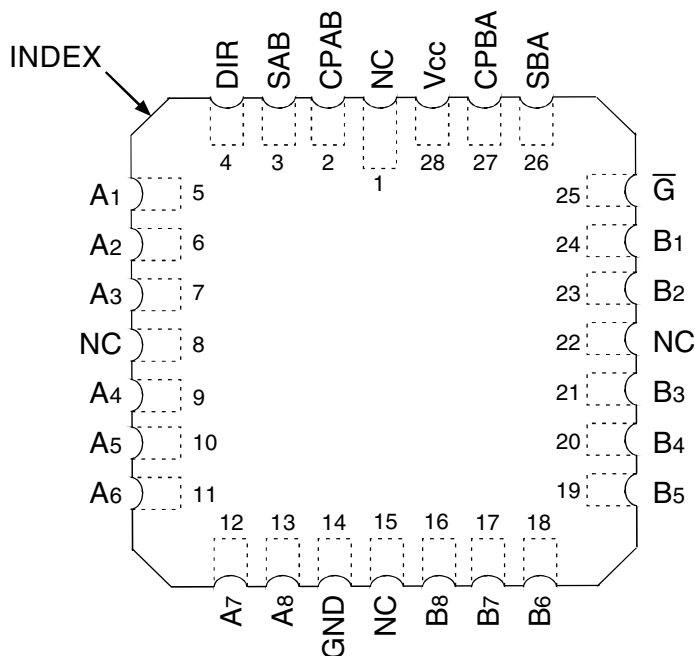
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



CERDIP/ SOIC/ SSOP/ QSOP  
TOP VIEW



LCC  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                           | Description                          | Max                          | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to +7                   | V    |
| V <sub>TERM</sub> <sup>(3)</sup> | Terminal Voltage with Respect to GND | -0.5 to V <sub>CC</sub> +0.5 | V    |
| T <sub>STG</sub>                 | Storage Temperature                  | -65 to +150                  | °C   |
| I <sub>OUT</sub>                 | DC Output Current                    | -60 to +120                  | mA   |

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Output and I/O terminals only.

## PIN DESCRIPTION

| Pin Names  | Description                                       |
|------------|---|
| A1 - A8    | Data Register A Inputs<br>Data Register B Outputs |
| B1 - B8    | Data Register B Inputs<br>Data Register A Outputs |
| CPAB, CPBA | Clock Pulse Inputs                                |
| SAB, SBA   | Output Data Source Select Inputs                  |
| DIR, G-bar | Output Enable Inputs                              |

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 6    | 10   | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 8    | 12   | pF   |

### NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE<sup>(1)</sup>

| Inputs    |     |        |        |     |     | Data I/O <sup>(2)</sup> |         | Operation or Function     |
|-----------|-----|--------|--------|-----|-----|-------------------------|---------|---------------------------|
| $\bar{G}$ | DIR | CPAB   | CPBA   | SAB | SBA | A1 - A8                 | B1 - B8 |                           |
| H         | X   | H or L | H or L | X   | X   | Input                   | Input   | Isolation                 |
| H         | X   | ↑      | ↑      | X   | X   |                         |         | Store A and B Data        |
| L         | L   | X      | X      | X   | L   | Output                  | Input   | Real-Time B Data to A Bus |
| L         | L   | X      | H or L | X   | H   |                         |         | Stored B Data to A Bus    |
| L         | H   | X      | X      | L   | X   | Input                   | Output  | Real-Time A Data to B Bus |
| L         | H   | H or L | X      | H   | X   |                         |         | Stored A Data to B Bus    |

NOTES:

- H = HIGH  
L = LOW  
X = Don't Care  
↑ = LOW-to-HIGH transition.  
Select control = L: clocks can occur simultaneously.  
Select control = H: clocks must be staggered in order to load both registers.
- The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- $\bar{A}$  in B Register.
- $\bar{B}$  in A Register.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

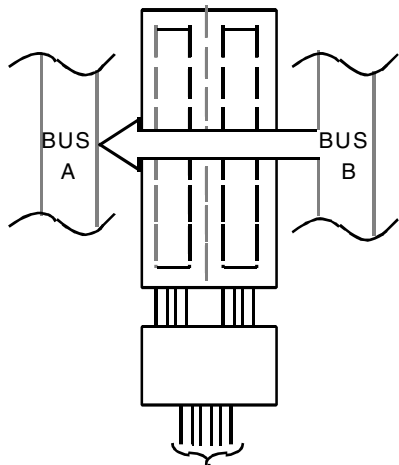
| Symbol    | Parameter   | Test Conditions <sup>(1)</sup>                         |                     | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|---|--|---------------------|------|---------------------|---------|---------------|
| $V_{IH}$  | Input HIGH Level  | Guaranteed Logic HIGH Level                            |                     | 2    | —                   | —       | V             |
| $V_{IL}$  | Input LOW Level   | Guaranteed Logic LOW Level                             |                     | —    | —                   | 0.8     | V             |
| $I_{IH}$  | Input HIGH Current <sup>(4)</sup>                                     | $V_{CC} = \text{Max.}$                                 | $V_I = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current <sup>(4)</sup>                                      | $V_{CC} = \text{Max.}$                                 | $V_I = 0.5\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZH}$ | High Impedance Output Current<br>(3-State output pins) <sup>(4)</sup> | $V_{CC} = \text{Max}$                                  | $V_O = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZL}$ |   |  | $V_O = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $I_I$     | Input HIGH Current <sup>(4)</sup>                                     | $V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$     |                     | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $V_{IK}$  | Clamp Diode Voltage   | $V_{CC} = \text{Min}, I_{IN} = -18\text{mA}$           |                     | —    | -0.7                | -1.2    | V             |
| $V_H$     | Input Hysteresis  | —  |                     | —    | 200                 | —       | mV            |
| $I_{CC}$  | Quiescent Power Supply Current  | $V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$ |                     | —    | 0.01                | 1       | $\mu\text{A}$ |

OUTPUT DRIVE CHARACTERISTICS

| Symbol    | Parameter                                     | Test Conditions <sup>(1)</sup>                                |  | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|---|---|--|------|---------------------|---------|---------------|
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -6\text{mA MIL}$<br>$I_{OH} = -8\text{mA IND}$   | 2.4  | 3.3                 | —       | V             |
|           |   |   | $I_{OH} = -12\text{mA MIL}$<br>$I_{OH} = -15\text{mA IND}$ | 2    | 3                   | —       |               |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 48\text{mA MIL}$<br>$I_{OL} = 64\text{mA IND}$   | —    | 0.3                 | 0.55    | V             |
| $I_{OS}$  | Short Circuit Current                         | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$                |  | -60  | -120                | -225    | mA            |
| $I_{OFF}$ | Input/Output Power Off Leakage <sup>(5)</sup> | $V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$ |  | —    | —                   | $\pm 1$ | $\mu\text{A}$ |

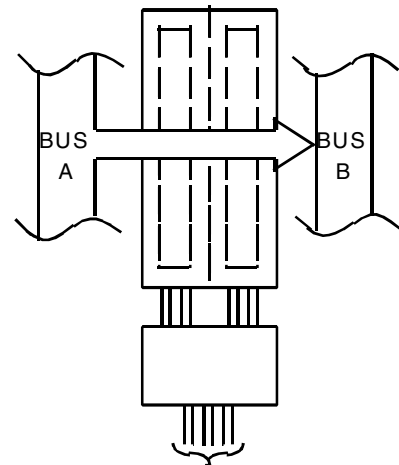
NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .
- This parameter is guaranteed but not tested.



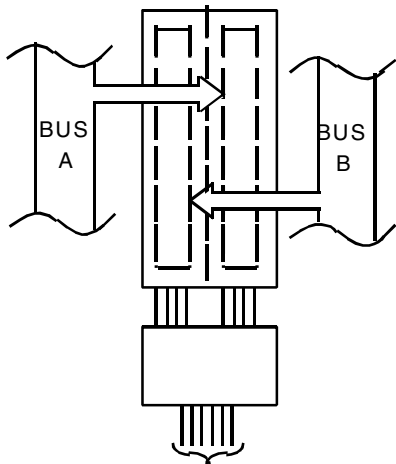
| DIR | $\bar{G}$ | CPAB | CPBA | SAB | SBA |
|-----|-----------|------|------|-----|-----|
| L   | L         | X    | X    | X   | L   |

*Real-Time Transfer  
Bus B to A*



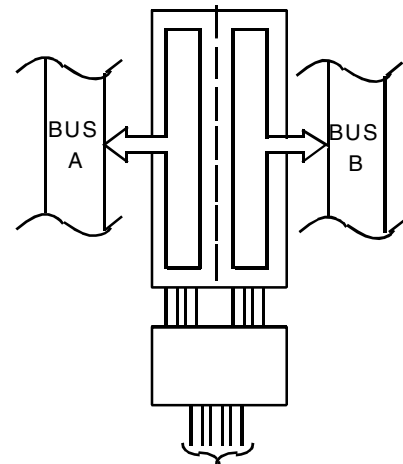
| DIR | $\bar{G}$ | CPAB | CPBA | SAB | SBA |
|-----|-----------|------|------|-----|-----|
| H   | L         | X    | X    | L   | X   |

*Real-Time Transfer  
Bus A to B*



| DIR | $\bar{G}$ | CPAB | CPBA | SAB | SBA |
|-----|-----------|------|------|-----|-----|
| H   | L         | ↑    | X    | X   | X   |
| L   | L         | X    | ↑    | X   | X   |
| X   | H         | ↑    | ↑    | X   | X   |

*Storage From  
A and/or B*



| DIR | $\bar{G}$ | CPAB   | CPBA   | SAB | SBA |
|-----|-----------|--------|--------|-----|-----|
| L   | L         | X      | H or L | X   | H   |
| H   | L         | H or L | X      | H   | X   |

*Transfer Stores<sup>(1)</sup>  
Data to A and/or B*

NOTE:

1. Cannot transfer data to A bus and B bus simultaneously.

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter   | Test Conditions <sup>(1)</sup>  |  | Min. | Typ. <sup>(2)</sup> | Max.                | Unit       |
|-----------------|---|---|--|------|---------------------|---------------------|------------|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC} = \text{Max.}$<br>$V_{IN} = 3.4V^{(3)}$   |  | —    | 0.5                 | 2                   | mA         |
| $I_{CCD}$       | Dynamic Power Supply<br>Current <sup>(4)</sup>    | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$\bar{G} = \text{DIR} = \text{GND}$<br>One Input Toggling<br>50% Duty Cycle   | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 0.15                | 0.25                | mA/<br>MHz |
| $I_C$           | Total Power Supply Current <sup>(6)</sup>         | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\bar{G} = \text{DIR} = \text{GND}$<br>One Bit Toggling<br>at $f_i = 5\text{MHz}$      | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 1.5                 | 3.5                 | mA         |
|                 |   |   | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 2                   | 5.5                 |            |
|                 |   | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\bar{G} = \text{DIR} = \text{GND}$<br>Eight Bits Toggling<br>at $f_i = 2.5\text{MHz}$ | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 3.8                 | 7.3 <sup>(5)</sup>  |            |
|                 |   |   | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 6                   | 16.3 <sup>(5)</sup> |            |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
  - Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
  - Per TTL driven input; ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
  - This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
  - Values for these conditions are examples of  $\Delta I_{CC}$  formula. These limits are guaranteed but not tested.
  - $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_i$  = Output Frequency  
 $N_i$  = Number of Outputs at  $f_i$
- All currents are in milliamps and all frequencies are in megahertz.

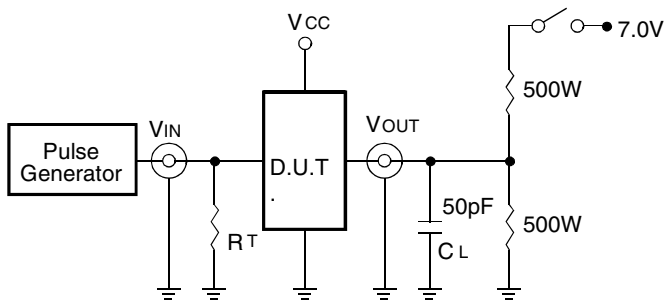
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol                               | Parameter                                | Condition <sup>(1)</sup>                       | 54FCT646T           |      | 54/74FCT646AT       |      |                     |      | 54/74FCT646CT       |      |                     |      | Unit |
|--------------------------------------|--|--|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
|                                      |  |  | Mil.                |      | Ind.                |      | Mil.                |      | Ind.                |      | Mil.                |      |      |
|                                      |  |  | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay,<br>Bus to Bus         | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2                   | 11   | 2                   | 6.3  | 2                   | 7.7  | 1.5                 | 5.4  | 1.5                 | 6    | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time,<br>G̅, DIR to Bus    |  | 2                   | 15   | 2                   | 9.8  | 2                   | 10.5 | 1.5                 | 7.8  | 1.5                 | 8.9  | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time,<br>G̅, DIR to Bus   |  | 2                   | 11   | 2                   | 6.3  | 2                   | 7.7  | 1.5                 | 6.3  | 1.5                 | 7.7  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay,<br>Clock to Bus       |  | 2                   | 10   | 2                   | 6.3  | 2                   | 7    | 1.5                 | 5.7  | 1.5                 | 6.3  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay,<br>SBA or SAB to Bus  |  | 2                   | 12   | 2                   | 7.7  | 2                   | 8.4  | 1.5                 | 6.2  | 1.5                 | 7    | ns   |
| t <sub>SU</sub>                      | Set-up Time HIGH or LOW,<br>Bus to Clock |  | 4.5                 | —    | 2                   | —    | 2                   | —    | 2                   | —    | 2                   | —    | ns   |
| t <sub>H</sub>                       | Hold Time HIGH or LOW,<br>Bus to Clock   |  | 2                   | —    | 1.5                 | —    | 1.5                 | —    | 1.5                 | —    | 1.5                 | —    | ns   |
| t <sub>w</sub>                       | Clock Pulse Width,<br>HIGH or LOW        |  | 6                   | —    | 5                   | —    | 5                   | —    | 5                   | —    | 5                   | —    | ns   |

NOTES:

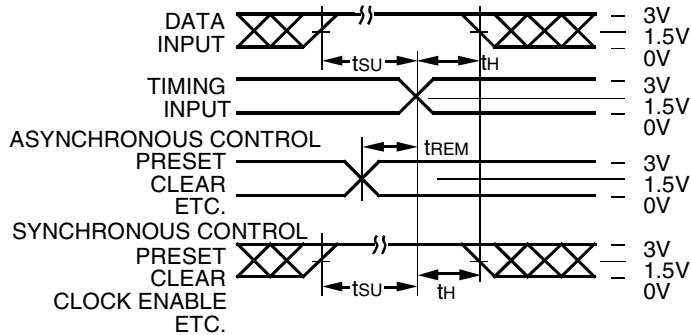
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

## TEST CIRCUITS AND WAVEFORMS



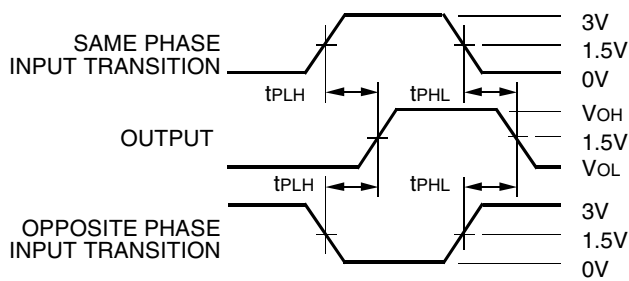
Octal Link

*Test Circuits for All Outputs*



Octal Link

*Set-Up, Hold, and Release Times*



Octal Link

*Propagation Delay*

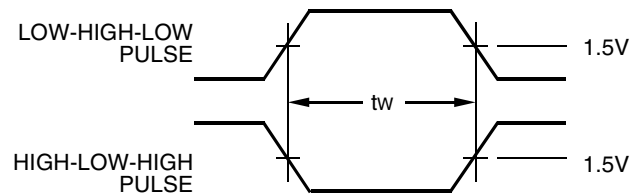
## SWITCH POSITION

| Test                                    | Switch |
|---|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

### DEFINITIONS:

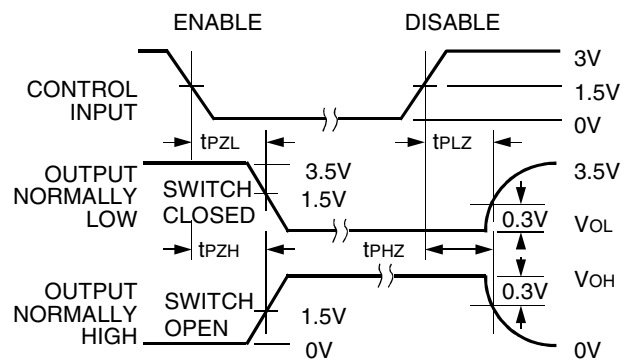
$C_L$  = Load capacitance: includes jig and probe capacitance.

$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.



*Pulse Width*

Octal Link



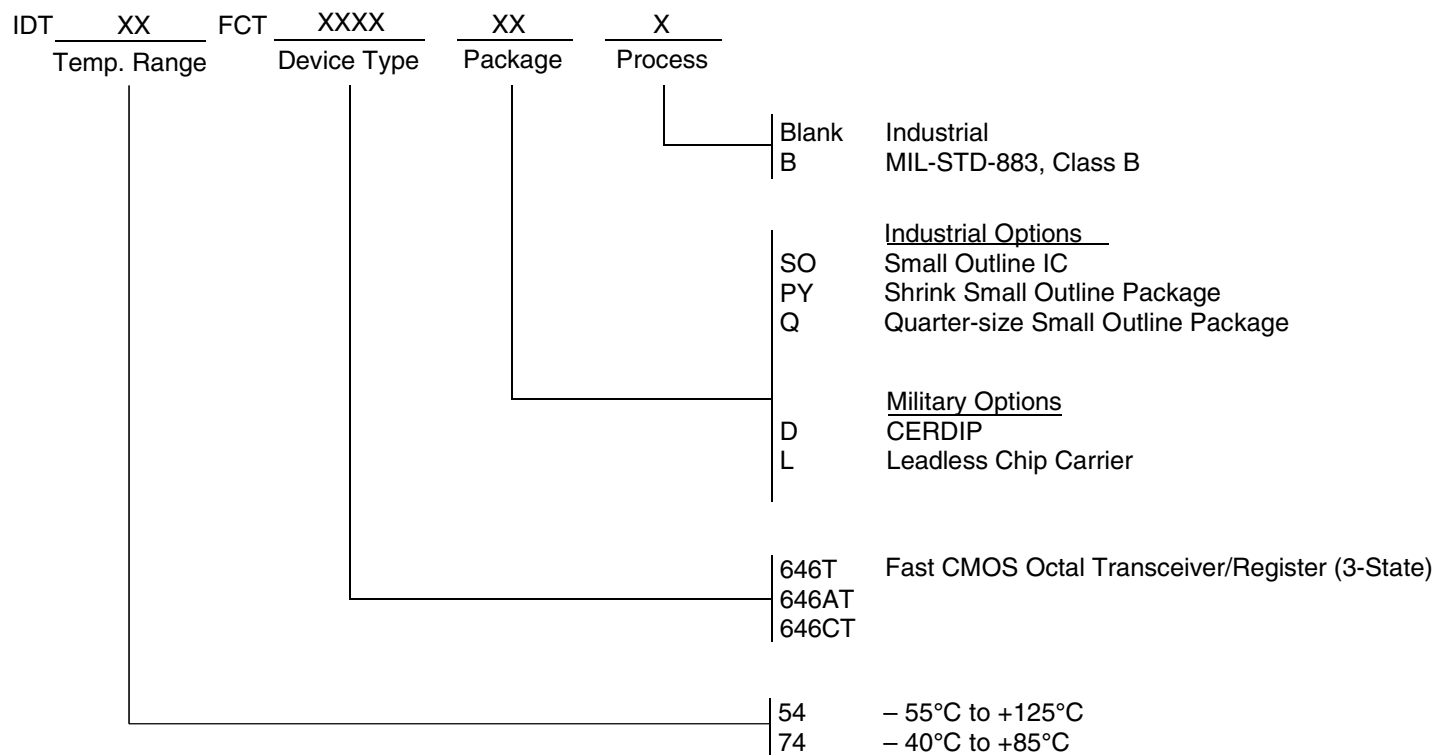
Octal Link

*Enable and Disable Times*

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
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 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
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**for Tech Support:**  
 logichelp@idt.com  
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