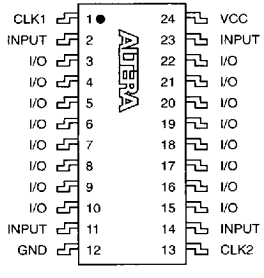
Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 100 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 Clock pins
- The following devices are pin-, function-, and programming file-compatible: EP610, EP610I, EP610T, EP610 MIL-STD-883-compliant, EP600I, and PALCE610
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 7):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

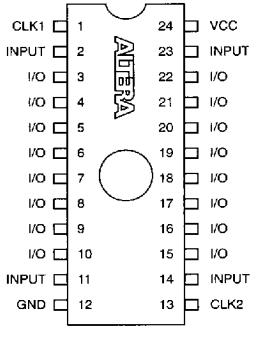
Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



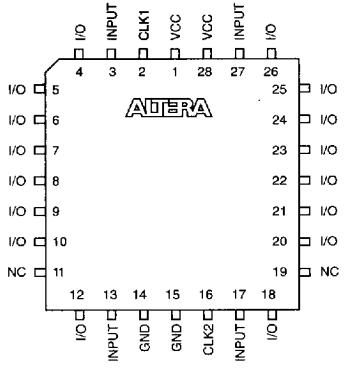
24-Pin SOIC

EP610
EP610T



24-Pin DIP

EP610
EP610T
EP610 MIL-STD-883-Compliant
EP610I



28-Pin J-Lead

EP610
EP610T
EP610I

Table 2 summarizes EP610 device features.

Table 2. EP610 Device Features

Feature	EP610	EP610T	EP610 MIL-STD-883-Compliant	EP610I
t_{PD}	15 ns	15 ns	35 ns	10 ns
Counter frequency	83 MHz	83 MHz	28.5 MHz	100 MHz
Pipeline data rates	83 MHz	83 MHz	37 MHz	100 MHz
Packages	24-pin SOIC 24-pin CerDIP 24-pin PDIP 28-pin PLCC	24-pin SOIC 24-pin PDIP 28-pin PLCC	24-pin CerDIP	24-pin CerDIP 24-pin PDIP 28-pin PLCC

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global Clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLK1 is a dedicated Clock input for the registers in macrocells 9 through 16. CLK2 is a dedicated Clock input for registers in macrocells 1 through 8.

Figure 8. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

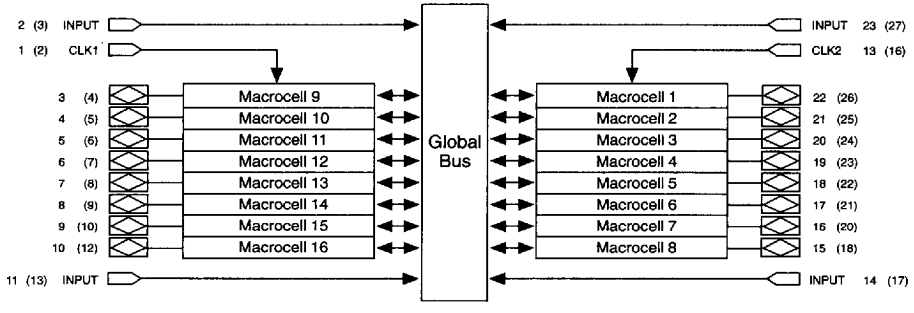
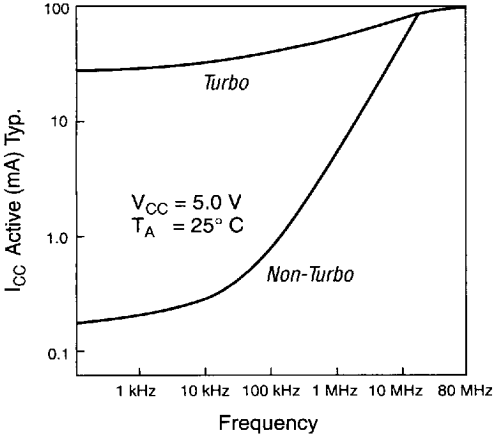


Figure 9 shows the typical supply current (I_{CC}) versus frequency for EP610 devices.

Figure 9. EP610 I_{CC} vs. Frequency

EP610 & EP610 MIL-STD-883-Compliant EPLDs



EP610T EPLDs

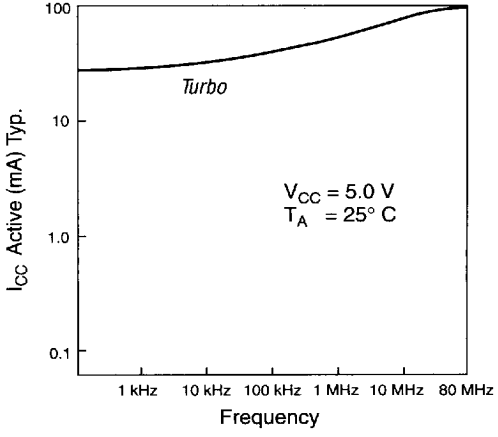
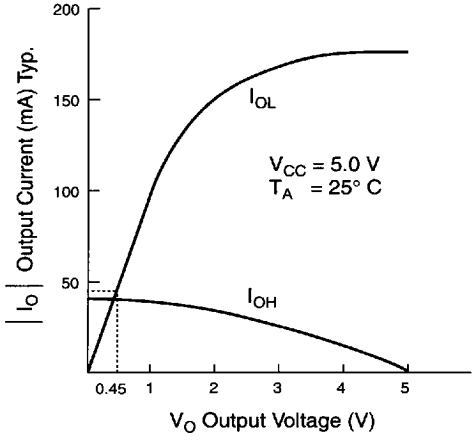


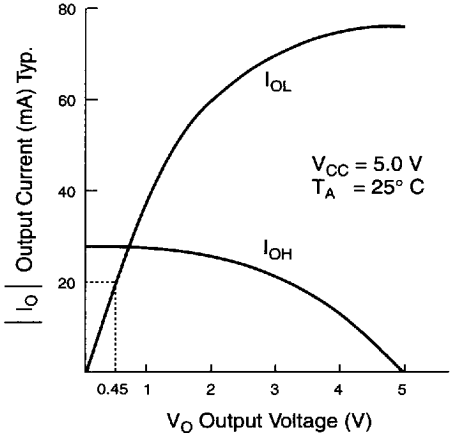
Figure 10 shows the maximum output drive characteristics of EP610 I/O pins.

Figure 10. EP610 Output Drive Characteristics

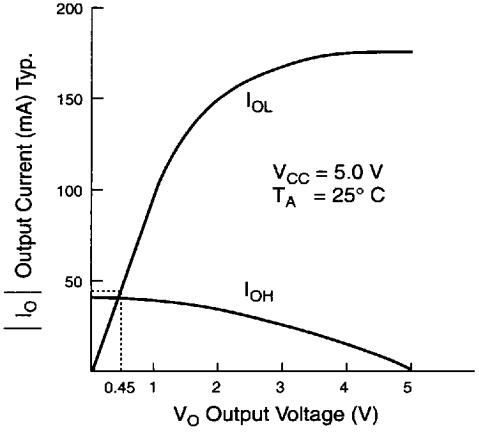
EP610-15 & EP610-20 EPLDs



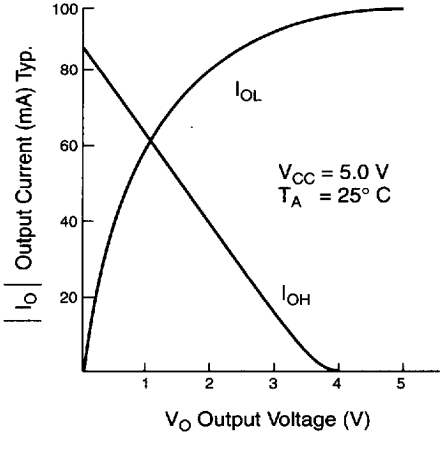
EP610-25, EP610-25T, EP610-30 & EP610-35



EP610-15T & EP610-20T EPLDs



EP610I EPLDs



Absolute Maximum Ratings *Note (1)*

			EP610 EP610T EP610 MIL-STD-883-Compliant		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC}+ 0.5	V
I_{MAX}	DC V_{CC} or GND current		–175	175			mA
I_{OUT}	DC output current, per pin		–25	25			mA
P_D	Power dissipation			1,000			mW
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (3)*	–65	135 (125)	–10	85	° C
T_J	Junction temperature	Under bias, *Note (3)*		(150)			° C

Recommended Operating Conditions *Note (4)*

			EP610 EP610T EP610 MIL-STD-883-Compliant		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Notes (3), (5)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	–40	85	° C
T_C	Case temperature	For military use	–55	125			° C
t_R	Input rise time	*Notes (3), (6)*		100 (50)		500	ns
t_F	Input fall time	*Notes (3), (6)*		100 (50)		500	ns

DC Operating Conditions *Notes (3), (4), (7)*

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (8)*	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10		10	µA

Capacitance *Note (9)*

			EP610 EP610T		EP610 MIL-STD-883-Compliant		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		12	pF

I_{CC} Supply Current: EP610 & EP610T *Note (7)*

				EP610			EP610T			
Symbol	**Parameter**	**Conditions**	**Speed Grade**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Notes (10), (11), (12)*			20	150				µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (3), (12)*			5	10 (15)				mA
I_{CC3}	V_{CC} supply current (turbo, active)	*Notes (3), (11), (12)*	-15, -20		60	90 (115)		60	90	mA
			-25, -30, -35		45	60 (75)		60	90	mA

I_{CC} Supply Current: EP610 MIL-STD-883-Compliant & EP610I *Note (7)*

			EP610 MIL-STD-883-Compliant			EP610I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, no load, *Notes (10), (11), (12)*			900		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (10), (12)*			25		3	8	mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (10), (12)*			140		65	105	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15, EP610-15T, EP610-20, and EP610-20T EPLDs: maximum V_{PP} = 14.0 V.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_A = –55° C to 125° C for military use.
(5) For EP610, EP610T, and EP610 MIL-STD-883-compliant devices, maximum V_{CC} rise time is 50 ms. For EP610I devices, V_{CC} rise time is unlimited with monotonic rise.
(6) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns.
For EP610-15 and EP610-20 Clocks: t_R and t_F = 20 ns.
(7) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(8) For EP610 MIL-STD-883-compliant, tested at maximum operating temperature only.
(9) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. For EP610-25, EP610-30, EP610-35, EP610-25T, and EP610 MIL-STD-833 EPLDs: Pin 13 has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(10) When the Turbo Bit is not set (non-turbo mode), an EP610 EPLD enters standby mode if no logic transitions occur for 100 ns after the last transition.
(11) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.
(12) For EP610 MIL-STD-883-compliant, tested with non-output loading using a data pattern specified by Altera. Data path is programmed as a 16-bit counter.

AC Operating Conditions: EP610-15 & EP610-20 *Notes (1), (2)*

			EP610-15 EP610-15T		EP610-20 EP610-20T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17		22	20	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns
f_{MAX}	Maximum clock frequency	*Note (5)*	83.3		62.5		0	MHz
t_{SU}	Global clock input setup time		9		11		20	ns
t_{H}	Global clock input hold time		0		0		0	ns
t_{CH}	Global clock high time		6		8		0	ns
t_{CL}	Global clock low time		6		8		0	ns
t_{CO1}	Global clock to output delay			11		13	0	ns
t_{CNT}	Global clock minimum period			12		16	0	ns
f_{CNT}	Global clock internal maximum frequency	*Note (6)*	83.3		62.5		0	MHz
t_{ASU}	Array clock input setup time		6		8		20	ns
t_{AH}	Array clock input hold time		6		8		0	ns
t_{ACH}	Array clock high time		7		9		0	ns
t_{ACL}	Array clock low time		7		9		0	ns
t_{ACO1}	Array clock to output delay			15		20	20	ns
t_{ACNT}	Array clock minimum period			14		18	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	71.4		55.6		0	MHz

AC Operating Conditions: EP610-25, EP610-30 & EP610-35 *Notes (1), (2)*

			EP610-25 EP610-25T		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns
f_{MAX}	Maximum frequency	*Note (5)*	47.6		41.7		37.0		0	MHz
t_{SU}	Global clock input setup time		21		24		27		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		10		11		12		0	ns
t_{CL}	Global clock low time		10		11		12		0	ns
t_{CO1}	Global clock to output delay			15		17		20	0	ns
t_{CNT}	Global clock minimum period			25		30		35	0	ns
f_{CNT}	Global clock internal maximum frequency	*Note (6)*	40.0		33.3		28.6		0	MHz
t_{ASU}	Array clock input setup time		8		8		8		30	ns
t_{AH}	Array clock input hold time		12		12		12		0	ns
t_{ACH}	Array clock high time		10		11		12		0	ns
t_{ACL}	Array clock low time		10		11		12		0	ns
t_{ACO1}	Array clock to output delay			27		32		37	30	ns
t_{ACNT}	Array clock minimum period			25		30		35	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	40.0		33.3		28.6		0	MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.
$V_{CC} = 5\ V \pm 10\%$, $T_C = -55°\ C$ to $125°\ C$ for military use.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) See "Turbo Bit" on page 336 of this data sheet. EP610T devices do not have a non-turbo mode.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.

AC Operating Conditions: EP610 MIL-STD-883-Compliant *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		35	ns
t_{PD2}	I/O input to non-registered output	*Notes (3), (4)*		37	ns
t_{PZX}	Input to output enable			35	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Notes (3), (4), (5), (6)*		35	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF, *Notes (3), (4)*		37	ns
f_{MAX}	Maximum frequency	*Notes (3), (7), (8)*	37.0		MHz
t_{SU}	Global clock input setup time	*Notes (3), (4)*	27		ns
t_{H}	Global clock input hold time	*Note (3)*	0		ns
t_{CH}	Global clock high time	*Note (5)*	12		ns
t_{CL}	Global clock low time	*Note (5)*	12		ns
t_{CO1}	Global clock to output delay			20	ns
t_{CNT}	Global clock minimum period	*Notes (5), (9)*		35	ns
f_{CNT}	Global clock internal maximum frequency	*Note (9)*	28.5		MHz
t_{ASU}	Array clock input setup time	*Notes (3), (4), (5)*	8		ns
t_{AH}	Array clock input hold time	*Notes (3), (4), (5)*	12		ns
t_{ACH}	Array clock high time	*Notes (4), (5)*	12		ns
t_{ACL}	Array clock low time	*Notes (4), (5)*	12		ns
t_{ACO1}	Array clock to output delay	*Notes (3), (4)*		37	ns
t_{ACNT}	Array clock minimum period	*Notes (5), (9)*		35	ns
f_{ACNT}	Array clock internal maximum frequency	*Notes (5), (9)*	28.6		MHz

Notes to tables:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) All array-dependent delays are specified for an XOR pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM cell. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an XOR pattern in which only one pure input switches at a time.

(4) When the Turbo Bit is not set (non-turbo mode), a non-turbo adder of 30 ns (maximum) is added to this parameter to determine worst-case timing. Parameters may not be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.

(5) These parameters may not be tested, but are guaranteed to the limits specified in the table under "Absolute Maximum Ratings" on page 349.

(6) Not tested directly, but guaranteed by testing t_{PD}.

(7) The f_{MAX} values represent the highest frequency for pipelined data.

(8) Not tested directly, but derived from t_{SU}.

(9) Specified with device programmed as a 16-bit counter with no output loading.

AC Operating Conditions: EP610I *Notes (1), (2)*

		EP610I-10		EP610I-15		EP610I-25		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Units**
t_{PD1}	Input to non-registered output, *Note (4)*		10		15		25	25	ns
t_{PD2}	I/O input to non-registered output, *Note (4)*		10		15		25	25	ns
t_{PZX}	Input to output enable		15		18		25	25	ns
t_{PXZ}	Input to output disable, *Note (5)*		13		18		25	25	ns
t_{CLR}	Asynchronous output clear time		13		18		25	25	ns
f_{MAX}	Maximum frequency	111		83.3		66		0	MHz
t_{SU}	Global clock input setup time	7		12		15		25	ns
t_{H}	Global clock input hold time	0		0		0		0	ns
t_{CH}	Global clock high time	5		6		7.5		0	ns
t_{CL}	Global clock low time	5		6		7.5		0	ns
t_{CO1}	Global clock to output delay		6.5		8		10		ns
t_{CNT}	Global clock minimum period		10		15		25	25	ns
f_{CNT}	Global clock internal maximum frequency, *Note (6)*	100		66		40		0	MHz
t_{ASU}	Array clock input setup time	2		4		5		25	ns
t_{AH}	Array clock input hold time	3		6		8		0	ns
t_{ACH}	Array clock high time	5		7.5		10		0	ns
t_{ACL}	Array clock low time	5		7.5		10		0	ns
t_{ACO1}	Array clock to output delay		12		16		25	25	ns
t_{ACNT}	Array clock minimum period, *Note (6)*		10		15		25	25	ns
f_{ACNT}	Array clock internal maximum frequency, *Note (6)*	100		66		40		0	MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) See "Turbo Bit" on page 336 of this data sheet.

(4) Measured with eight outputs switching.

(5) Sample-tested only for an output change of 500 mV.

(6) Measured with a device programmed as a 16-bit counter.