STC9120C/M

CMOS 1,200 bps MSK MODEM

- **Minimum External Parts Required**
- **1200 bps for Full-duplex or Half-duplex System**
- **Low Supply Current**
- **On-chip Carrier Detector**

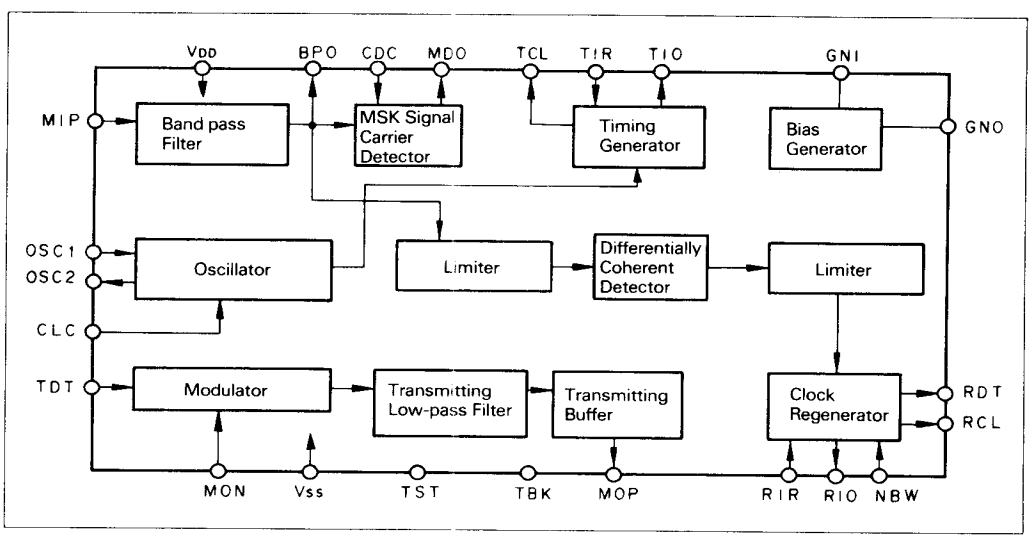
■ DESCRIPTION

The STC9120C/M is a single chip CMOS 1200 bps MSK MODEM for full-duplex or half-duplex radio communication equipment. The modulator provides a low-distrotion sinusoidal output and a sync clock output. A receiving low-pass filter, a differentially coherent detector and a clock regenerator makes up the demodulator incorporating a MSK signal carrier detector, the STC9120C/M offers a high-performance MSK MODEM with a minimum of external parts.

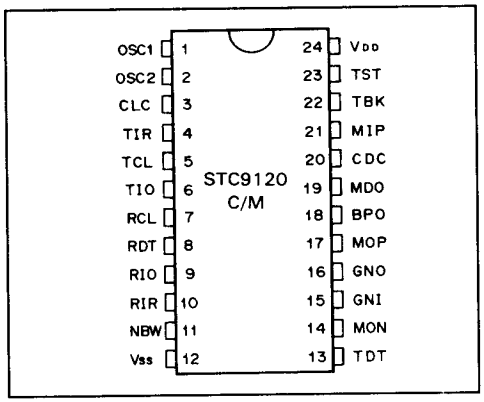
■ FEATURES

- 1200 bps full-duplex/half-duplex MSK MODEM
- Low supply current
- 5.5296 MHz crystal oscillator, or external 5.5296 MHz clock input
- Minimized external parts
- Built-in MSK signal carrier detect circuit
- TTL compatible input/output (except for terminals OSC1, OSC2, CLC, TBK and TST)
- Transmitting/receiving filter based on SCF (Switched Capacitor Filter) technology
- Little group delay distortion at the pass band
- Single power supply (+5V)
- Package····STC9120C 24-pin DIP(plastic)
  STC9120M 24-pin SOP(plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION (common to DIP and SOP)



■ PIN DESCRIPTION

Pin name	Pin No.	Functions
OSC1	1	5.5296 MHz (CLC = "L") or 2.7648 MHz (CLC = "H") crystal oscillator circuit or external clock input terminal.
OSC2	2	Crystal oscillator output terminal
CLC*1	3	Input teminal for oscillator frequency division control (with pull-down resistor)
TIR*2	4	Input terminal that resets the 1-bit data transmit interruption flip-flop (without pull-down resistor)
TCL	5	Transmit data sync clock signal output terminal
TIO	6	Output terminal for the 1-bit data transmit interruption flip-flop
RCL	7	Output terminal of sync clock signals regenerated from demodulated data
RDT	8	Output terminal of demodulated receive data
RIO	9	Output terminal for the 1-bit data receive interruption flip-flop
RIR*2	10	Input terminal that resets the 1-bit data receive interruption flip-flop (without pull-down resistor)
NBW*2	11	Input terminal that controls selection of DPLL circuit lock-in range (narrow/wide) (without pull-down resistor) Narrow..... high level Wide..... low level
Vss	12	Supply voltage (0V)
TDT*2	13	Input terminal of NRZ signals to be transmitted (without pull-down resistor)
MON*2	14	Input terminal for MSK signal transmit control (without pull-down resistor)
GNI	15	Input terminal of intermediate point reference voltage for power supply
GNO	16	Output terminal of intermediate point reference voltage for built-in operational amplifier
MOP	17	MSK signal output terminal
BPO	18	Receiving band low-pass filter output monitor terminal (normally non-connected)
MDO	19	MSK signal carrier detector output terminal
CDC	20	Input terminal for application of offset voltage to set MSK signal carrier detection threshold value (with C-R connected externally)
MIP	21	MSK signal input terminal
TBK*1	22	Function test terminal (normally non-connected; with pull-down resistor)
TST*1	23	Function test terminal (normally non-connected; with pull-down resistor)
VDD	24	Supply voltage (+5V)

*1 These input terminals are pulled down with a resistor, typically 500 kΩ. It is recommended that they are directly pulled down to VDD not left open, when they are not used, regarding to noise effect.

*2 These input terminals are input gate floating type. When not used, they must be directly pulled down to Vss not left open.

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0V, Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	−0.3 to 8.0	V
Input voltage*	VI	−0.3 to VDD +0.3	V
Output voltage	VO	−0.3 to VDD +0.3	V
Power dissipation	PD (Max)	500	mW
Operating temperature	Topr	−25 to 70	°C
Storage temperature	Tstg	−65 to 150	°C
Soldering temperature and time	Tsol	260°C, 10 s (at lead)	−

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD} = 5.0V, V_{SS} = 0V and Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
Supply current	I_{DD}	f_{OSC} = 5.5296 MHz		–	6	12	mA
"L" level input voltage	V_{IL1}	OSC1		V_{SS}	–	V_{SS} +0.3	V
"H" level input voltage	V_{IH1}			V_{DD} –0.3	–	V_{DD}	V
Input frequency	F_{I1}			–	5.5296	–	MHz
Input current	I_{I1}		V_{IH1} = 5V	–	0.5	–	μA
"L" level input voltage	V_{IL2}	CLC, TBK, TST		V_{SS}	–	V_{SS} +0.3	V
"H" level input voltage	V_{IH2}			V_{DD} –0.3	–	V_{DD}	V
Pull-down resistance	R_{I2}			200	500	1250	KΩ
"L" level input voltage	V_{IL3}	NBW, RIR*3, RIE*3 TDT,		0	–	0.8	V
"H" level input voltage	V_{IH3}	MON		2.4	–	V_{DD}	V
Input impedance	R_{I4}	MIP		70	120	190	kΩ
Input signal voltage	V_{I4}		Sinewave input	–	1.0	2.0*4	V_{P-P}
"L" level output voltage	V_{OL1}	RCL, RDT RIO, MDO	I_{OL1}=2.6mA	V_{SS}	–	0.5	V
"H" level output voltage	V_{OH1}	TCL, TIO	I_{OH1}= –0.2 mA	4.6	–	V_{DD}	V
Mark output voltage	V_{OM}	Load resistance: Min 10 kΩ		0.9	1.0	1.1	V_{P-P}
Space signal output voltage	V_{OS}			0.9	1.0	1.1	V_{P-P}

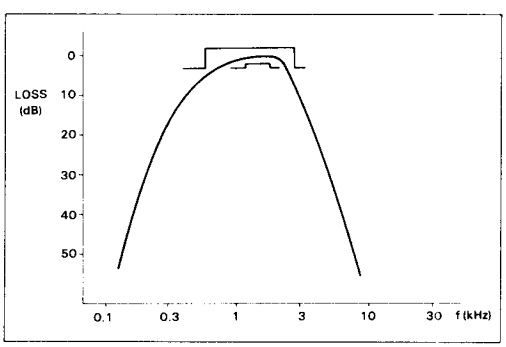
*3 The reset pulse width must be at least 1 μs.

*4 The maximum input level should be adjusted not so as to happen a malfunction.

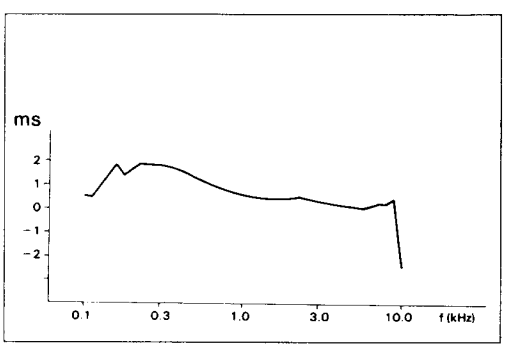
● Filter Specifications

(V_{DD} = 5.0V, V_{SS} = 0V and Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
3 dB band width (Low Band)	F_{CL1}	Receiving band-pass filter	600	700	800	Hz
3 dB band width (High Band)	F_{CH1}	Butterworth	2000	2400	2800	Hz
Insertion loss	L_{B1}	10 order	–2	0	2	dB
3 dB band width (High Band)	F_{C2}	Transmitting low band-pass	4250	5000	5750	Hz
Insertion loss	L_{B2}	filter Butterworth 5 order	–2	0	2	dB
3 dB band width (High Band)	F_{C3}	Receiving low band-pass filter	1000	1200	1400	Hz
Insertion loss	L_{B3}	Butterworth 3 order	–2	0	2	dB



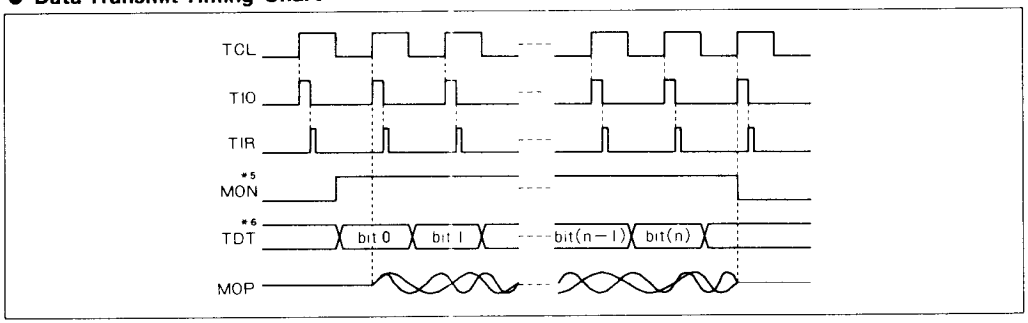
Band Pass Filter Frequency Characteristics



Band Pass Filter Group Delay Characteristics

■ DATA INPUT/OUTPUT TIMING CHART

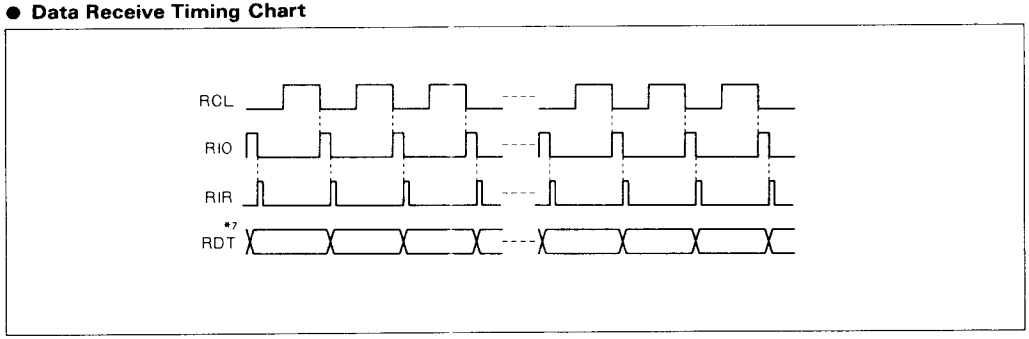
● Data Transmit Timing Chart



*5 When data transmission starts, MON must go to "H" level within about 833 μs following the leading edge of the TCL. When the data transmission ends, MON must go to "L" level at the leading edge of the next TCL following the transmission of the last bit of MOP.

*6 For TDT, data must be set within about 833 μs after the occurrence of an interrupt.

● Data Receive Timing Chart



*7 RDT must be read within about 833 μs following the leading edge of RCL.

■ PACKAGE DIMENSIONS