

# MC100LVELT22

## 3.3V Dual LVTTTL/LVCMOS to Differential LVPECL Translator

The MC100LVELT22 is a dual LVTTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

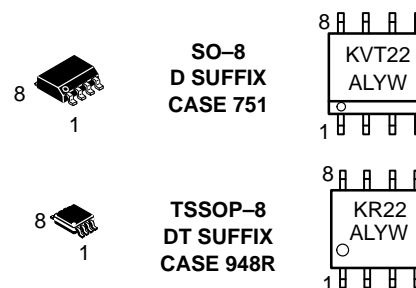
- 350 ps Typical Propagation Delay
- <100 ps Output-to-Output Skew
- ESD Protection: >4 KV HBM, >200 V MM
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range:  $V_{CC} = 3.0\text{ V to } 3.8\text{ V}$  with  $GND = 0\text{ V}$
- When Unused TTL Input is left Open, Q Output will Default High
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 164 devices



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### MARKING DIAGRAMS\*



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC100LVELT22D	SO-8	98 Units / Rail
MC100LVELT22DR2	SO-8	2500 / Reel
MC100LVELT22DT	TSSOP-8	98 Units / Rail
MC100LVELT22DTR2	TSSOP-8	2500 / Reel

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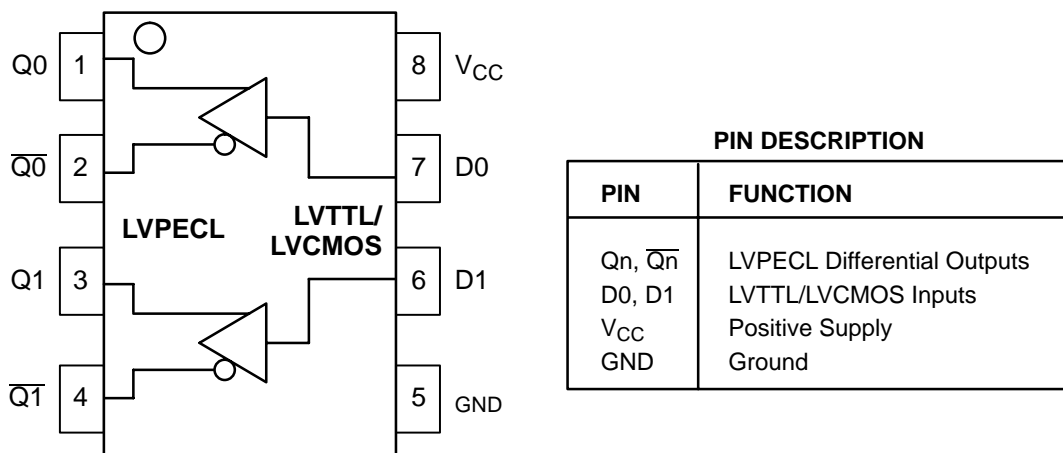


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		7	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	7	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

# MC100LVELT22

## LVPECL DC CHARACTERISTICS $V_{CC}=3.3\text{ V}$ ; $GND=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{CC}$	Power Supply Current			28			28			29	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	2275		2420	2275		2420	2275		2420	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	1490		1680	1490		1680	1490		1680	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

- Output parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.15\text{V}$ .
- Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

## LVTTTL/LVCMOS INPUT DC CHARACTERISTICS $V_{CC}=3.3\text{V}$ ; $T_A=-40^\circ\text{C}$ to $85^\circ\text{C}$ (Note 1.)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{IN}=2.7\text{V}$
$I_{IHH}$	Input HIGH Current			100	$\mu\text{A}$	$V_{IN}=V_{CC}$
$I_{IL}$	Input LOW Current			-0.2	mA	$V_{IN}=0.5\text{V}$
$V_{IK}$				-1.2	V	$I_{IN}=-18\text{mA}$
$V_{IH}$	Input HIGH Voltage	2.0			V	
$V_{IL}$	Input LOW Voltage			0.8	V	

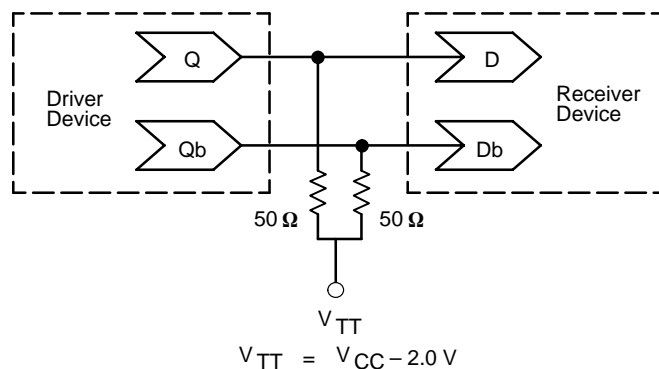
- $V_{CC}$  can vary  $\pm 0.15\text{V}$ .

## AC CHARACTERISTICS $V_{CC}=3.3\text{ V}$ ; $GND=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$	Propagation Delay (Note 2.)	200	350	600	200	350	600	200	350	600	ps
$t_{skew}$	Skew Output-to-Output Part-to-Part		30	100 400		30	100 400		30	100 400	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r/t_f$	Output Rise/Fall Time (20-80%)	200		550	200		500	200		500	ps

- $V_{CC}$  can vary  $\pm 0.15\text{ V}$ .
- Specifications for standard TTL input signal.

## MC100LVELT22



**Figure 1. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

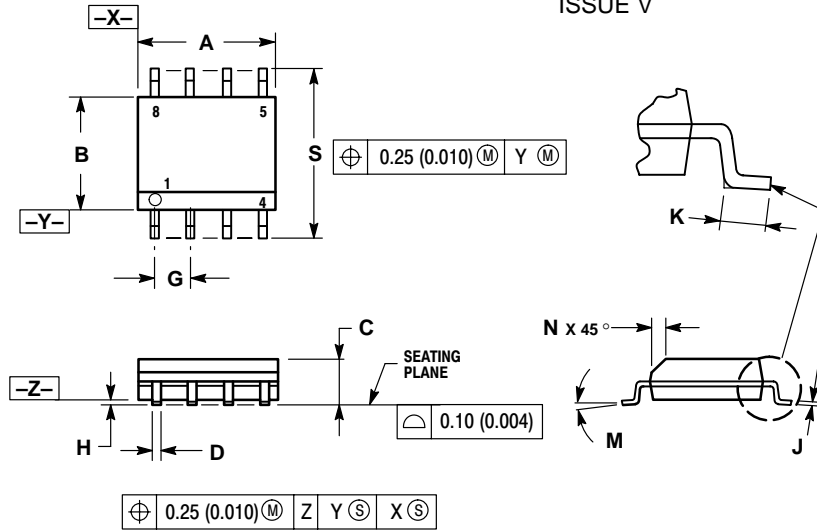
### Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC100LVELT22

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-07  
ISSUE V



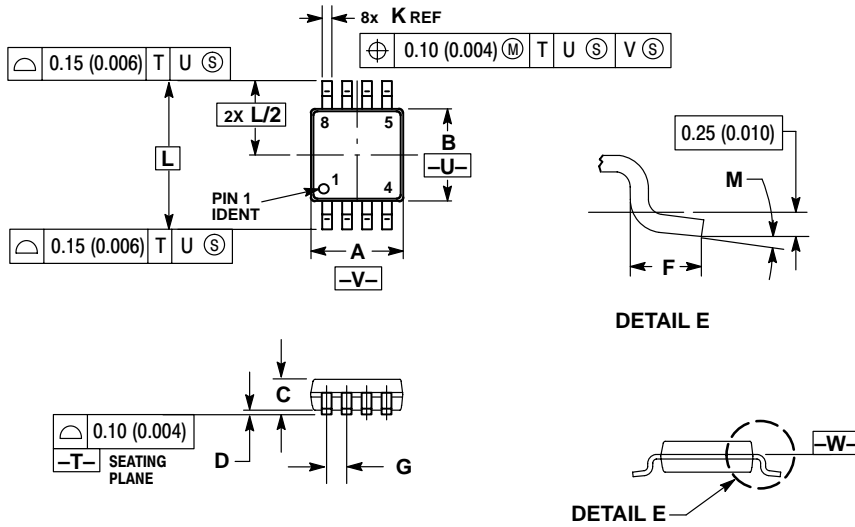
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

# MC100LVELT22

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

**Notes**

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