REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Added device type 03 to drawing. Changed t_{APW} minimum limits from 75ns and 100 ns to the quantity $t_{RP} + t_{CK}$. Removed all references to n_{BSD} from drawing. - glg	98-01-20	Raymond Monnin
B	Changes in accordance with NOR 5962-R071-98. - glg	98-03-19	Raymond Monnin
C	Changes to paragraph 1.3 and 1.4. Table IA changes to I_L, I_O, I_{CC2N}, I_{CC3P}, I_{CC3PS}, I_{CC3N}, I_{CC4}, and I_{CC5}. Removed number of cycles table from Table IA, sheet 12. - glg	99-03-16	Raymond Monnin

REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52		
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Gary L. Gross	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Jeff Bowling	
	APPROVED BY Raymond Monnin	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 512K x 16-BIT x 2-BANK, SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY (SDRAM), MONOLITHIC SILICON
	DRAWING APPROVAL DATE 97-06-17	
	REVISION LEVEL C	SIZE A / CAGE CODE **67264** / **5962-97545**
		SHEET 1 OF 52

DSCC FORM 2233
APR 97

5962-E175-99

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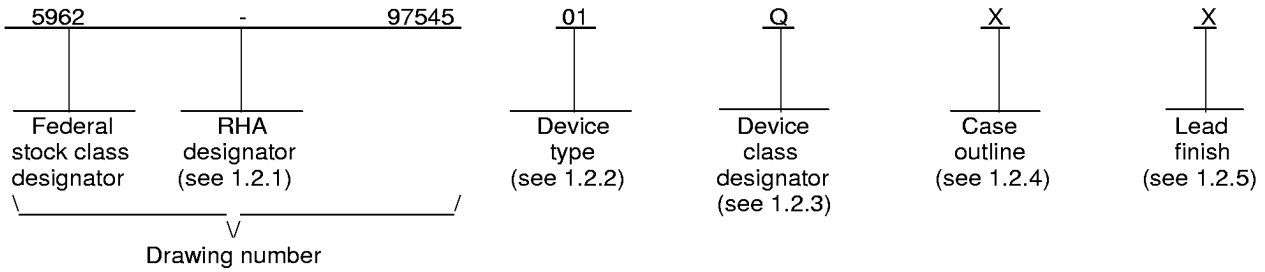
1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	626162-15	512K word x 16 bit x 2 bank, synchronous DRAM	15 ns
02	626162-20	512K word x 16 bit x 2 bank, synchronous DRAM	20 ns
03	626162-12	512K word x 16 bit x 2 bank, synchronous DRAM	12 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	50	Ceramic dual flat pack
Y	See figure 1	50	Plastic TSOP(II) package

1/ A device outside the traditional performance environment; a plastic encapsulated microcircuit (PEM).

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1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range, (V_{CC})	-0.5 V dc to +4.6 V dc
Supply voltage range for output drivers, (V_{CCQ})	-0.5 V dc to +4.6 V dc
Voltage range on any input pin	-0.5 V dc to +4.6 V dc
Voltage range on any output pin	-0.5 V dc to V_{CC} +0.5 V dc
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, (T_A)	-55°C to +125°C
Storage temperature range, (T_{stg})	-65°C to +150°C
Junction temperature, (T_J)	+175°C
Thermal resistance, junction-to-case, (Θ_{JC}):	
Case X	+5°C/W
Case Y	+1°C/W

1.4 Recommended operating conditions. 3/

Supply voltage range, (V_{CC})	+3.135 V dc to +3.465 V dc
Supply voltage for output drivers, (V_{CCQ})	+3.135 V dc to +3.465 V dc 4/
Supply voltage, (V_{SS})	0 V dc
Supply voltage for output drivers, (V_{SSQ})	0 V dc
High-level input voltage, (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc
Low-level input voltage, (V_{IL})	-0.3 V dc to +0.8 V dc
Operating free-air temperature, (T_A)	-55°C to +125°C

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values in this drawing are with respect to V_{SS}.
4/ $V_{CCQ} \leq V_{CC}$ +0.3 V.

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HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or aquiring activity upon request. For device class Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or aquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

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3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table II herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table II herein.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_A \le +125°C$ $+3.135\ V \le V_{CC} \le +3.465\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	I_{OH} = -2 mA	1,2,3	ALL	2.4		V
Low-level output voltage	V_{OL}	I_{OL} = +2 mA	1,2,3	ALL		0.4	V
Input current (leakage)	I_I	$0\ V \le V_I \le V_{CC}$ All other pins = 0 V to V_{CC}	1,2,3	ALL		±10	µA
Output current (leakage)	I_O	$0\ V \le V_O \le V_{CCQ}$ Output disabled	1,2,3	ALL		±10	µA
Average read or write current	I_{CC1}	Burst length = 1, $t_{RC} \ge t_{RC}$MIN, I_{OH}/I_{OL} = 0 mA, One bank activated 2/					mA
		Read latency = 2	1,2,3	01		75	
				02		70	
				03		85	
		Read latency = 3		01		95	
				02		85	
				03		100	
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}MAX, t_{CK} = MIN 3/	1,2,3	ALL		2	mA
	I_{CC2PS}	CKE & CLK ≤ V_{IL}MAX, $t_{CK} = \infty$ 4/	1,2,3	ALL		2	mA
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}MIN, t_{CK} = MIN 3/	1,2,3	01		35	mA
				02		30	
				03		40	
	I_{CC2NS}	CKE ≥ V_{IH}MIN, CLK ≤ V_{IL}MAX, $t_{CK} = \infty$ 4/	1,2,3	ALL		2	mA
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}MAX, t_{CK} = MIN, One bank activated 3/	1,2,3	ALL		10	mA
	I_{CC3PS}	CKE & CLK ≤ V_{IL}MAX, $t_{CK} = \infty$ One bank activated 4/	1,2,3	ALL		10	mA
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}MIN, t_{CK} = MIN One bank activated 3/	1,2,3	01		45	mA
				02		40	
				03		55	
	I_{CC3NS}	CKE ≥ V_{IH}MIN, CLK ≤ V_{IL}MAX, $t_{CK} = \infty$, One bank activated 4/	1,2,3	ALL		15	mA

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_A \le +125°C$ $+3.135\ V \le V_{CC} \le +3.465\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Burst current	I_{CC4}	Continuous burst, I_{OH}/I_{OL} = 0 mA, 5/ All banks activated, n_{CCD} = One cycle					
		Read latency = 2	1,2,3	01		130	mA
				02		110	
				03		165	
		Read latency = 3		01		175	
				02		150	
				03		210	
Auto refresh	I_{CC5}	$t_{RC} \ge t_{RC}MIN$					
		Read latency = 2	1,2,3	01		100	mA
				02		80	
				03		120	
		Read latency = 3		01		100	
				02		80	
				03		120	
Input capacitance, CLK input	$C_{i(S)}$	f = 1MHz, bias on pin under test = 0 V, all other pins are open, T_A = +25°C, See 4.4.1e 6/	4	All	Pkg X	8.0	pF
					Pkg Y	6.0	
Output capacitance, address and control inputs: A_0-A_{11}, $\overline{CS}$, DQMx, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	$C_{i(AC)}$		4	All	X	8.0	pF
					Y	6.0	
Input capacitance, CKE input	$C_{i(E)}$		4	All	X	8.0	pF
					Y	6.0	
Output capacitance	C_o		4	All	X	10.0	pF
					Y	9.0	
Functional test		See 4.4.1c	7,8A,8B	All	L	H	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_A \le +125°C$, $+3.135\ V \le V_{CC} \le +3.465\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Cycle time, CLK (system clock)	t_{CK}	See figures 4 and 5. 7/	Read latency = 2	9,10,11	01	20		ns
					02	30		
					03	15		
			Read latency = 3		01	15		
					02	20		
					03	12		
Pulse duration, CLK (system clock) high	t_{CKH}	See figures and 4 and 5. 7/		9,10,11	All	4		ns
Pulse duration, CLK (system clock) low	t_{CKL}			9,10,11	All	4		ns
Access time, CLK ↑ to data out	t_{AC}	See figures and 4 and 5. 7/ 8/						ns
			Read latency = 2	9,10,11	01		15	
					02		20	
					03		9	
			Read latency = 3		01		9	
					02		10	
					03		8	
Delay time, CLK to DQ in the low-impedance state	t_{LZ}	See figures 4 and 5. 7/ 9/		9,10,11	All	0		ns
Delay time, CLK to DQ in the high-impedance state	t_{HZ}	See figures and 4 and 5. 7/ 10/						ns
			Read latency = 2	9,10,11	01		14	
					02		15	
					03		8	
			Read latency = 3		01		11	
					02		12	
					03		8	
Setup time, data input	t_{DS}	See figures 4 and 5. 7/		9,10,11	01,02	4		ns
					03	3		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_A \le +125°C$ $+3.135\ V \le V_{CC} \le +3.465\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup time, address	t_{AS}	See figures 4 and 5. 7/	9,10,11	01,02	4		ns
				03	3		
Setup time, control input ($\overline{CS}$, DQMx, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	t_{CS}		9,10,11	01,02	4		ns
				03	3		
Setup time, CKE (suspend entry/exit, power-down entry)	t_{CES}		9,10,11	01,02	4		ns
				03	3		
Setup time, CKE (power-down/self-refresh exit)	t_{CESP}	See figures 4 and 5. 7/ 11/	9,10,11	All	10		ns
Hold time, CLK ↑ to data out	t_{OH}	See figures 4 and 5. 7/	9,10,11	01,02	2		ns
				03	1.5		
Hold time, data input	t_{DH}		9,10,11	01,02, 03	2		ns
Hold time, address	t_{AH}		9,10,11	01,02, 03	2		ns
Hold time, control input ($\overline{CS}$, DQMx, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	t_{CH}		9,10,11	01,02, 03	2		ns
Hold time, CKE	t_{CEH}		9,10,11	01,02, 03	2		ns
REFR command to ACTV, MRS, or REFR command; ACTV command to ACTV, MRS, or REFR command	t_{RC}		9,10,11	01	120		ns
				02	160		
				03	96		
ACTV command to DEAC or DCAB command	t_{RAS}		9,10,11	01	75	100K	ns
				02	100	100K	
				03	60	100K	
ACTV command to READ or WRT command	t_{RCD}	See figures 4 and 5. 7/ 12/	9,10,11	01	30		ns
				02	40		
				03	24		

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_A \le +125°C$ $+3.135\ V \le V_{CC} \le +3.465\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DEAC or DCAB command to ACTV, MRS, or REFR command	t_{RP}	See figures 4 and 5. 7/	9,10,11	01	45		ns
				02	60		
				03	36		
Final data out of READ-P operation to ACTV, MRS, or REFR command	t_{APR}		9,10,11	All device types $t_{RP} + ({}^{n}EP \times t_{CK})$			ns
Final data in to WRT-P operation to ACTV, MRS, or REFR command	t_{APW}		9,10,11	All device types $t_{RP} + t_{CK}$			ns
Final data in to DEAC or DCAB command	t_{RWL}		9,10,11	01	30		ns
				02	40		
				03	24		
ACTV command for one bank to ACTV command for the other bank	t_{RRD}		9,10,11	01	30		ns
				02	40		
				03	24		
Transition time, all inputs	t_T	See figures 4 and 5. 7/ 13/	9,10,11	All	1	5	ns
Refresh interval	t_{REF}	See figures 4 and 5. 7/	9,10,11	All		32	ms

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_A ≤ +125°C +3.135 V ≤ V_{CC} ≤ +3.465 V unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Final data out to DEAC or DCAB command	^{n}EP	7/ 14/	Read latency = 2	9,10,11	All	-1		cycles
			Read latency = 3		All	-2		
DEAC or DCAB interrupt of data-out burst to DQ in the high-impedance state	^{n}HZP	7/ 14/	Read latency = 2	9,10,11	All	2		cycles
			Read latency = 3		All	3		
READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command	^{n}CCD	7/ 14/		9,10,11	All	1		cycles
Final data in to READ or WRT command in either bank	^{n}CWL			9,10,11	All	1		cycles
WRT command to first data in	^{n}WCD			9,10,11	All	0	0	cycles
ENBL or MASK command to data in	^{n}DID			9,10,11	All	0	0	cycles
ENBL or MASK command to data out	^{n}DOD			9,10,11	All	2	2	cycles
HOLD command to suspended CLK edge; HOLD operation exit to entry of any command	^{n}CLE			9,10,11	All	1	1	cycles
MRS command to ACTV, REFR, or MRS command	^{n}RSA			9,10,11	All	2		cycles
DESL command to control input inhibit	^{n}CDD			9,10,11	All	0	0	cycles

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

1/ All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
2/ Control and address inputs change state only twice during t_{RC}.
3/ Control and address inputs change state only once every 2 x t_{CK}.
4/ Control and address inputs do not change (stable).
5/ Control and address inputs change state only once every cycle.
6/ This test is performed at initial characterization and after any design or process changes.
7/ All references are made to the rising transition of CLK unless otherwise specified.
8/ t_{AC} is referenced from the rising transition of CLK that precedes the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK that is one cycle before read latency for the READ command. An access time is measured at output reference level 1.4 V.
9/ t_{LZ} is measured from the rising transition of CLK that is one cycle before read latency for the READ command.
10/ t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11/ See figure 5, READ BURST waveform.
12/ For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.
13/ Transition time (rise and fall) should be a minimum of 1 ns and a maximum of 5 ns measured between V_{IH}MIN and V_{IL}MAX. This is ensured by design but not tested.
14/ A CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

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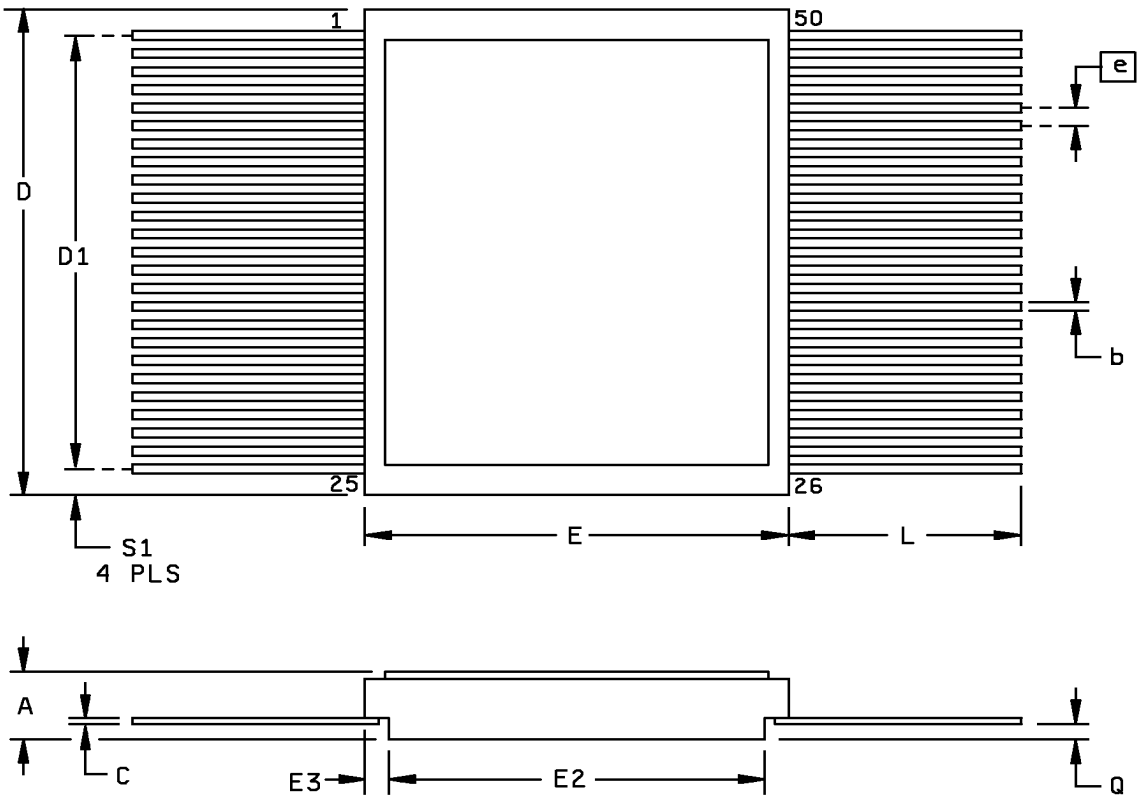
Case X



Dimension	Millimeters		Dimension	Millimeters	
	Min	Max		Min	Max
A	2.80	3.55	E2	14.10	14.90
b	.30	.50	E3	.76 min.	
C	.10	.23	e	.80 BSC	
D	20.60	21.40	L	6.35	9.40
D1	18.95	19.45	Q	.66 min.	
E	16.10	16.90	S1	.38 min.	

FIGURE 1. Case outline.

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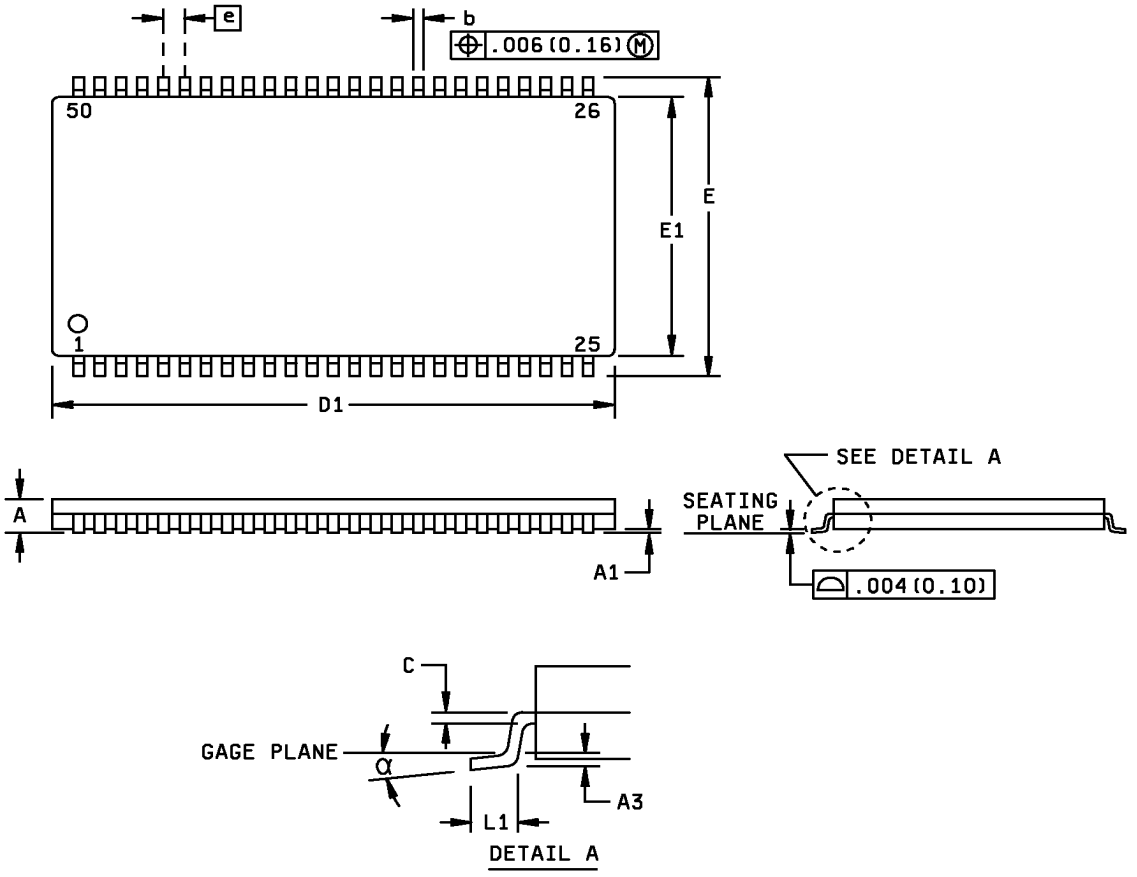
Case Y



Dimension	Millimeters		Dimension	Millimeters	
	Min	Max		Min	Max
A	---	1.20	D1	20.85	21.05
A1	.00	.00	E	11.56	11.96
A3	.25		E1	10.06	10.26
b	.30	.45	e	.80 BSC	
C	.15 nom.		L1	.40	.60
∝	0° to 5°				

FIGURE 1. Case outline - continued.

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Device types	ALL	Device types	ALL
Case outlines	X, Y	Case outlines	X, Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	26	V_{SS}
2	DQ0	27	A4
3	DQ1	28	A5
4	V_{SSQ}	29	A6
5	DQ2	30	A7
6	DQ3	31	A8
7	V_{CCQ}	32	A9
8	DQ4	33	NC
9	DQ5	34	CKE
10	V_{SSQ}	35	CLK
11	DQ6	36	DQMU
12	DQ7	37	NC
13	V_{CCQ}	38	V_{CCQ}
14	DQML	39	DQ8
15	$\overline{W}$	40	DQ9
		41	V_{SSQ}
16	$\overline{CAS}$	42	DQ10
17	$\overline{RAS}$	43	DQ11
		44	V_{CCQ}
18	$\overline{CS}$	45	DQ12
19	A11	46	DQ13
20	A10	47	V_{SSQ}
21	A0	48	DQ14
22	A1	49	DQ15
23	A2	50	V_{SS}
24	A3		
25	V_{CC}		

FIGURE 2. Terminal connections.

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Basic command truth table 1/

COMMAND	STATE OF BANKS	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9-A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9 = V A8 - A7 = 0 A6 - A0 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with auto-deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with auto-deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit/no operation	X	H	X	X	X	X	X	X	DESL
Auto refresh 2/	T = deac B = deac	L	L	L	H	X	X	X	REFR

1/ For execution of these commands on cycle n.
- CKE (n-1) must be high, or
- t_{CESP} must be satisfied for power-down exit, or
- t_{CES} and n_{CLE} must be satisfied for clock-suspend exit.

DQMx(n) is irrelevant

2/ Auto-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:
- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Irrelevant, either logic low or logic high
- V = Valid
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- BS = Logic high to select bank T; logic low to select bank B
- SB = Bank selected by A11 at cycle n

FIGURE 3a. Truth table.

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Clock-Enable (CKE) Command Truth Table 1/

COMMAND	STATE OF BANK(S)	CKE (n-1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Power-down entry on cycle (n+1) 2/	T = no access operation 3/ B = no access operation 3/	H	L	X	X	X	X	PDE
Power-down exit 4/	T = power down B = power down	L	H	X	X	X	X	---
CLK suspend on cycle (n+1)	T = access operation 3/ B = access operation 3/	H	L	X	X	X	X	HOLD
CLK suspend exit on cycle (n+1)	T = access operation 3/ B = access operation 3/	L	H	X	X	X	X	---

1/ For execution of these commands, A0-A11 (n) and DQMx (n) are don't care.

2/ On cycle n, the device executes the respective command (listed in Figure 3a). On cycle (n+1), the device enters power-down mode.

3/ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

4/ If setup time from CKE high to the next CLK high satisfies t_{CESP} , the device executes the respective command (listed in figure 3a). Otherwise, either a DESL or a NOOP command must be applied before any other command.

Legend:
- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care
- T = Bank T
- B = Bank B
- deac = Deactivated

FIGURE 3b. Truth table - continued.

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Data Mask (DQM) Command Truth Table. 1/

COMMAND	STATE OF BANK(S)	DQML DQMU 2/ (n)	DATA IN (n)	DATA OUT (n)	MNEMONIC
---	T = deac and B = deac	X	N/A	Hi-Z	---
---	T = actv and B = actv (no access operation) 3/	X	N/A	Hi-Z	---
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

1/ For execution of these commands on cycle n
- CKE (n) must be high, or
- t_{CESP} must be satisfied for power-down exit, or
- t_{CES} and n_{CLE} must be satisfied for clock suspend exit.

$\overline{CS}$n, $\overline{RAS}$n, $\overline{CAS}$n, $\overline{W}$ n, and A0-A11 are irrelevant.

2/ DQML controls D0-D7 and Q0-Q7. DQMU controls D8-D15 and Q8-Q15.

3/ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:
- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care
- V = Valid
- M = Masked input data
- N/A = Not applicable
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- write = Activated and accepting data in on cycle n.
- Read = Activated and delivering data out on cycle (n+2).

FIGURE 3b. Truth table - continued.

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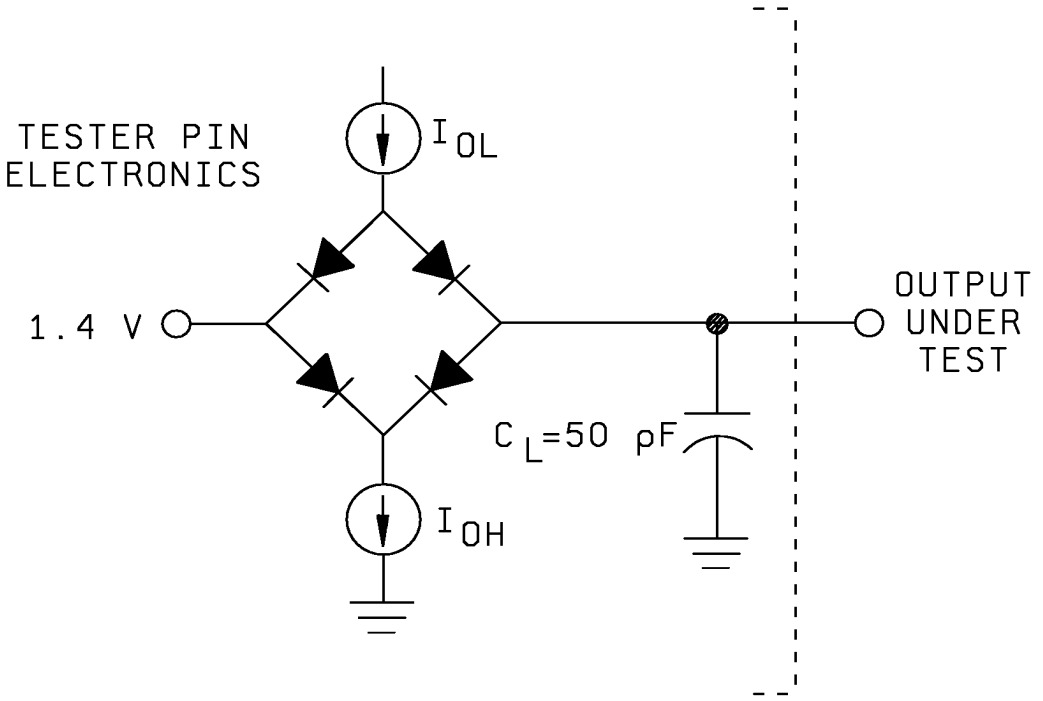

FIGURE 4. Output load circuit.

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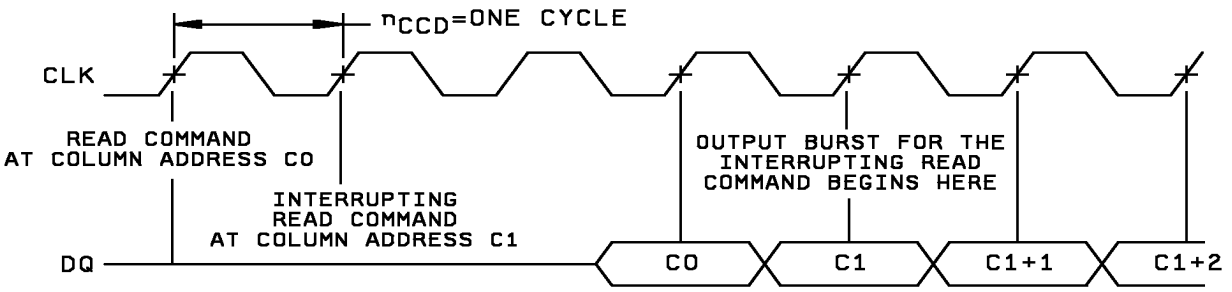
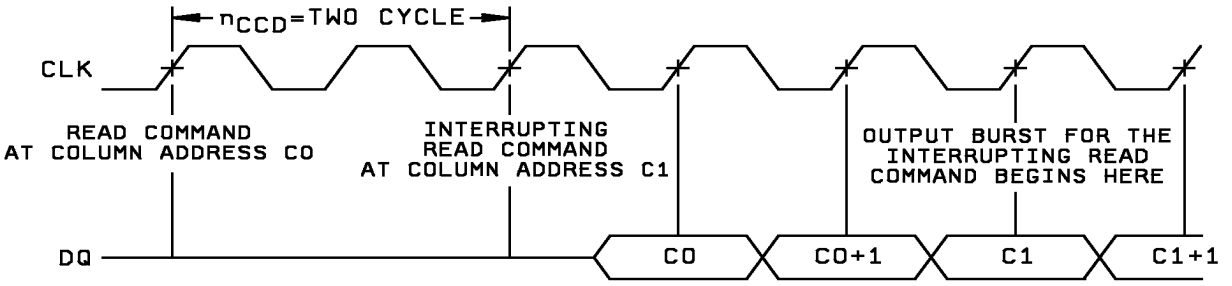
READ BURST INTERRUPTED BY READ COMMAND

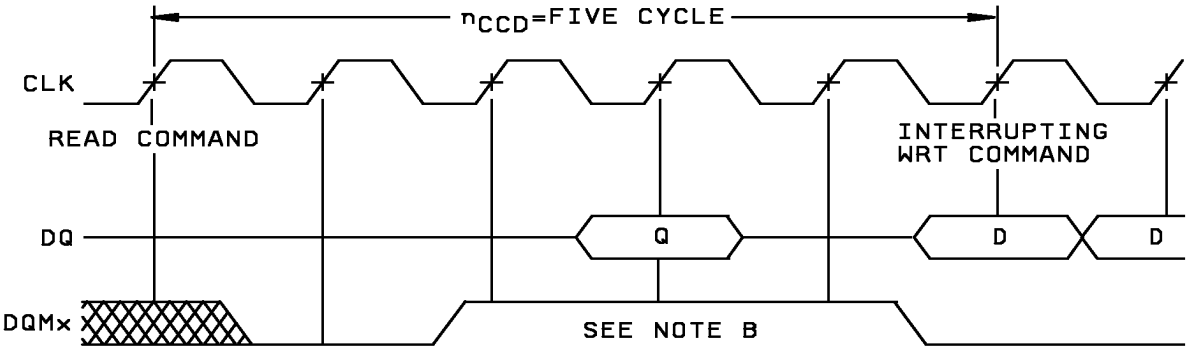


a) Interrupted on odd cycles.



b) Interrupted on even cycles.

READ BURST INTERRUPTED BY WRITE COMMAND



NOTES: 1. For the purposes of these examples, assume read latency = 3, and burst length = 4.
2. DQMx must be high to mask output of the read burst on cycles (n_{CCD} - 1), n_{CCD}, and (n_{CCD} + 1).

FIGURE 5. Timing waveforms.

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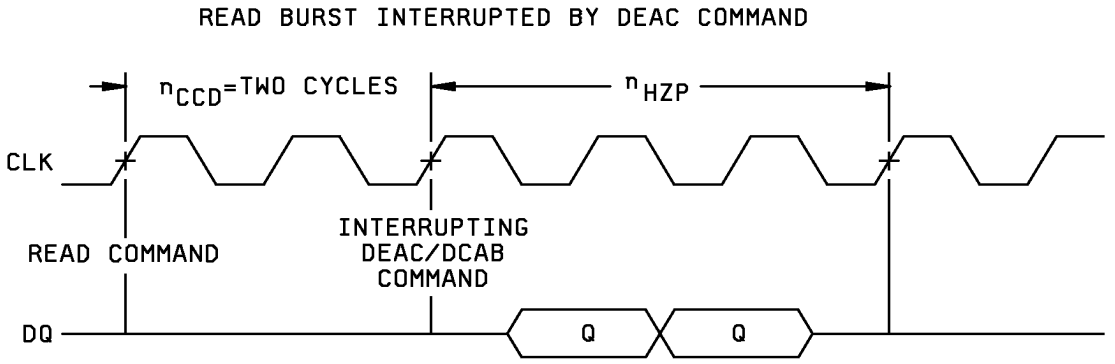

NOTE: For the purposes of these examples, assume read latency = 3, and burst length = 4.

FIGURE 5. Timing waveforms - continued.

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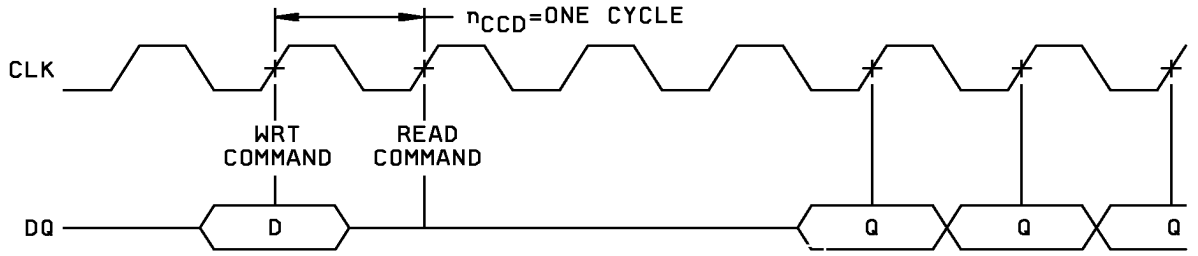
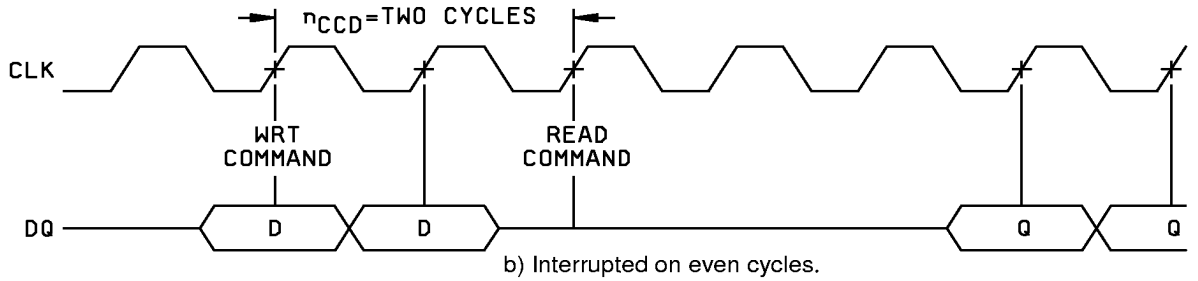
WRITE BURST INTERRUPTED BY READ COMMAND



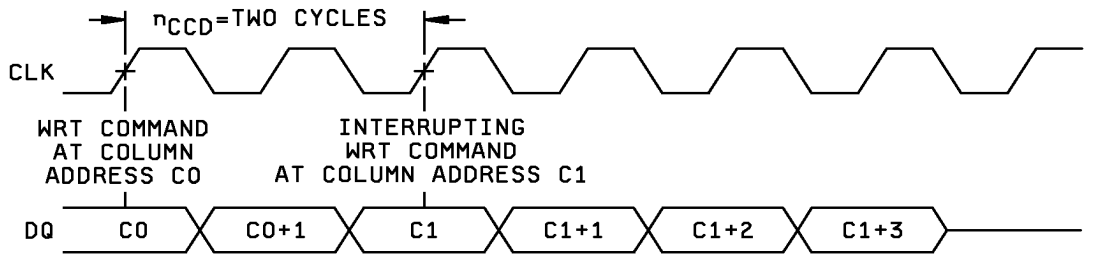
a) Interrupted on odd cycles.



b) Interrupted on even cycles.

NOTE: For these examples, assume read latency = 3, burst length = 4.

WRITE BURST INTERRUPTED BY WRITE COMMAND



NOTE: For this example, assume burst length = 4.

WRITE BURST INTERRUPTION	
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data that was input on the previous cycle is written; no further data inputs are accepted (see figure 5, WRITE BURST INTERRUPTED BY READ COMMAND).
WRT, WRT-P	The new WRT (WRT-P) command and data inputs immediately supercede the write burst in progress (see figure 5, WRITE BURST INTERRUPTED BY WRITE COMMAND).
DEAC, DCAB	The DEAC/DCAB command immedialely supercedes the write burst in progress. DQMx must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt (see figure 5, WRITE BURST INTERRUPTED BY DEAC/DCAB COMMAND).
STOP	The data on the input pins at the time of the burst-STOP command is not written; no further data is accepted. The bank remains active; however, a new read or write command cannot be entered for at least n_{BSD} cycles after the STOP command (see figure 5, WRITE BURST INTERRUPTED BY STOP COMMAND).

FIGURE 5. Timing waveforms - continued.

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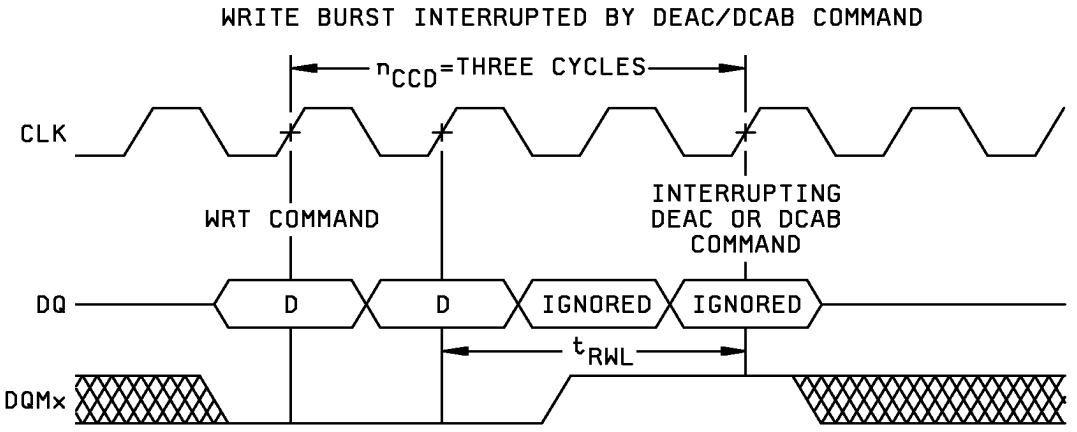

NOTE: For these examples, assume burst length = 4.

FIGURE 5. Timing waveforms - continued.

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INPUT-ATTRIBUTE PARAMETERS

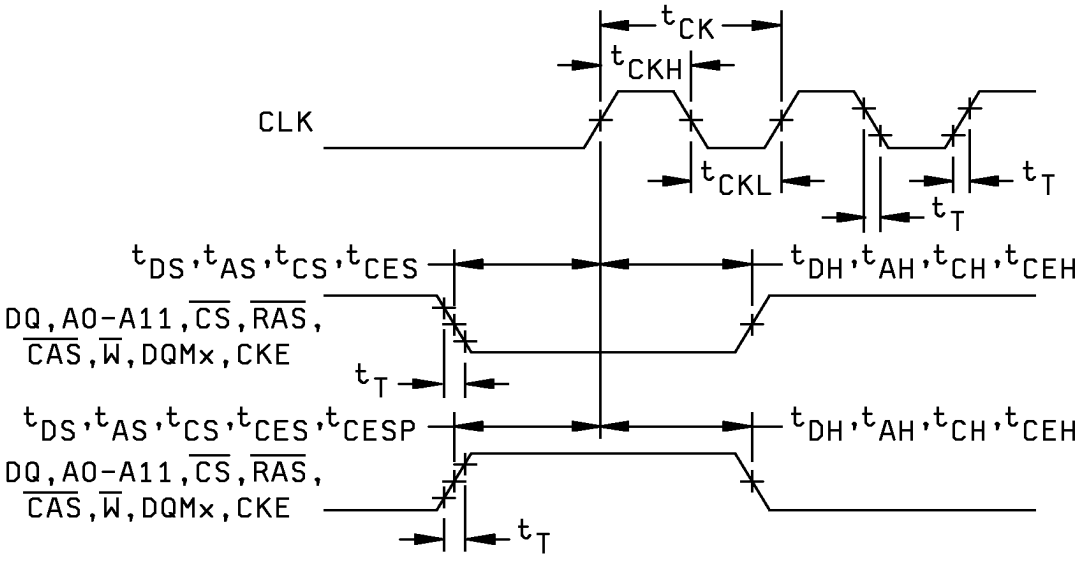

FIGURE 5. Timing waveforms - continued.

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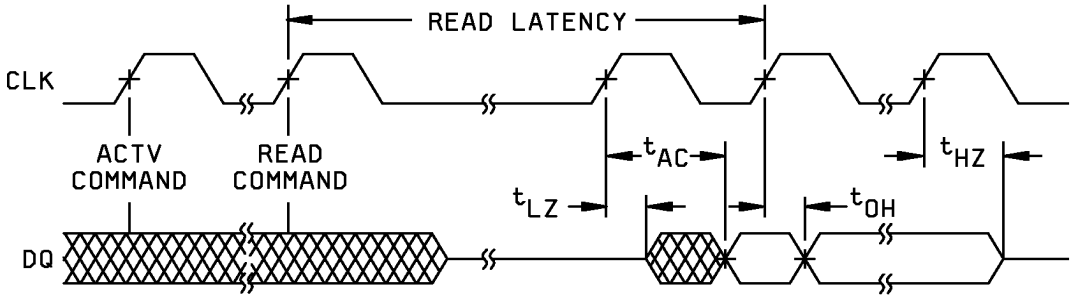
OUTPUT PARAMETERS



COMMAND TO COMMAND PARAMETERS

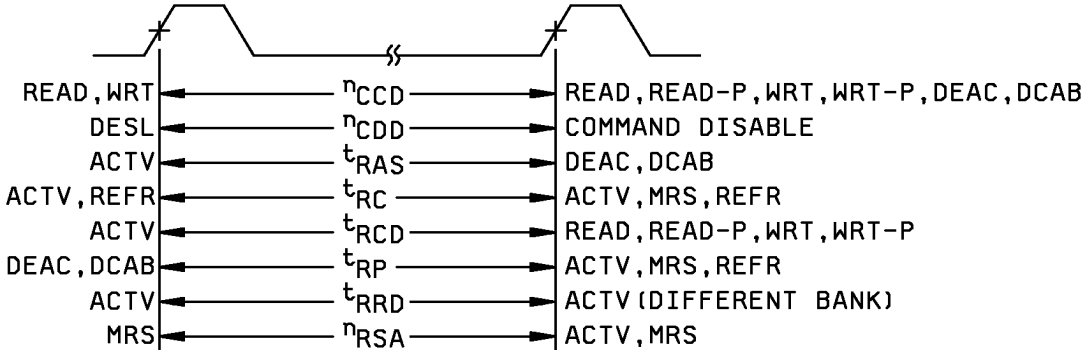


FIGURE 5. Timing waveforms - continued.

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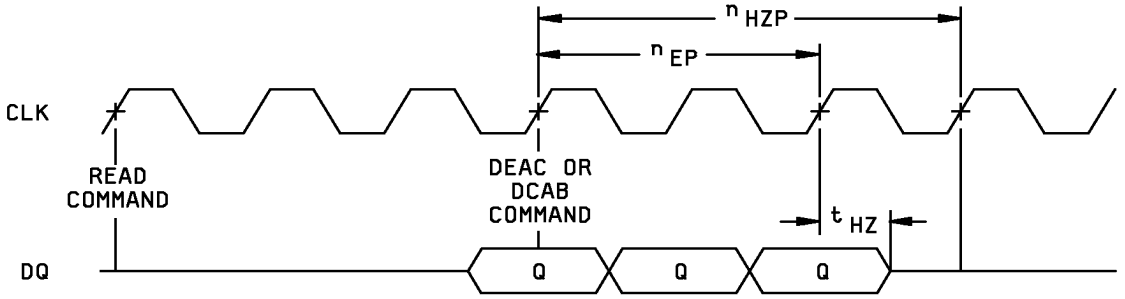
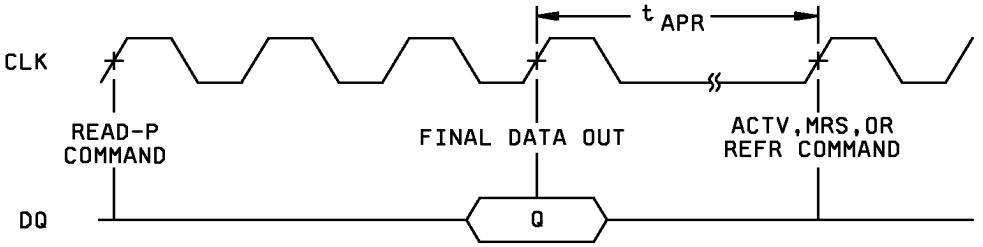
READ FOLLOWED BY DEACTIVATE



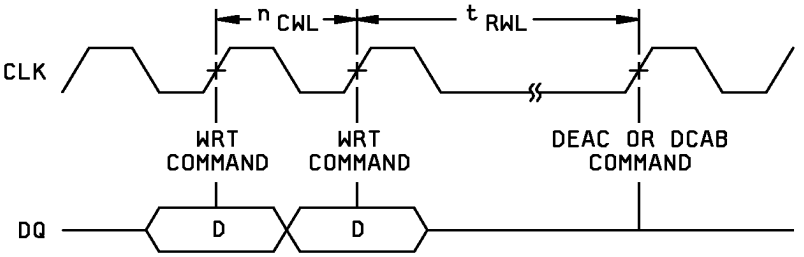
NOTE: For this example, assume read latency = 3, and burst length = 4.

READ WITH AUTO-DEACTIVATE



NOTE: For this example, assume read latency = 3, and burst length = 1.

WRITE FOLLOWED BY DEACTIVATE



NOTE: For this example, assume burst length = 1.

FIGURE 5. Timing waveforms - continued.

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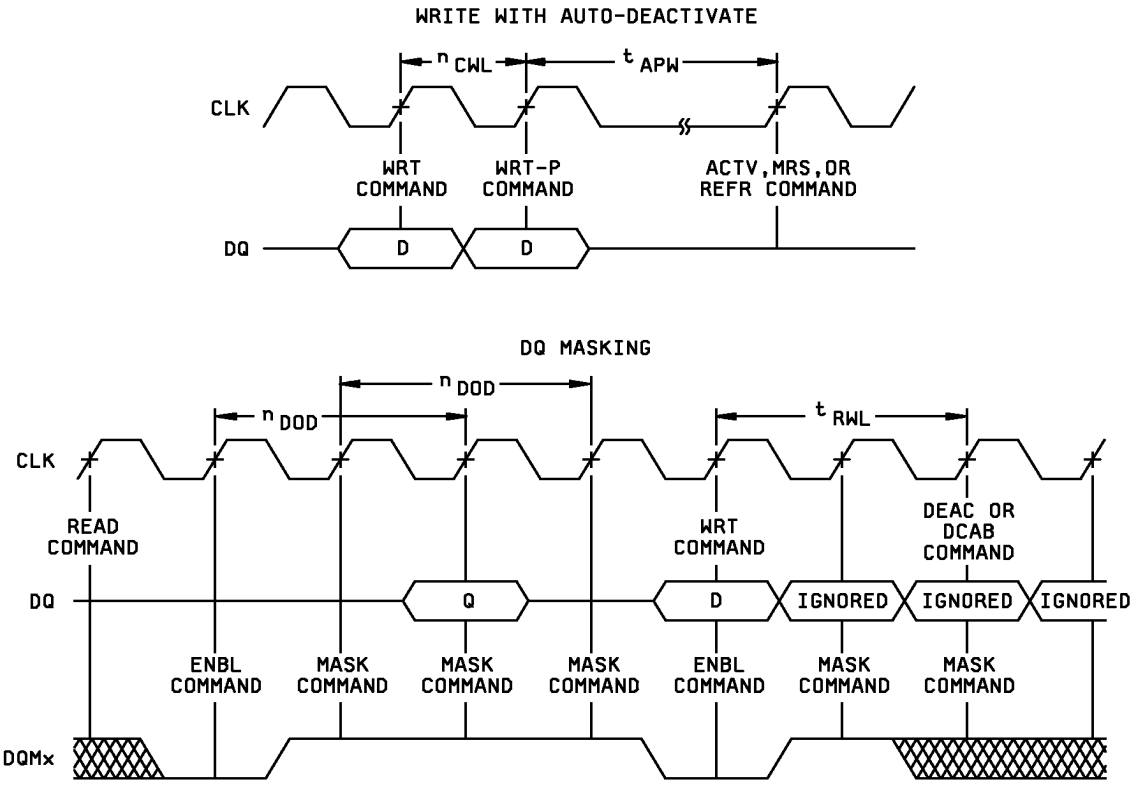

NOTE: For this example, assume read latency = 3, and burst length = 4.

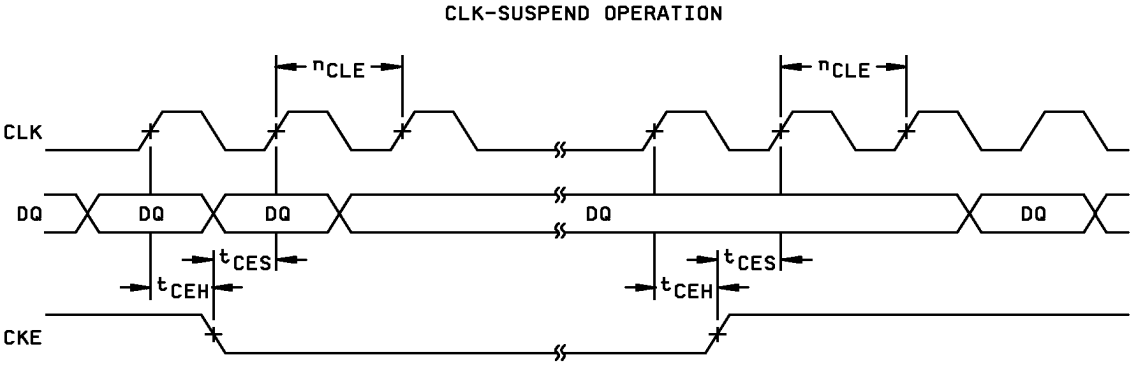

FIGURE 5. Timing waveforms - continued.

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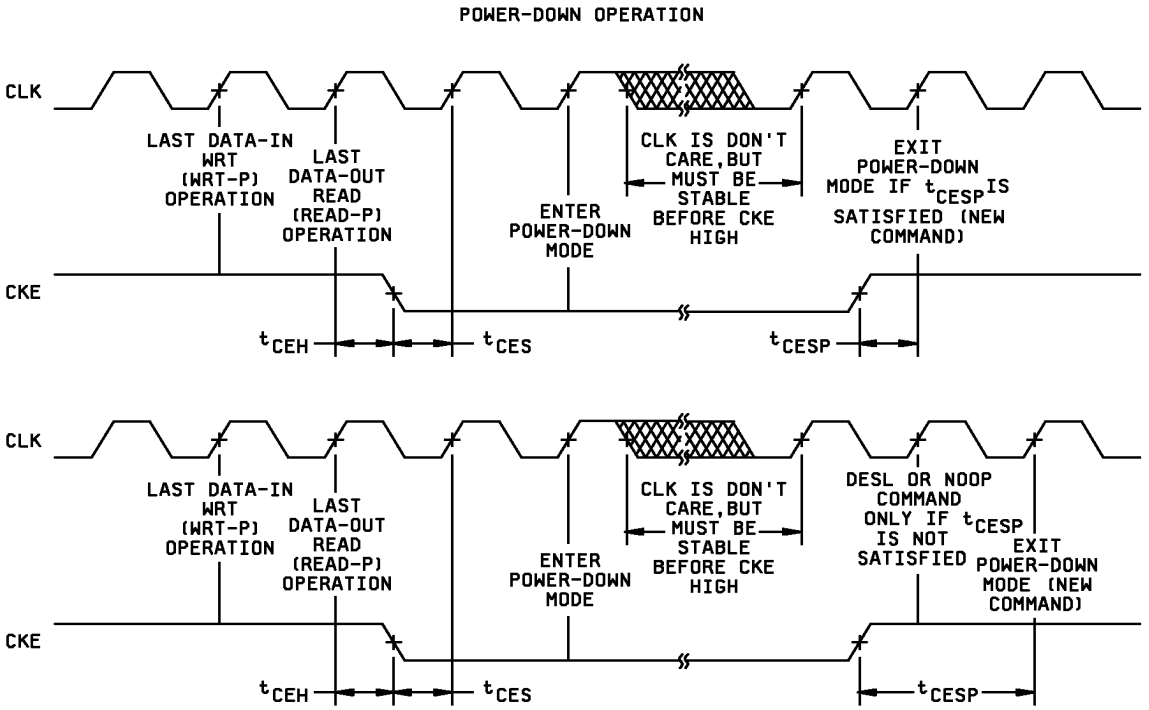

FIGURE 5. Timing waveforms - continued.

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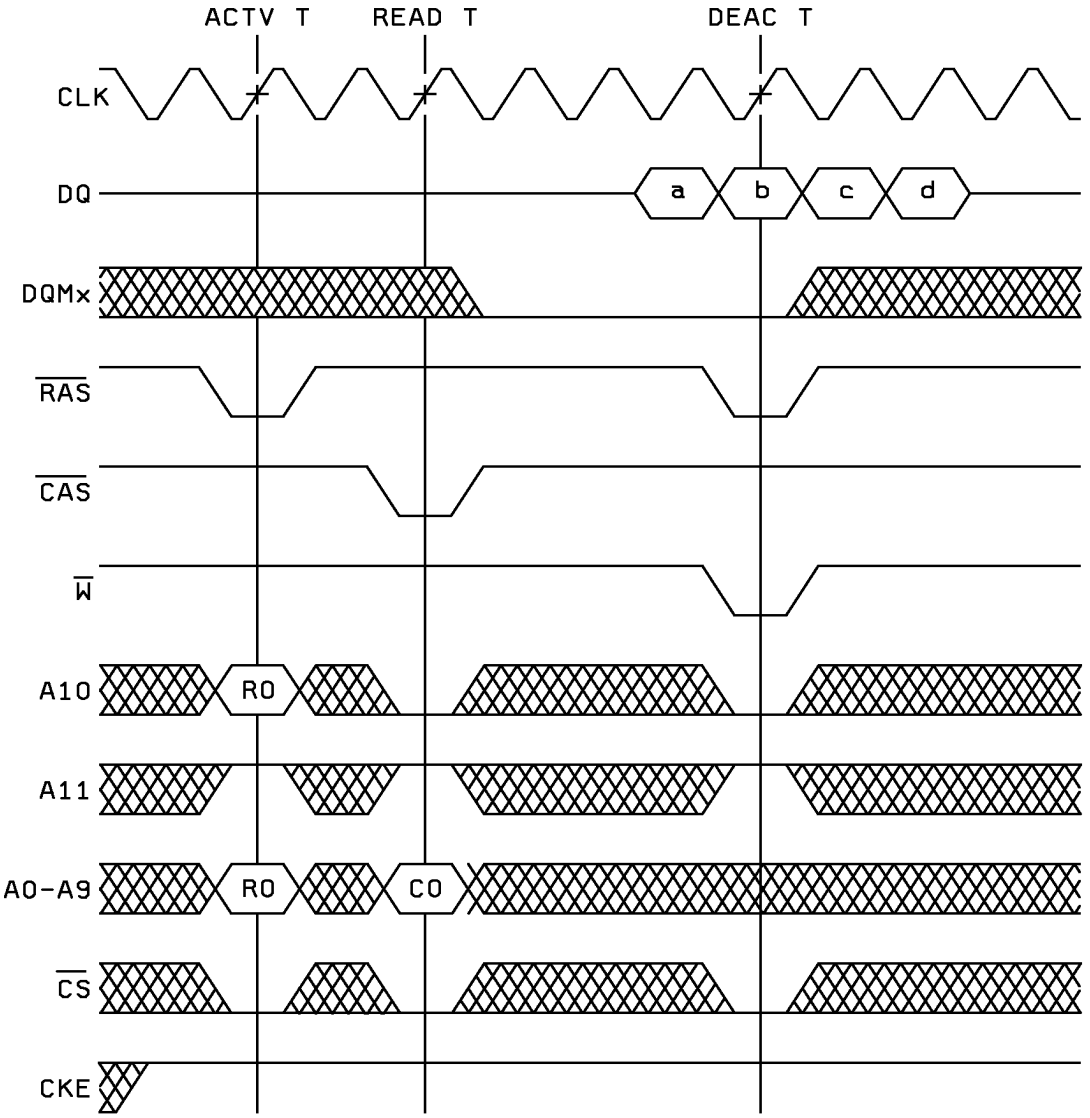
READ BURST(READ LATENCY = 3,BURST LENGTH = 4)



NOTE: This example illustrates minimum t_{RCD} and n_{EP} for device type 01 at 66 MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0.

FIGURE 5. Timing waveforms - continued.

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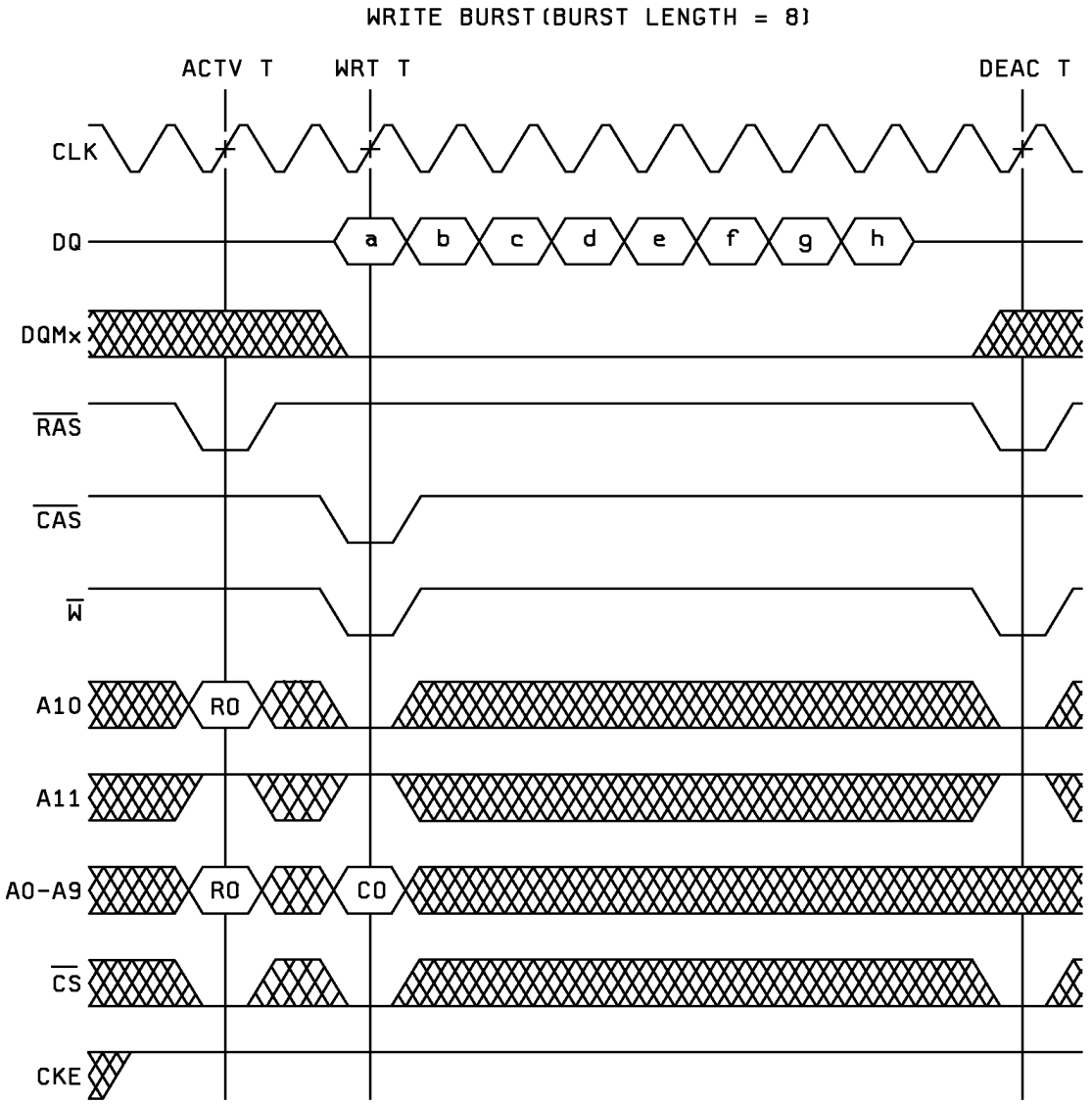

NOTE: This example illustrates minimum t_{RCD} and t_{RWL} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)							
			a	b	c	d	e	f	g	h
D	T	R0	C0	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

NOTE: Column-address sequence depends on programmed burst type and starting column address C0.

FIGURE 5. Timing waveforms - continued.

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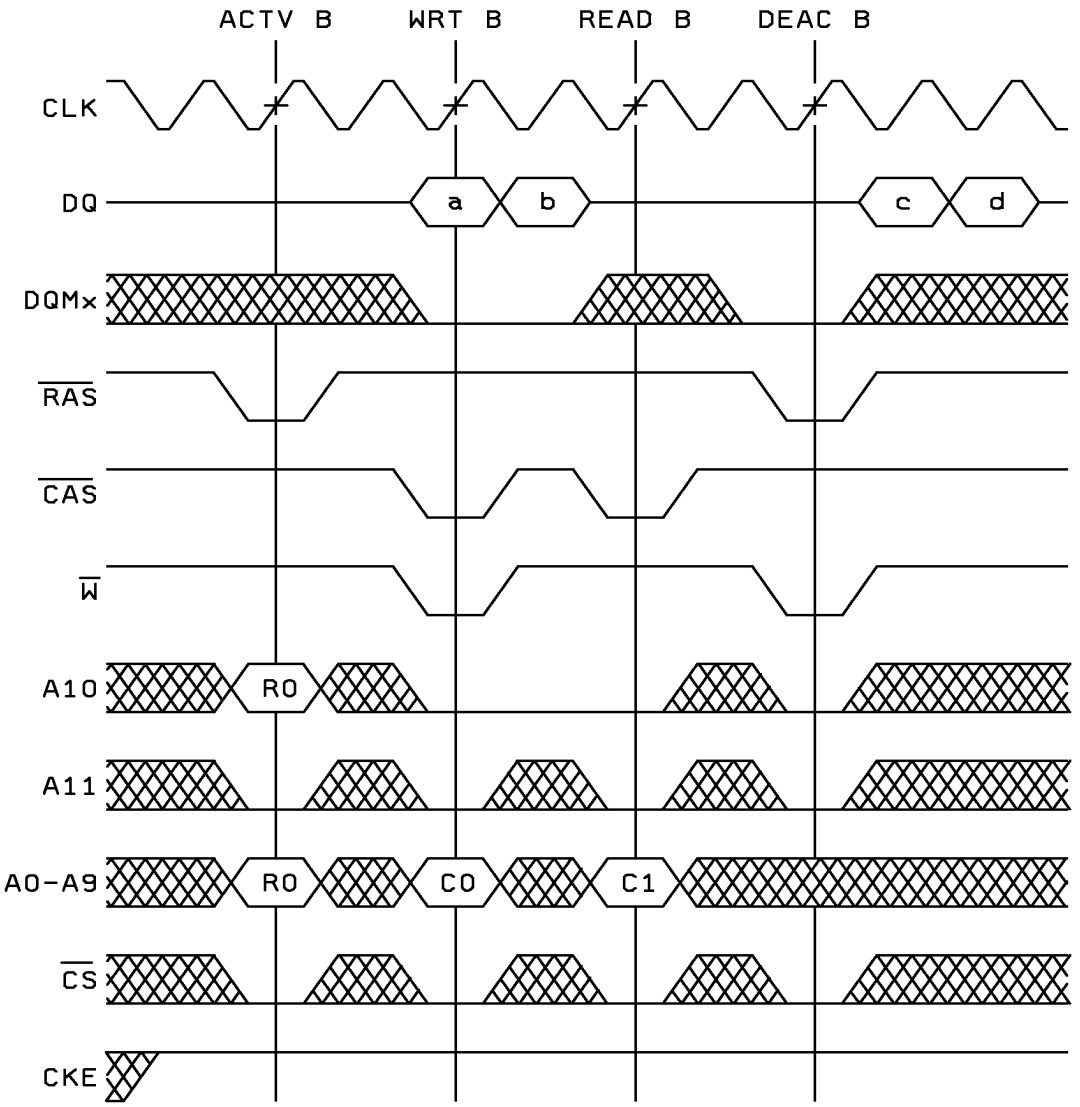
WRITE-READ BURST (READ LATENCY = 3, BURST LENGTH = 2)



NOTE: This example illustrates minimum t_{RCD} and n_{EP} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d
D	B	R0	C0	C0 + 1		
Q	B	R0			C1	C1 + 1

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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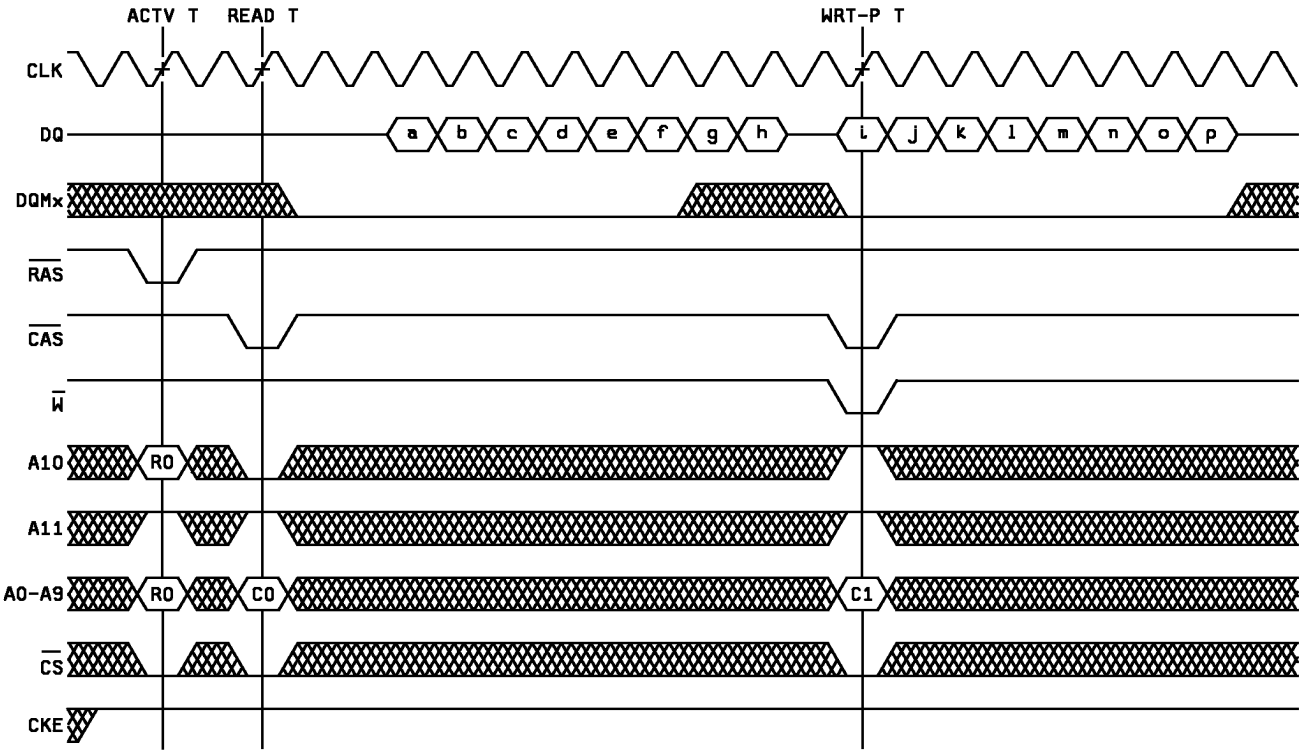
READ-WRITE BURST WITH AUTOMATIC DEACTIVATE(READ LATENCY = 3, BURST LENGTH = 8)



NOTE: This example illustrates minimum t_{RCD} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)															
			a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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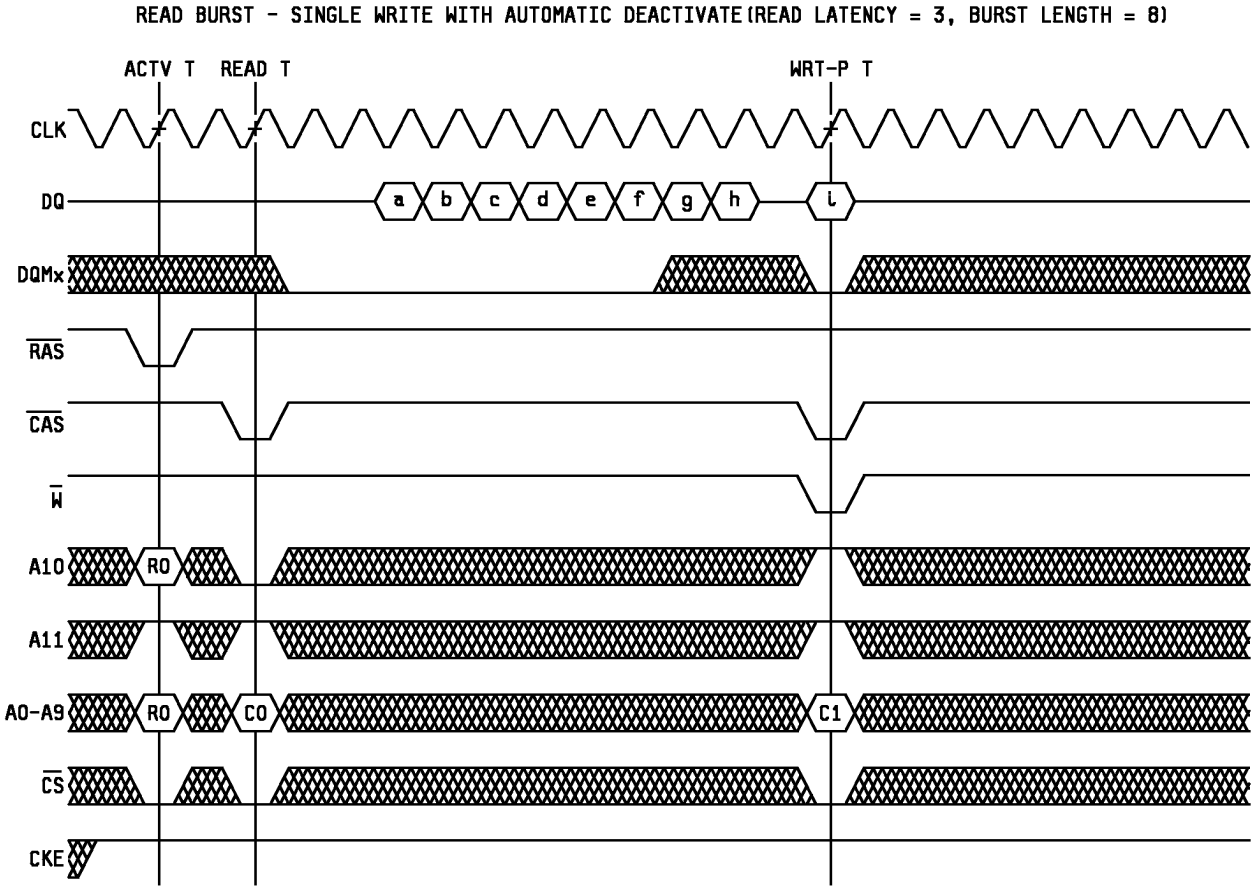

NOTE: This example illustrates minimum t_{RCD} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	g	h	i
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7	
D	T	R0									C1

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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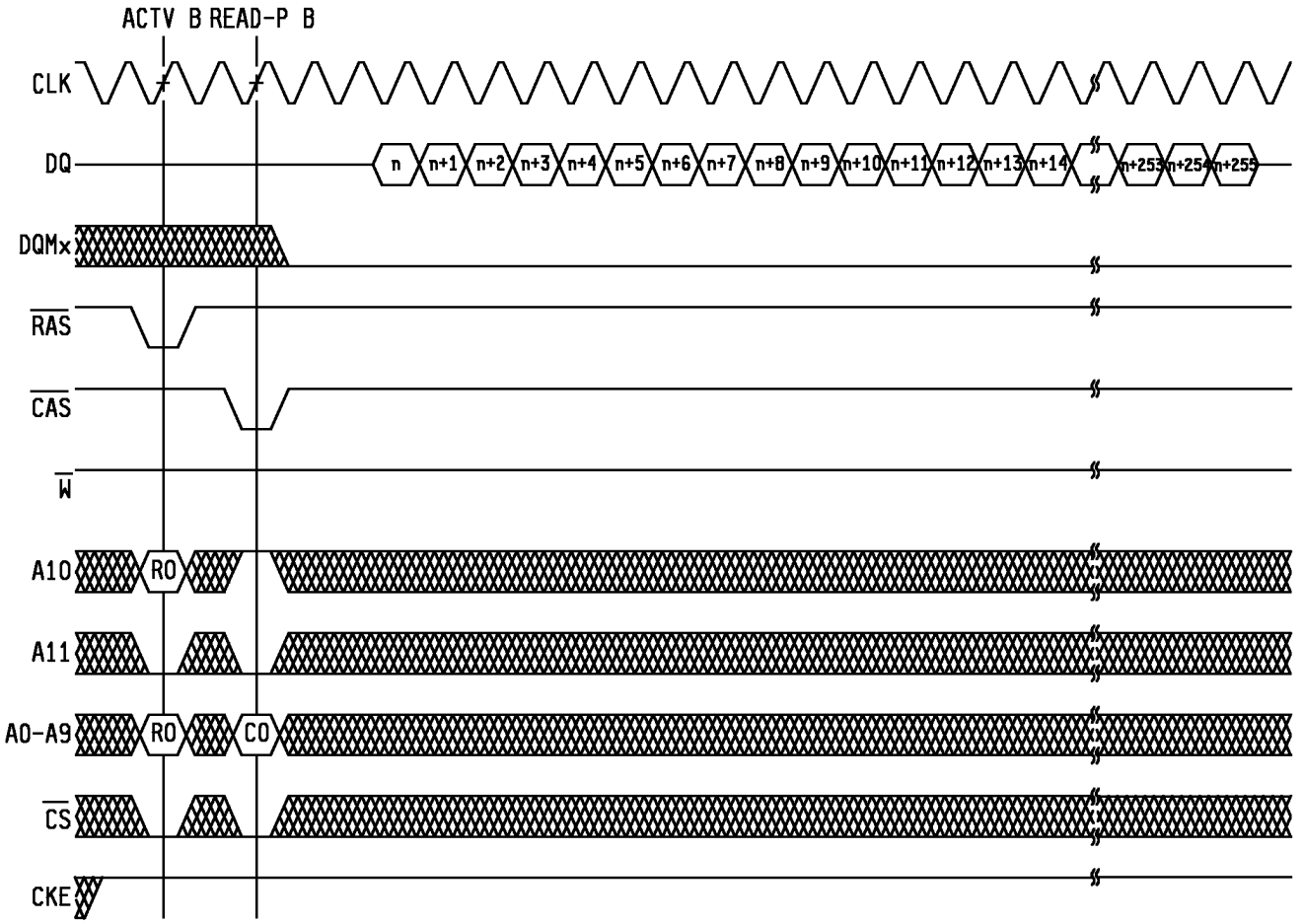
READ BURST - FULL PAGE(READ LATENCY = 3,BURST LENGTH = 256)



NOTE: This example illustrates minimum t_{RCD} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	.	.
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												255	

NOTE: Column-address sequence depends on programmed burst type and starting column address C0.

FIGURE 5. Timing waveforms - continued.

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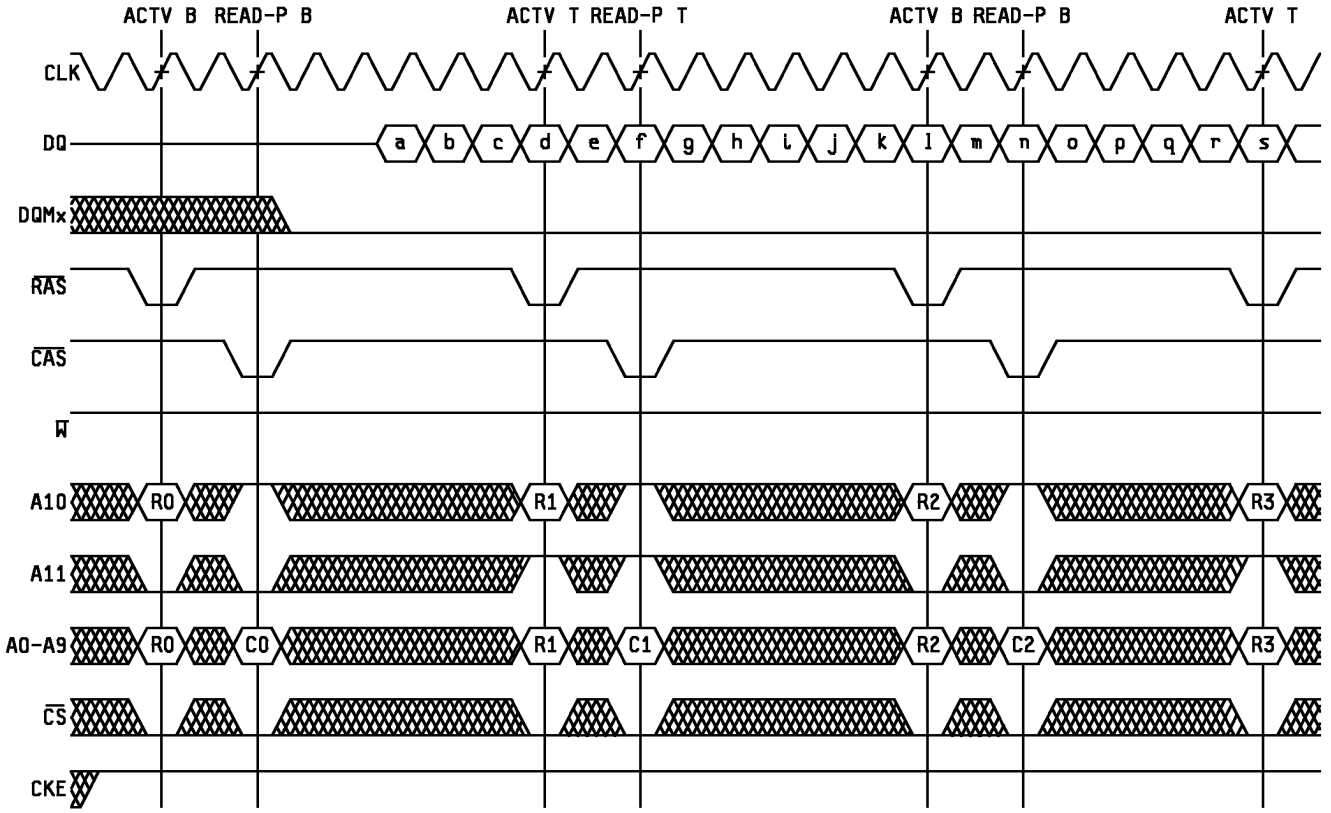
TWO-BANK ROW-INTERLEAVING READ BURSTS WITH AUTOMATIC DEACTIVATE
(READ LATENCY = 3,BURST LENGTH = 8)



NOTE: This example illustrates minimum t_{RCD} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	g	h	i	j	k
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7			
Q	T	R1									C1	C1+1	C1+2
Q	B	R2											

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (continued) l	m	n	o	p	q	r	s	.	.
Q	B	R0										
Q	T	R1	C1+3	C1+4	C1+5	C1+6	C1+7					
Q	B	R2						C2	C2+1	C2 +2	.	.

NOTE: Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2.

FIGURE 5. Timing waveforms - continued.

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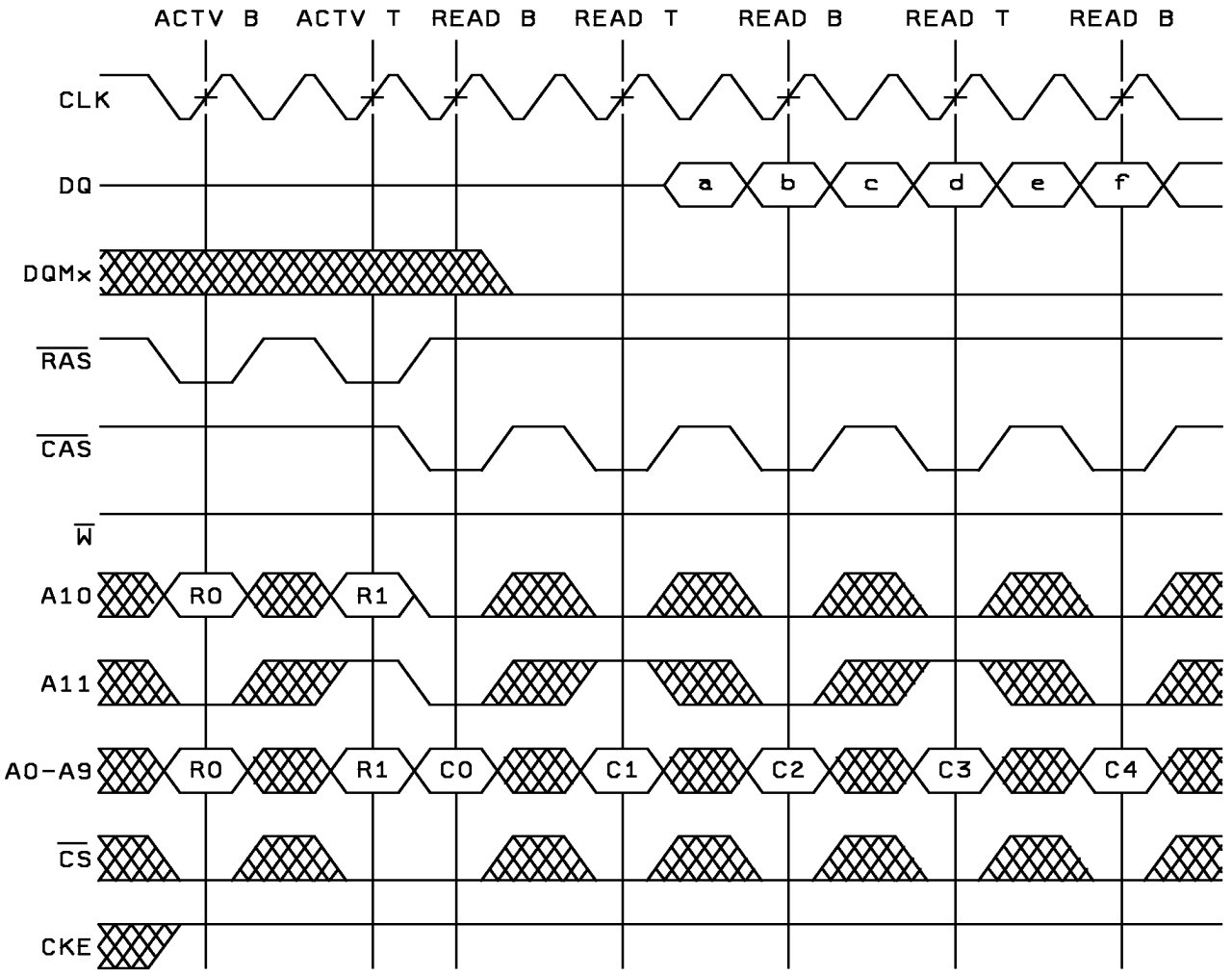
TWO-BANK COLUMN-INTERLEAVING READ BURSTS
(READ LATENCY = 3, BURST LENGTH = 2)



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	...	...
Q	B	R0	C0	C0 + 1						
Q	T	R1			C1	C1 + 1				
Q	B	R0					C2	C2 + 1		
.	...	...							...	...

NOTE: Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2.

FIGURE 5. Timing waveforms - continued.

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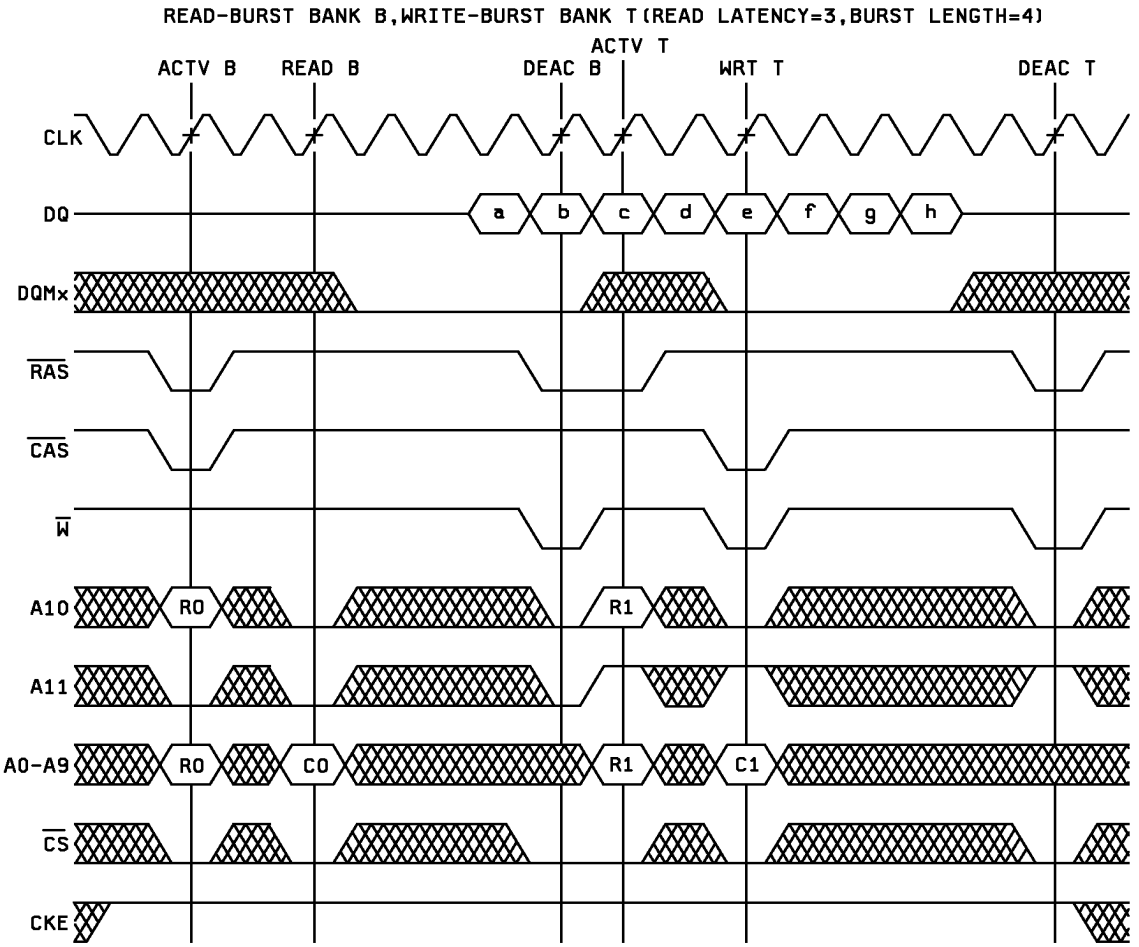

NOTE: This example illustrates minimum t_{RCD}, n_{EP}, and t_{RWL} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	g	h
Q	B	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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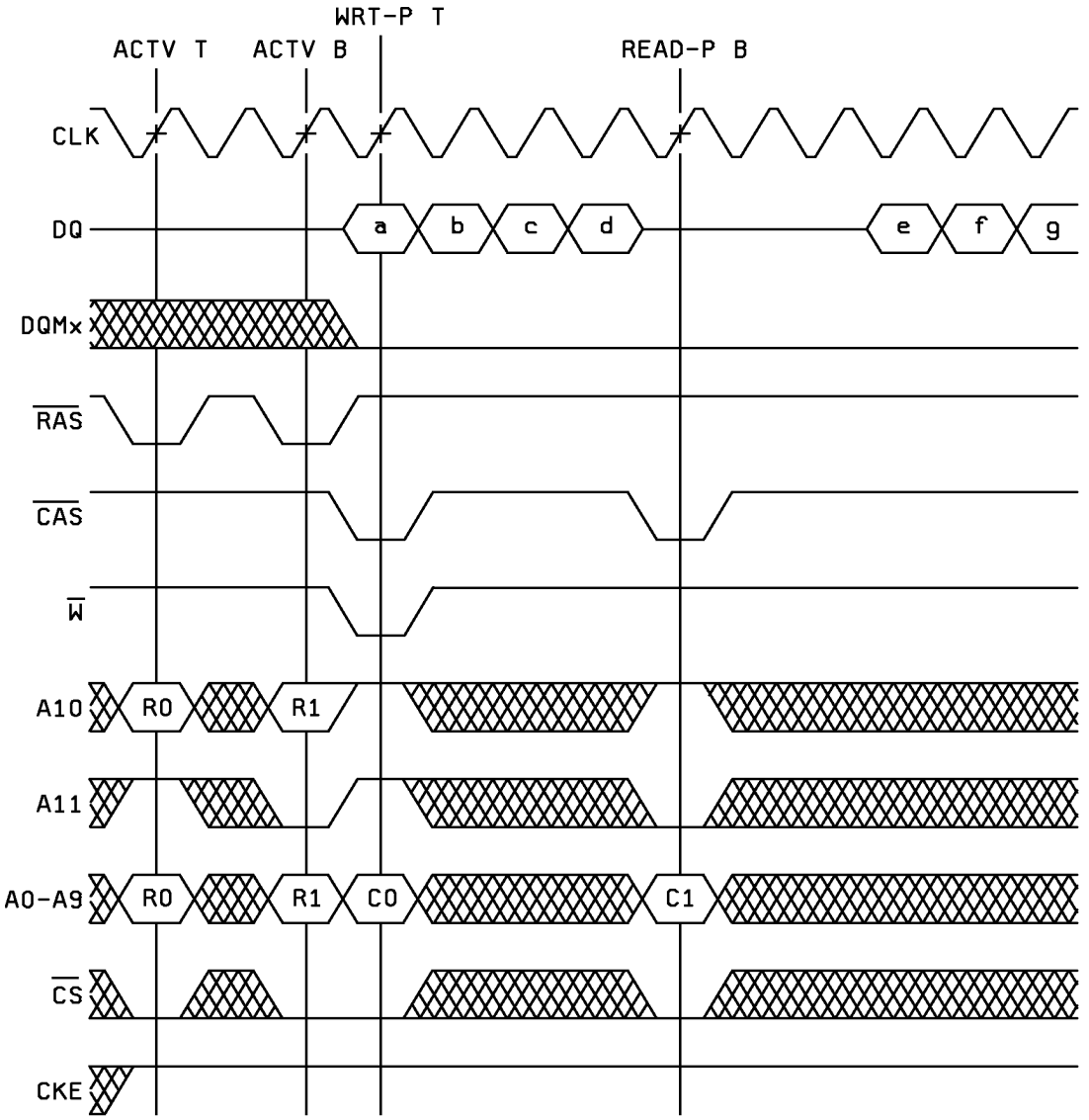
WRITE-BURST BANK T,READ-BURST BANK B WITH AUTOMATIC DEACTIVATE
(READ LATENCY = 3,BURST LENGTH = 4)



NOTE: This example illustrates minimum n_{CWL} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)							
			a	b	c	d	e	f	g	h
D	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
Q	B	R1					C1	C1 + 1	C1 + 2	C1 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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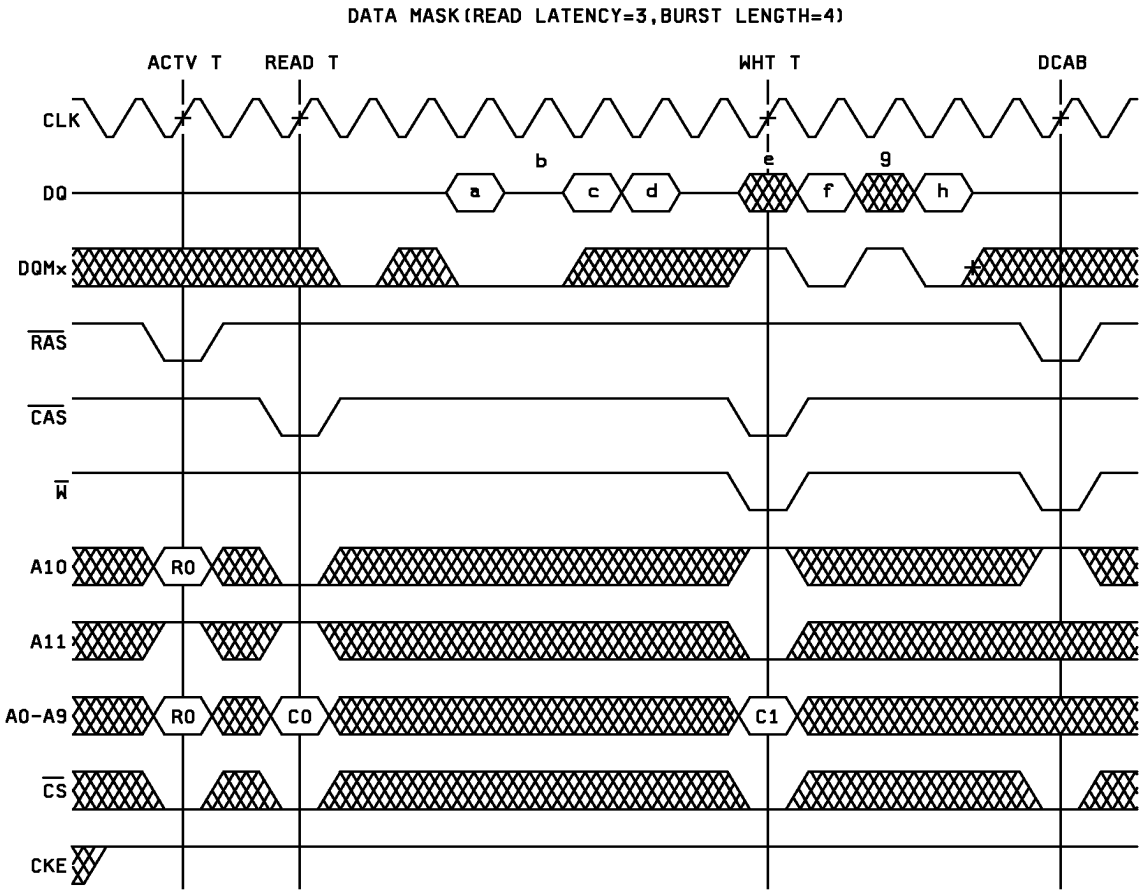

NOTE: This example illustrates minimum t_{RCD} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	g	h
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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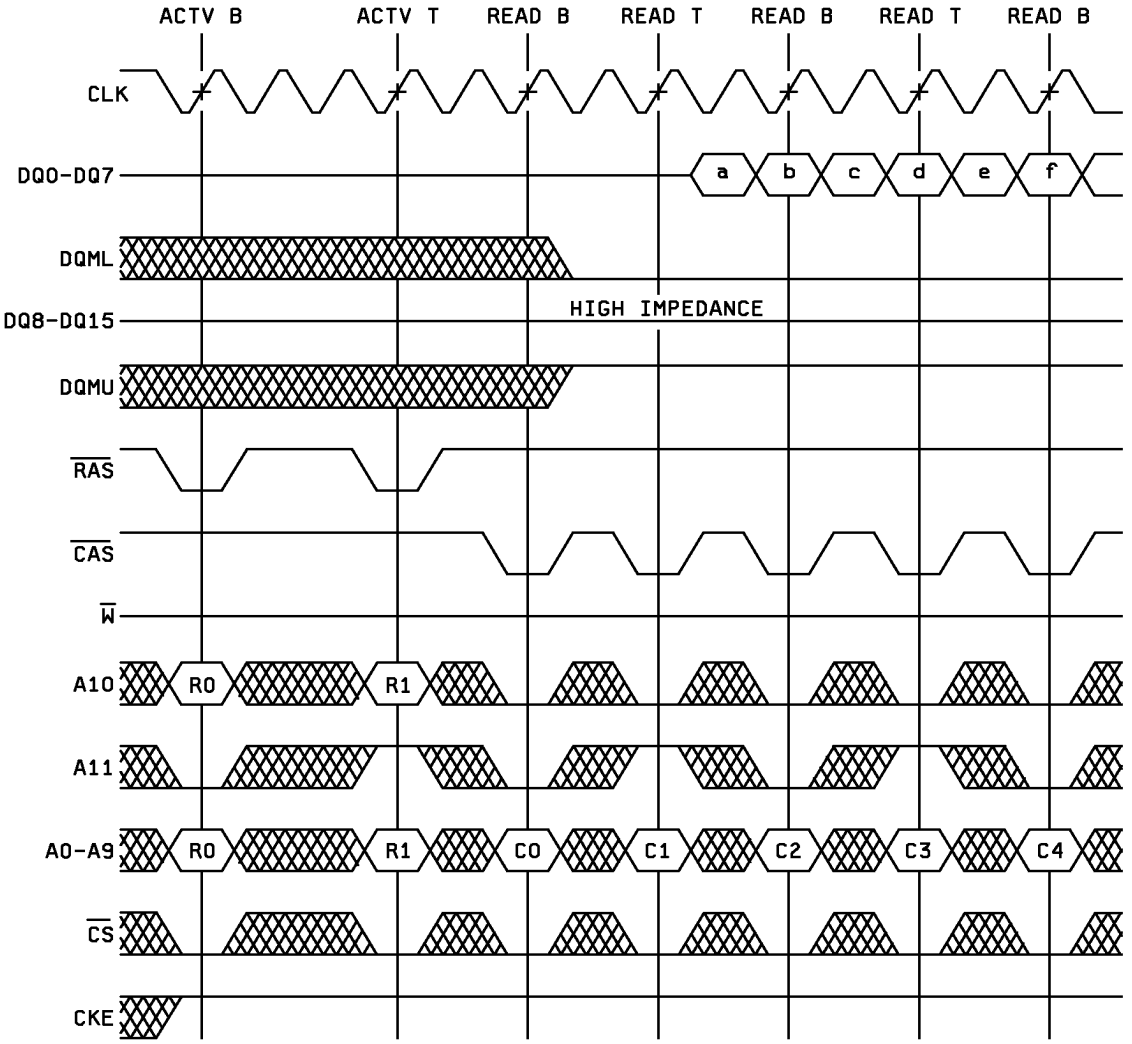
DATA MASK WITH BYTE CONTROL (READ LATENCY = 3, BURST LENGTH = 2)



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f		
Q	T	R0	C0	C0 + 1						
Q	B	R1			C1	C1 + 1				
Q	T	R0					C2	C2 + 1		
Q	B	R1							C3	C3 + 1

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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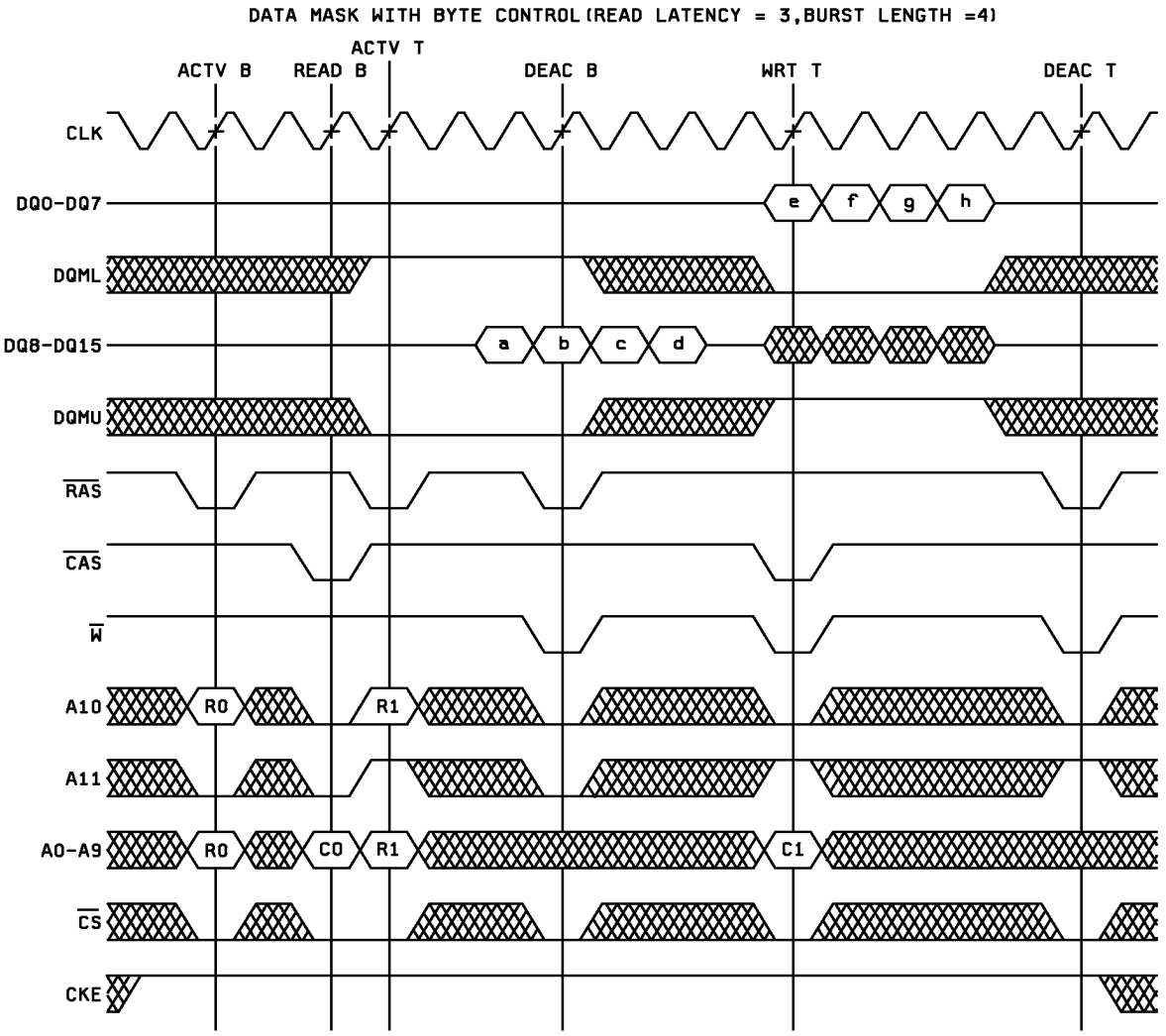

NOTE: This example illustrates minimum t_{RCD} and n_{EP} read burst, and a minimum t_{RWL} write burst for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)							
			a	b	c	d	e	f	g	h
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	B	R1					C1	C1 + 1	C1 + 2	C1 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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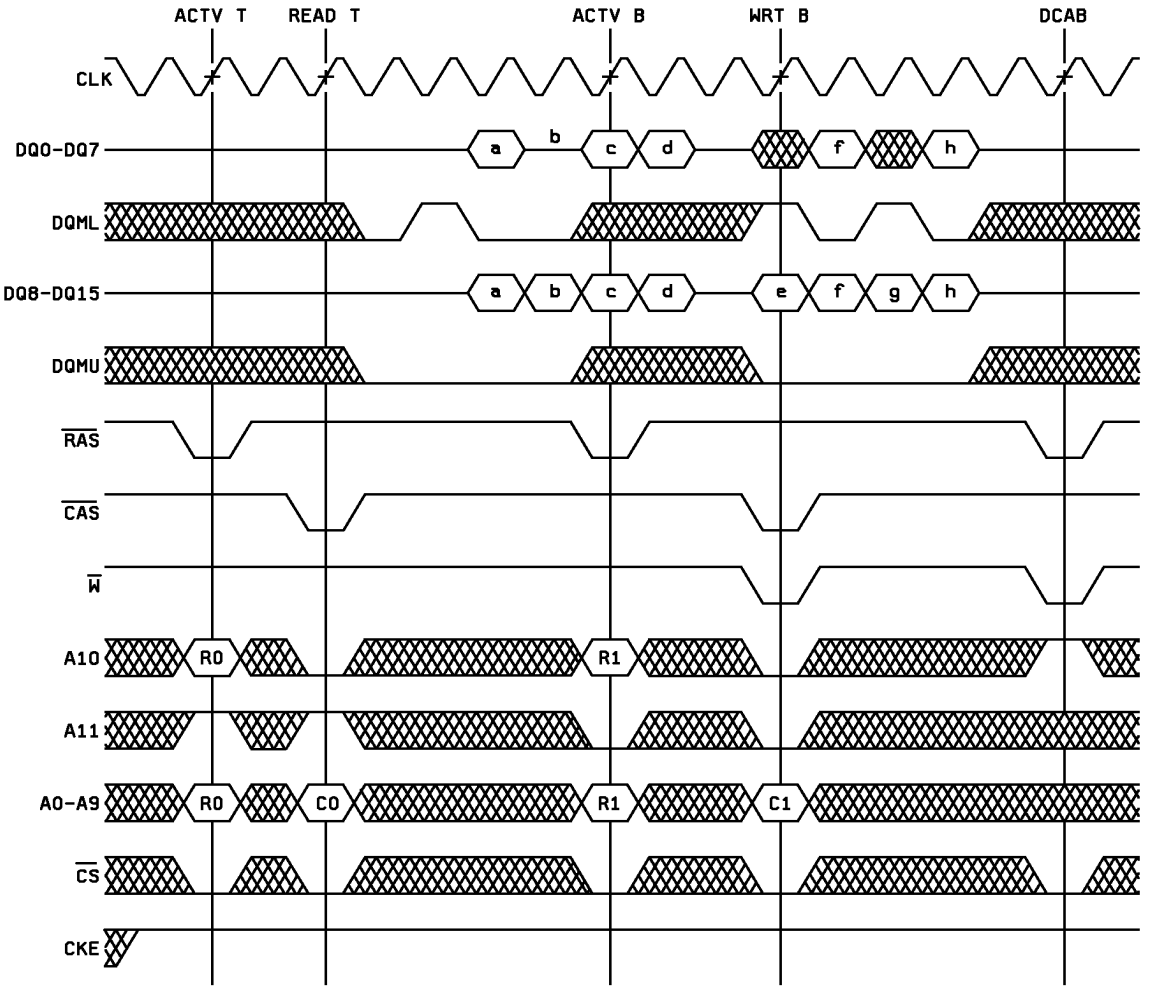
DATA MASK WITH CYCLE-BY-CYCLE BYTE CONTROL(READ LATENCY = 3,BURST LENGTH = 4)



NOTE: This example illustrates minimum t_{RCD} and t_{RWL} for device type 01 at 66MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)							
			a	b	c	d	e	f	g	h
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	B	R1					C1	C1 + 1	C1 + 2	C1 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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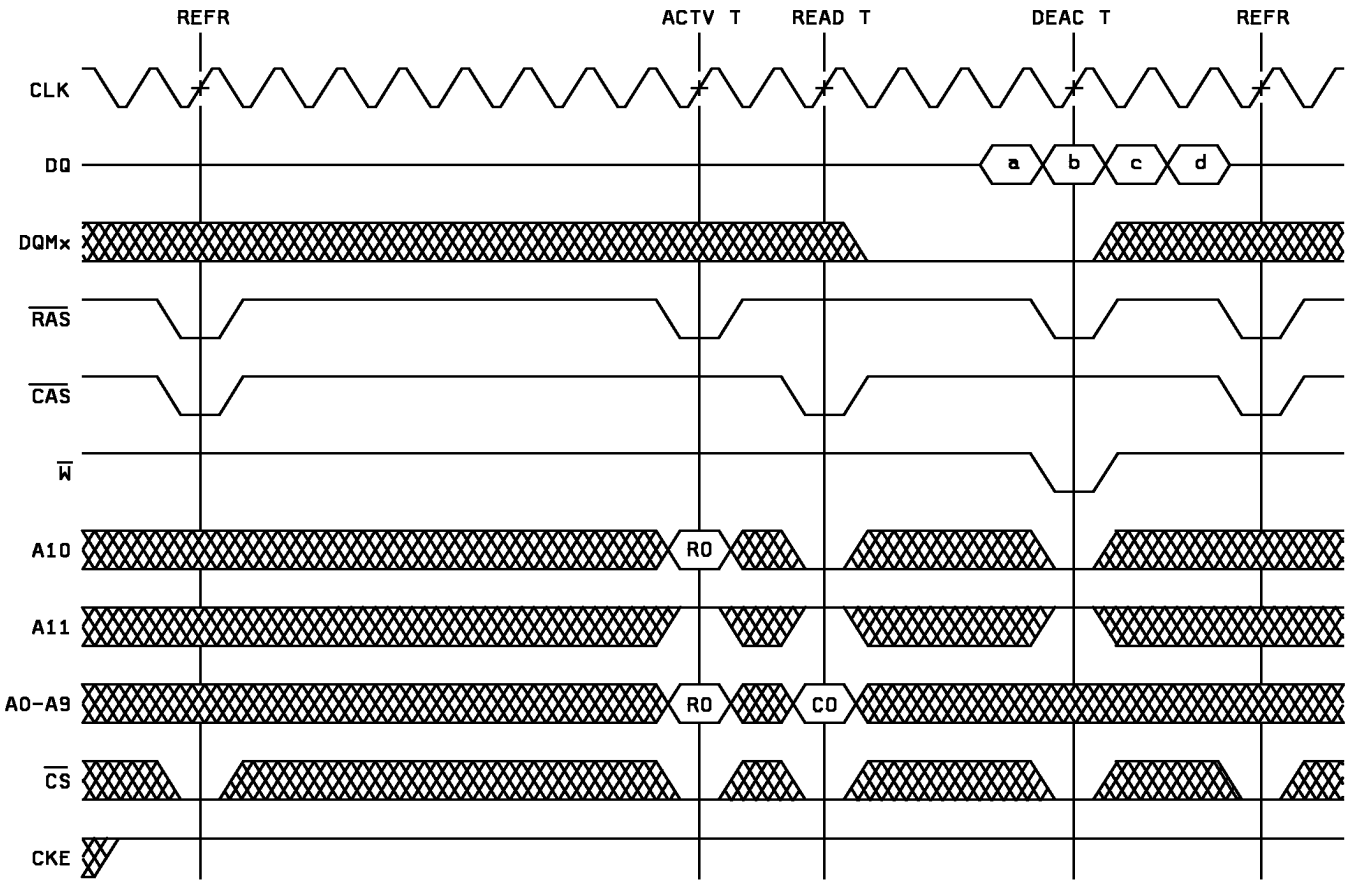
REFRESH CYCLES (READ LATENCY=3,BURST LENGTH=4)



NOTE: This example illustrates minimum t_{RC}, t_{RCD}, and n_{EP} for device type 01 at 66 MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)			
			a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0.

FIGURE 5. Timing waveforms - continued.

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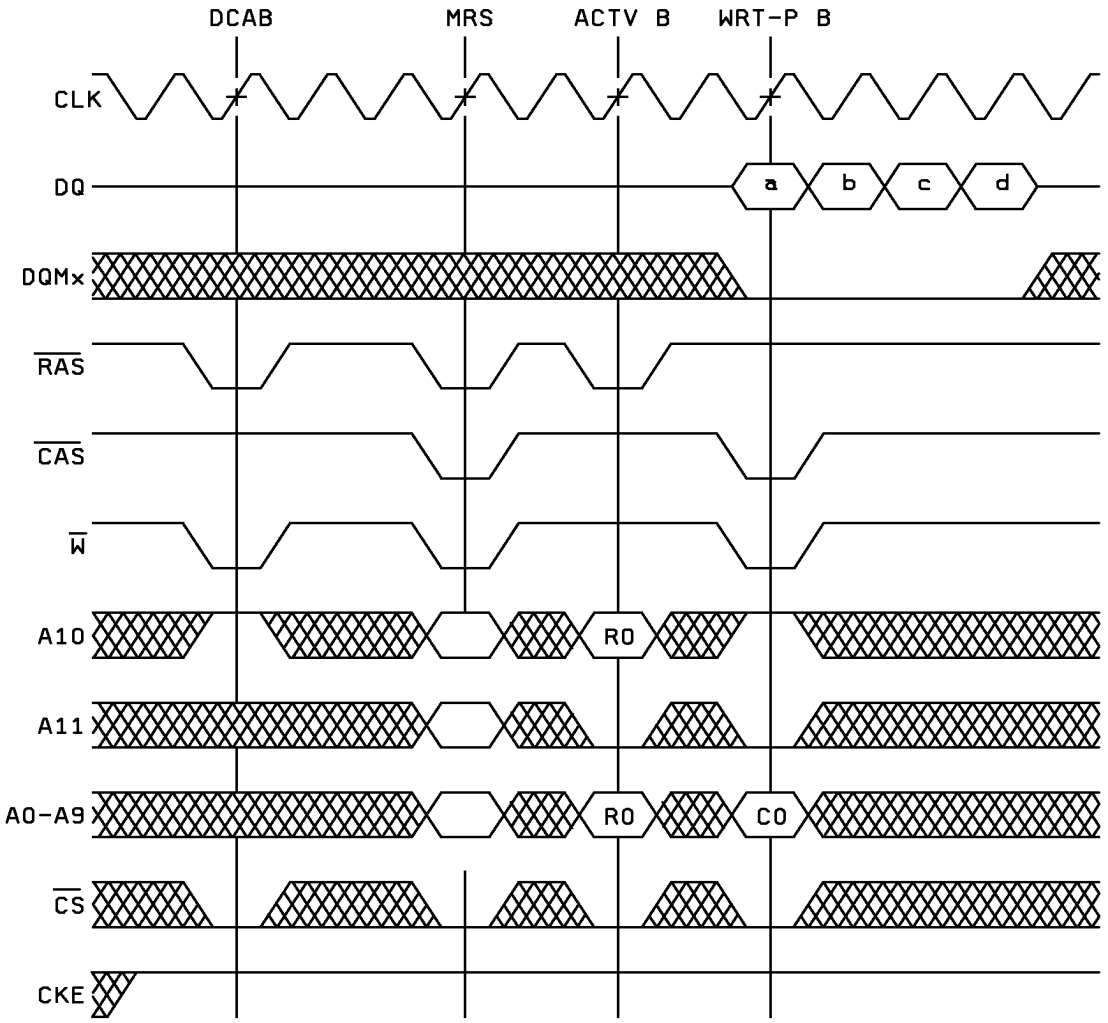
SET MODE REGISTER(DEACTIVATE ALL, SET MODE REGISTER,
WRITE BURST WITH AUTOMATIC DEACTIVATE)
(READ LATENCY = 3, BURST LENGTH = 4)



NOTE: This example illustrates minimum t_{RP}, n_{RSA}, and t_{RCD} for device type 01 at 66 MHz.

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note)			
			a	b	c	d
D	B	R0	C0	C0 + 1	C0 + 2	C0 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0.

FIGURE 5. Timing waveforms - continued.

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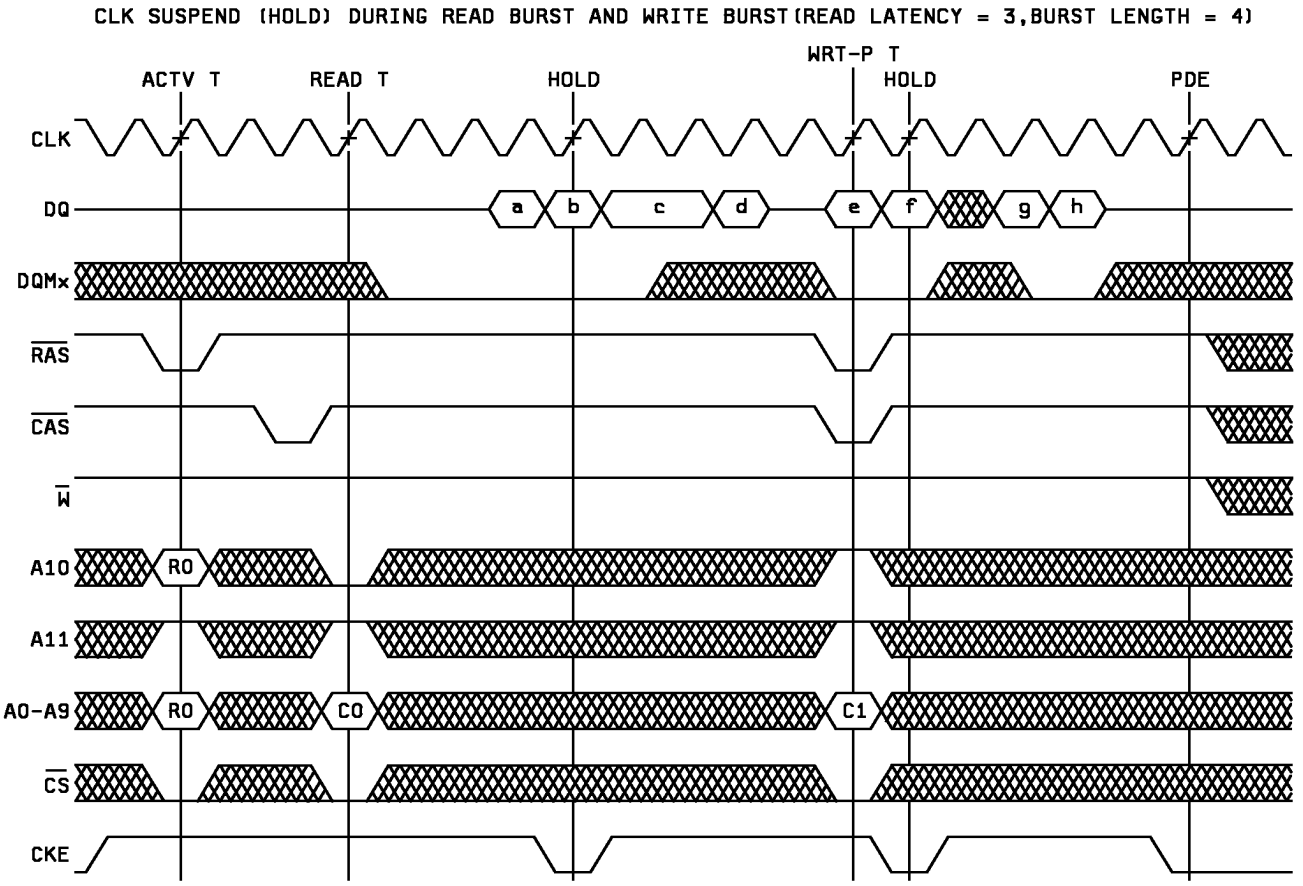

BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE (see note) a	b	c	d	e	f	g	h
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

NOTE: Column-address sequence depends on programmed burst type and starting column address C0 and C1.

FIGURE 5. Timing waveforms - continued.

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4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device class M, procedures and circuits shall be manitained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes N, Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 Mhz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

Line Number	Test requirements	Subgroups (inaccordance with MIL-STD-883, method 5005,table1)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class Q	Device class N	Device class V
1	Interim electrical parameters (see 4.2)	- - -	- - -	- - -	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Not required	Required
3	Same as line 1	- - -	- - -	- - -	1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required
5	Same as line 1	- - -	- - -	- - -	1*, 7* Δ
6	Final electrical parameters	1*, 2,3,7*,8, 9,10, 11	1*,2,3,7*,8, 9,10,11	2, 3, 8, 10, 11	1*, 2,3,7*,8, 9,10,11
7	Group A test requirements	1,2,3,4**, 7,8 9, 10,11	1,2, 3,4**, 7, 8,9,10,11	2, 3, 8, 10, 11	1,2,3,4**,7,8, 9,10,11
8	Group C end-point electrical parameters	1,2,3,7,8	1,2, 3,7,8	1, 7	1, 2, 3,7,8, 9, 10,11 Δ
9	Group D end-point electrical parameters	2,3,8	2, 3,8	- - -	2, 3,8
10	Group E end-point electrical parameters	1,7,9	1,7,9	- - -	1,7,9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limited shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan.
7/ See 4.4.1d.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

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a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA,Columbus, Ohio 43216-5000, or telephone (614)692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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Appendix A
FUNCTIONAL ALGORITHMS

10. Scope

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This Appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Mode Register Set (MRS). This pattern ensures that the device executes the proper sequence for each of the applicable device modes. The test verifies the proper operation of the mode register and mode control logic.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB)
Step 3: Set mode register (MRS)
Step 4: Activate bank, perform a write burst of data starting at location 0, and deactivate bank.
Step 5: Increment column address by burst length and repeat step 4 for entire row.
Step 6: Repeat steps 4 and 5 for each row address.
Step 7: Activate bank and perform read burst with proper read latency for data starting at location 0.
Step 8: Perform write burst of complement data starting at location 0 and deactivate bank.
Step 9: Increment column address by burst length and repeat steps 7 and 8 for entire row.
Step 10: Repeat 7, 8, and 9 for each row address.
Step 11: Read entire array for complement data.

This test is repeated for each applicable combination of burst length, burst type, and read latency that can be programmed by the mode register set (MRS) command. Test is performed at worst case limit V_{CC} levels and temperatures.

30.2 Algorithm B (pattern 2).

30.2.1 March Data, Bank Interleave. This algorithm tests for address uniqueness and multiple selection. It is also a primary check of many timing parameters. This test is designed to test the row and column address decode circuitry, address control, and the operations for writing and reading both one state and zero state from all memory cells in the memory array. Additionally, it is used to test for proper two-bank interleaved access operation.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Activate bottom and top memory banks.
Step 5: Perform a write burst of data starting at minimum address in bottom bank followed immediately by a write burst of data starting at minimum address in top bank.
Step 6: Deactivate both banks (DCAB).
Step 7: Increment row address and repeat steps 4, 5, and 6 for each row.
Step 8: Increment column address by burst length and repeat steps 4 - 7 through entire array.
Step 9: Activate bottom and top memory banks.

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Step 10: Perform a read burst with proper read latency for data followed by a write burst of complement data starting at minimum address in bottom bank.
Step 11: Immediately perform a read burst with proper read latency for data followed by a write burst of complement data starting at minimum address in top bank.
Step 12: Deactivate both banks (DCAB).
Step 13: Increment row address and repeat steps 9 - 12 for each row.
Step 14: Increment column address by burst length and repeat steps 9 - 13 through entire array.
Step 15: Activate bottom and top memory banks.
Step 16: Perform a read burst with proper read latency for complement data followed by a write burst of data starting at maximum address in top bank.
Step 17: Immediately perform a read burst with proper read latency for complement data followed by a write burst of data starting at maximum address in bottom bank.
Step 18: Deactivate both banks (DCAB).
Step 19: Decrement row address and repeat steps 15 - 18 for each row.
Step 20: Decrement column address by burst length and repeat steps 15 - 19 through entire array.
Step 21: Read entire array for data.

This test is repeated for each read latency mode with worst case timings and worst case topological data pattern for burst sequences.
Test is performed at worst case limit V_{CC} levels and temperatures.

30.3 Algorithm C (pattern 3).

30.3.1 Refresh Interval (tREF). This pattern is intended to check the retention time (tREF) of the memory cells in the memory array.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Load memory with data.
Step 5: Pause tREF. (stop all clocks).
Step 6: Read data from all memory locations.
Step 7: Repeat steps 4, 5, and 6 using complement data.

Standard read sequence and write sequence timings are used. Test is performed at worst case limit V_{CC} levels and temperatures.

30.4 Algorithm D (pattern 4).

30.4.1 Auto-refresh (REFR). This pattern verifies the functionality of the auto-refresh mode. It is a test of the refresh control circuitry, specifically the internal auto-row address counter.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Perform a write burst of data starting at minimum memory address.
Step 5: Increment column address by burst length and repeat steps 4 across row.
Step 6: Increment row address and repeat step 4 and 5 for new row.
Step 7: Repeat steps 4 - 6 until the refresh interval (tREF) has elapsed.
Step 8: Perform 4096 auto-refresh cycles with the REFR command in order to refresh the entire memory array.
Step 9: Repeat steps 4 - 8 until entire array is written with data.
Step 10: Perform read burst for data starting at minimum memory address.
Step 11: Increment column address by burst length and repeat steps 10 across row.
Step 12: Increment row address and repeat step 10 and 11 for new row.
Step 13: Repeat steps 10 - 12 until the refresh interval (tREF) has elapsed.

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Step 14: Perform 4096 auto-refresh cycles with the REFR command in order to refresh the entire memory array.
Step 15: Repeat steps 10 - 14 until entire array is read for data.
Step 16: Repeat steps 4 - 15 for complement data.

Relaxed read and write cycle timings are used to provide test execution over multiple refresh intervals.
Test is performed at worst case limit V_{CC} levels and temperatures.

30.5 Algorithm E (pattern 5).

30.5.1 Vcc Slew. This pattern indicates sense amplifier margin by slewing the voltage supply between memory writing and reading. It is a basic functional test of the sense amplifier circuitry.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Load memory with background data using V_{CC} at V_{CC} minimum.
Step 5: Change V_{CC} to V_{CC} maximum.
Step 6: Read data from memory.
Step 7: Write memory with data complement.
Step 8: Change V_{CC} to V_{CC} minimum.
Step 9: Read data complement from memory.
Step 10: Repeat steps 4 - 9 with complement data.

Test is performed at worst case limit V_{CC} levels and temperatures.

30.6 Algorithm F (pattern 6).

30.6.1 Write Burst Interrupt. Provided that all applicable timing requirements are met, write burst sequences can be interrupted by read (READ/READ-P), write (WRT/WRT-P), deactivate (DEAC/DCAB), and STOP commands. A series of tests are used to verify proper execution for each of the possible interrupting command sequences. The algorithms for these tests follow a standard format and are listed here together due to their similarity. These tests are designed to ensure functionality of the interrupt control logic.
They are performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Load memory with data.
Step 5: Activate bank and begin write burst of complement data.
Step 6: Interrupt write burst to inhibit writing of complement data to the remaining memory addresses of burst sequence.
Step 7: Read memory to verify correct combination of complement data and true data in the array.

Tests are performed at worst case limit V_{CC} levels and temperatures using worst case timings for interrupt sequences.

30.7 Algorithm G (pattern 7).

30.7.1 Read Burst Interrupt. Provided that all applicable timing requirements are met, read burst sequences can be interrupted by read (READ/READ-P), write (WRT/WRT-P), deactivate (DEAC/DCAB), and STOP commands. A series of tests are used to verify proper execution for each of the possible interrupting command sequences. The algorithms for these tests follow a standard format and are listed here together due to their similarity. These tests are designed to ensure functionality of the interrupt control logic. In addition, for read bursts interrupted by the DEAC/DCAB commands, the tests verify that the output buffers switch to high impedance (tri-state) as specified by tHZ and nHZP.
They are performed in the following manner:

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Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Load memory with data.
Step 5: Activate bank and begin read burst of data.
Step 6: Interrupt read burst and verify that interrupting command properly supersedes the initial read burst.

Tests are performed at worst case limit V_{CC} levels and temperatures using worst case timings for interrupt sequences.

30.8 Algorithm H (pattern 8).

30.8.1 Write Mask. This pattern verifies proper functionality of the input mask control circuitry. It assures that data input is inhibited during write cycles when the DQMU/DQML inputs are driven high.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Load memory with background data.
Step 5: Perform write burst cycles of complement data with the DQMU/DQML inputs high.
Step 6: Read data from memory.

Standard read and write cycle timings are used with worst case timing for DQMU/DQML mask operations.
Test is performed at worst case limit V_{CC} levels and temperatures.

30.9 Algorithm I (pattern 9).

30.9.1 Read Mask. This pattern verifies proper functionality of the output mask control circuitry. It assures that the data output buffers switch to high impedance during write cycles when the DQMU/DQML inputs are driven high.
It is performed in the following manner:

Step 1: Perform 8 REFR command cycles.
Step 2: Deactivate both banks (DCAB).
Step 3: Set mode register (MRS).
Step 4: Load memory with background data.
Step 5: Perform read burst cycles for data, and switch the DQMU/DQML inputs high during output burst cycles to verify that the outputs are properly disabled.
Step 6: Read data from memory.
Step 7: Repeat steps 4 - 6 for complement data

Standard read and write cycle timings are used with worst case timing for DQMU/DQML mask operations.
Test is performed at worst case limit V_{CC} levels and temperatures.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-03-16

Approved sources of supply for SMD 5962-97545 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9754501QXA	01295	SMJ626162-15HKDM
5962-9754501NYB	3/	SMJ626162-15DGE
5962-9754502QXA	01295	SMJ626162-20HKDM
5962-9754502NYB	3/	SMJ626162-20DGE
5962-9754503QXA	01295	SMJ626162-12HKDM
5962-9754503NYB	3/	SMJ626162-12DGE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P. O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

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