Low Power T1, T148C & 2 M Bit/s Repeater

GENERAL DESCRIPTION

The XR-T5760 is a low power version of the XR-T5700 repeater circuit for T1 carrier system operating at 1.544 M bit/s (T1), European 2 M bit/s or 2.37 M bit/s (T148C). It provides all of the active circuitry required for one side of a PCM repeater and also has the cability of clock extraction using a crystal filter.

Clock recovery using an LC tank circuit instead of a crystal filter is also available as XR-T5660.

FEATURES

Low Power
Crystal Filter Clock Extraction
Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse Over the Operating Range
Triple Matched Automatic Line Build-out (ALBO) Ports
2 M Bit/s Capability

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
European 2 M Bit/s PCM Repeater
T1C PCM Repeater (requires external preamplifier)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150C
Operating Temperature	−40°C to +85°C
Supply Voltage	−0.5 to +10V
Supply Voltage Surge (10 ms)	+25V
Input Voltage (except Pins 2,3,4,17)	−0.5 to 7V
Input Voltage (Pins 2,3,4,17)	−0.5 to +0.5V
Data Output Voltage (Pins 10,11)	20V
Voltage Surge (Pins 5,6,10,11) (10 msec only)	50V

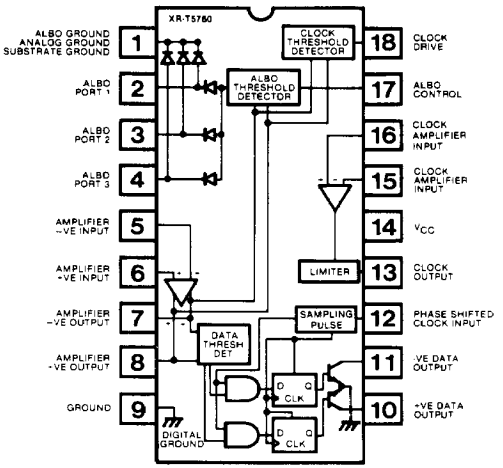
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5760	Ceramic	−40°C to +85°C

SYSTEM DESCRIPTION

The XR-T5760 is a monolithic bipolar PCM repeater IC operating at 1.544 (T1), 2.048 and 2.37 (T148C) M bits/sec. It is the low power version of XR-T5720 PCM repeater IC. It contains all the active circuitry to implement one side of a PCM, repeater operating on either pulp or plastic insulated cables. Repeater to repeater spacing on either type of cable is 6300 ft. max.

FUNCTIONAL BLOCK DIAGRAM



Bipolar PCM signal is attenuated and dispersed in time as it travels along the transmission cable, characteristics of which vary with length, frequency, temperature and humidity. The PCM signal when received is amplified, equalized for amplitude characteristics and reconstructed by the preamplifier, automatic line build out (ALBO), clock and data threshold circuits. Amplitude equalization is achieved through shaping the frequency spectrum with the help of variable impedance ALBO ports.

Timing information is contained in the incoming pulse stream. This signal is full wave rectified and applied to a crystal filter circuit to extract the clock signal at the data rate. The clock signal is amplified and phase shifted between Pins 13 and 12 to obtain 90° phase shift by means of an R-L-C circuit.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1 V ±5%, T_A = 25°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Current			14	mA	ALBO Off
Clock and Data Output					
Output Leakeage Current		0	100	μA	$V_{pull\text{-}up}$ = 15 V
Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
Amplifier Output					
Offset Voltage	−50	0	50	mV	R_S = 8.2 kΩ
Voltage Swing	2.2			V	Measured Differentially from Pin 8 to Pin 7
Amplifier Input					
Bias Current			5	μA	
ALBO on Current	3			mA	
Drive Current		1		mA	
AC CHARACTERISTICS					
Pre-Amplifier					
AC Gain at 1 MHz		50		dB	
Input Impedance	20			kΩ	
Output Impedance			200	Ω	
Clock Amplifier					
AC Gain		32		dB	
−3 dB Bandwidth	10			MHz	
Delay		10		ns	
Output Impedance			200	Ω	
ALBO					
Off Impedance	20			kΩ	
On Impedance			25	Ω	
DATA OUTPUT BUFFERS					R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1 V ±5%
Rise Time		30		ns	
Fall Time		30		ns	
Output Pulse Width		244		ns	
Sample Pulse Width		10		ns	
V_{OL}		0.7		V	
I_L sink		35		mA	
THRESHOLDS					
ALBO	1.4	1.5	1.6	V	
Clock Drive Current Peak		1.0		mA	At V_O = V_{ALBO} Threshold
CLOCK THRESHOLD					
% of ALBO	63	68	75	%	
DATA THRESHOLD					
% of ALBO	40	46	52	%	