B8ZS/AMI Line Transcoder

GENERAL DESCRIPTION

The XR-T5670 is an LSI CMOS integrated circuit which performs the B8ZS or AMI transmission coding and receiving decoding functions with error detection. It is intended for DS1 (1.544MBPS) PCM transmission applications, but can operate at clock frequencies up to 6MHz.

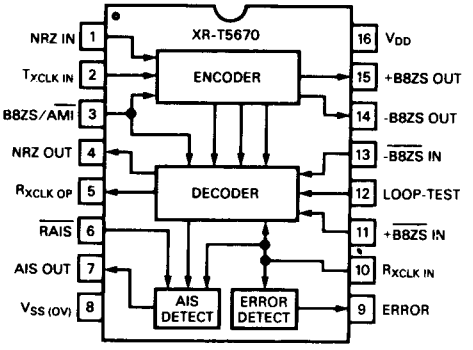
FEATURES

B8ZS Coding and Decoding for Data Rates up to 6MBPS to AT&T Technical Advisory 69
B8ZS/AMI Transmission Coding/Reception Decoding with Code Error Detection
All Transmitter and Receiver Inputs/Outputs are TTL Compatible
Internal Loop Test Capability
Single 5V ± 10% Supply Rail

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD})	-0.3 to 7.0V
Input Voltage Range (V_{IN})	-0.3 to V_{DD} + 0.3V
Input Protection Current (I_D)	±10mA
Storage Temperature Range	-55°C to 150°C,

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5670CP	Plastic	0°C to 70°C
XR-T5670CN	Ceramic	-40°C to +85°C

APPLICATIONS

AMI Encoding/Decoding
B8ZS Encoding/Decoding

SYSTEM DESCRIPTION

Coder

Binary data in "NRZIN" is clocked into the coder by a synchronous transmission clock "T_{XCLKIN}" on the failing edge. The "+B8ZS" and "-B8ZS" output signals appear 8.5 clock cycles later to allow for the insertion of extra pulses due to sequences of eight consecutive zeros. These two signals are full width data and will be mixed with the "T_{XCLKIN}" at the input of an external line driver to produce bipolar B8ZS signals for transmission.

Decoder

Received half width data on "+$\overline{\text{B8ZSIN}}$" and "-$\overline{\text{B8ZSIN}}$" are locked into the decoder on the rising edge of the received clock "R_{XCLKIN}". The "NRZOUT" binary data output occurs on eight clock cycles later. Received signals not consistant with B8ZS coding rules are detected as errors. The error output "ERROR" is active high during one "R_{XCLKIN}" clock period. The error output is not an accurate measure of error count; it is intended for alarm indication only.

AIS (Alarm Indication Signal)

If the decoder inputs received a continuous of ones (all marks) over two consecutive periods of the external reset signal "$\overline{\text{RAIS}}$", the "AISOUT" output will be set high and latched in that state until one or more zeros are received when the next reset signal "$\overline{\text{RAIS}}$" occurs.

The number of received zeros required to reset "AISOUT" over two consectuive periods of "$\overline{\text{RAIS}}$" can be mask programmed to two or three.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40°C$ to $+85°C$, $V_{DD} = 4.5$ to $5.5V$, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX	UNIT	CONDITIONS
DYNAMIC CHARACTERISTICS						
T_{XCLKIN}	Clock Input Frequency			6	MHz	
R_{XCLKIN}	Clock Input Frequency			6	MHz	
t_{s1}	Data Set-Up Time	55			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{h1}	Data Hold Time	25			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{pd1}	Data Propagation Delay Time			65	ns	T_{XCLKIN} to B8ZS OUT See Figure, 3 and 6. Note 1
t_{s2}	Data Set-Up Time	55			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{h2}	Data Hold Time	0			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{pd2}	Data Propagation Delay Time			90	ns	R_{XCLKIN} to NRZOUT See Figures 4 and 7, Note 2 Loop Test = 0
t_{pd3}	Clock Delay Time			50	ns	R_{XCLK} IN to $R_{XCLKOUT}$ See Figure 8, Loop Test = 0
t_{s3}	RAIS = 0 Set-Up Time	30			ns	RAIS to R_{XCLKIN} See Figure 7
t_{h3}	RAIS= 0 Hold Time	30			ns	RAIS to R_{XCLKIN}
STATIC CHARACTERISTICS, $V_{DD} = 5.0V$						
I_{DD}	Quiescent Device Current			100	µA	
	Operating Current			4	mA	Input Clock Frequency = 2.0MHz
V_{DD}	Supply Voltage	4.5	5	5.5	V	
V_{IN}	Input Voltage 0	0		5.0	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.1	V	$I_{OL} = 0$
V_{OH}	Output High Voltage	4.9			V	$I_{OH} = 0$
I_{OL}	Output Lo, Current	1.6			mA	$V_{OL} = 0.4V$
I_{OH}	Output High Current	−1			mA	$V_{OH} = 4.6V$
I_{IL}	Input Low Current			−10	µA	$V_{IL} = 0V$
I_{IH}	Input High Current			10	µA	$V_{IH} = 5V$

Note 1: The encoded B8ZS OUT are delayed by 8 1/2 clock periods from NRZIN.
Note 2: The decoded NRZOUT are delayed by 7 = clock periods from B8ZS IN.

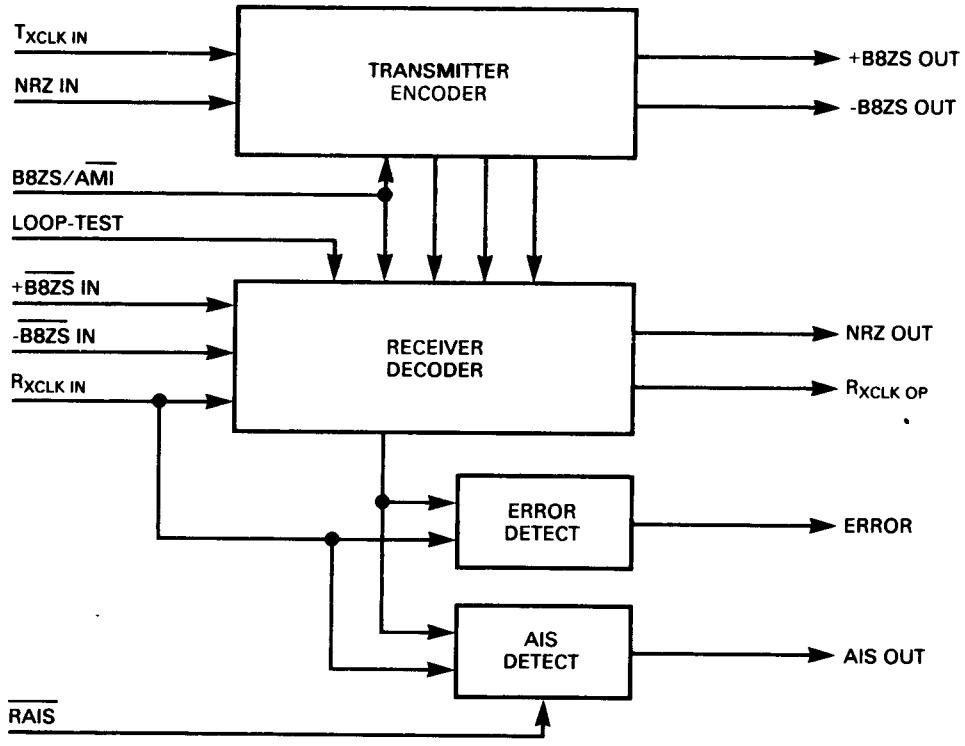


Figure 1. XR-T5670 Block Diagram

Loop Test

When the Loop Test control input is set high, a test mode is made in which the "+B8ZSOUT" and "–B8ZSOUT" are internally connected to the decoder inputs. The external B8ZS inputs and the "R_{XCLKIN}" are disabled, and the "T_{XCLKIN}" is used to control the decoder timing. The "NRZOUT" signals correspond to the "NRZIN" input, but delayed by 16 clock periods.

B8ZS/AMI

To operate the XR-T5670 in AMI mode, the B8ZS/AMI control input is driven low. In this mode, two consecutive pulses of the same polarity at the decoder inputs will be detected and flagged as an error at the "ERROR" output.

Definition of B8ZS Code Used in XR-T5670 Transcoder

With B8ZS coding, each block of eight consecutive zeros is removed and the B8ZS code is inserted. If the pulse preceding the inserted code is transmitted as a positive pulse (+), the inserted code is 000+–0–+. Bipolar violations occur in the fourth and seventh bit position of the inserted code. If the pulse preceeding the inserted code is a negative pulse (–), the inserted code is 000–+0+–. Bipolar violations again occur in the fourth and seventh bit positions as illustrated in Figure 2.

Binary Signal	1	0	0	0	0	0	0	0	0
B8ZS Signal	+1	0	0	0	+1	–1	0	–1	+1
or	–1	0	0	0	–1	+1	0	+1	–1

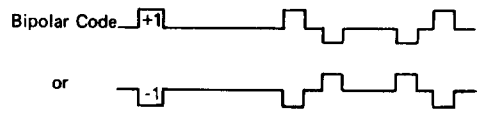


Figure 2. B8ZS Code

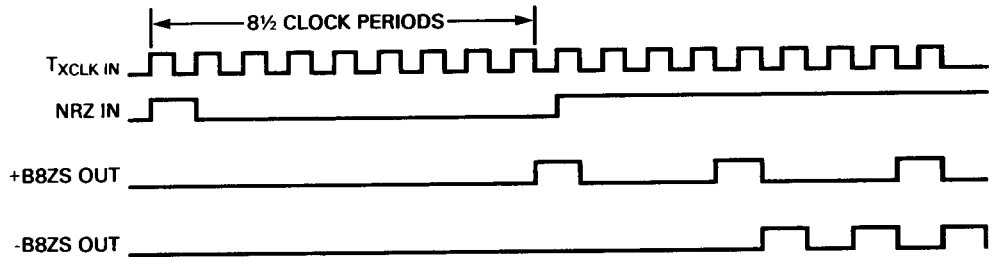


Figure 3. Encoder Waveforms

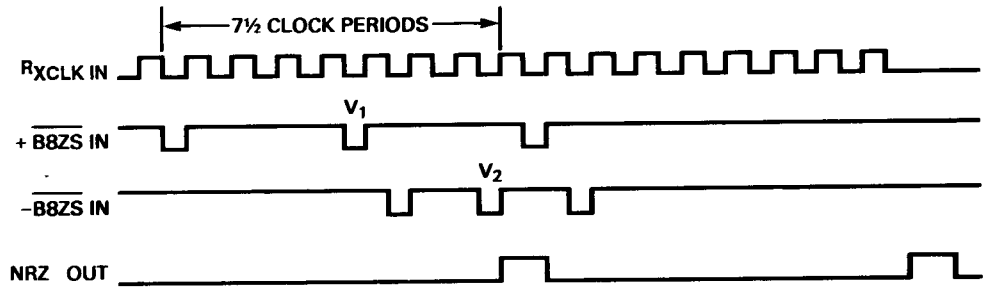


Figure 4. Decoder Waveforms

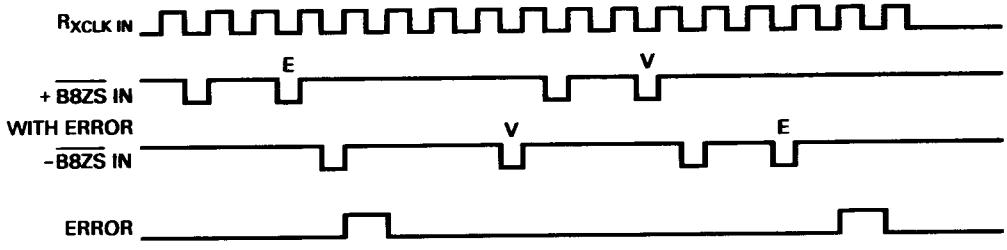


Figure 5. B8ZS Error Output Waveforms

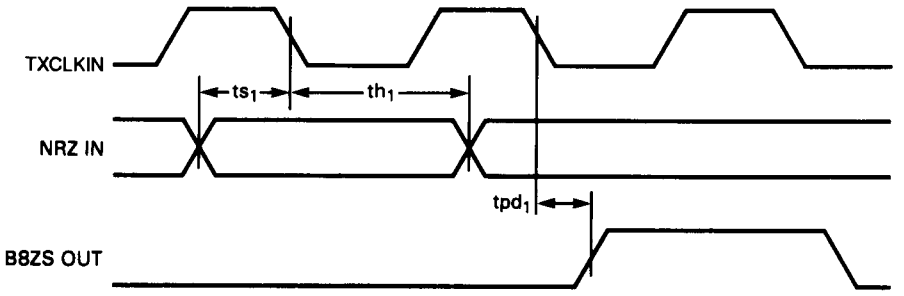


Figure 6. Encoder Timing Relationship

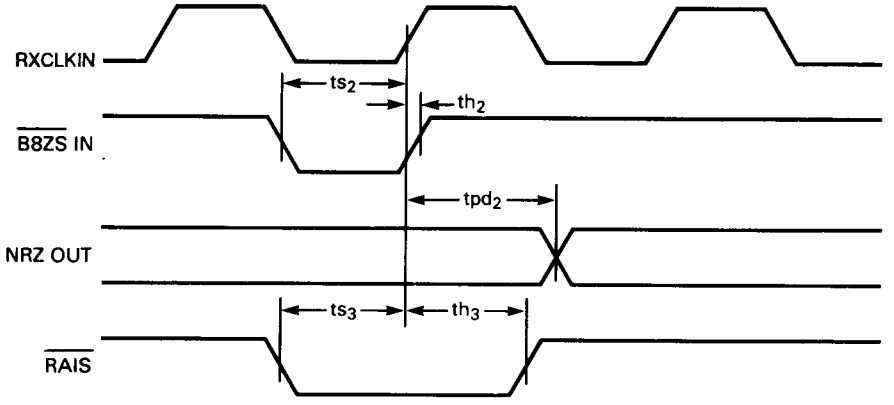


Figure 7. Decoder Timing Relationship

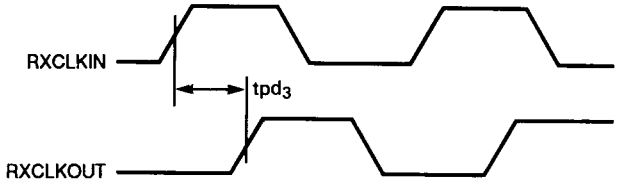


Figure 8. RXCLKIN To R XCLKOUT Relationship