NEC

BiCMOS INTEGRATED CIRCUIT

μPD3150GS

1 150 MHz/200 MHz DUAL PLL FREQUENCY SYNTHESIZER LSI FOR ANALOG CELLULAR PHONE

DESCRIPTION

μPD3150GS is a PLL frequency synthesizer LSI for analog cellular phone. This LSI is manufactured using 13 GHz f_T Bi-CMOS process and integrated 700 MHz to 1 150 MHz prescaler+PLL and 40 MHz to 200 MHz prescaler+PLL. This LSI realized low power consumption: on 3 V, 6.2 mA at dual operation. The additional functions are settings of decreased lock-up time and phase sensitivity. The package is 20 pin plastic SSOP suitable for high-density surface mounting.

Thus, this product contributes to produce low power-consumption, long-life battery and high performance hand-held systems.

FEATURES

- Supply voltage: V_{CC} = V_{DD} = 2.7 to 5.5 V
- Input operating frequency: f_{in1} = 700 MHz to 1 150 MHz PLL 1ch
  f_{in2} = 40 MHz to 200 MHz PLL 2ch
- Built-in power-save control pins: Control 2 prescaler's ON/OFF operation individually.
- Low power consumption: $I_{CC}OP$ = 6.2 mA TYP. @ V_{CC} = 3.0 V, Dual operation (both ch ON)
- Decreased lock-up time (eg 20 ms) available: Charge pump switch control (PLL 1ch only)
- Lock-phase sensitivity programmable: Phase difference allowance for lock up can be controlled as 4 stages. (5 μs/1.5 μs/500 ns/150 ns)
- High-density surface mounting: 20 pin plastic SSOP.

ORDERING INFORMATION

PARTS NUMBER	PACKAGE	SUPPLYING FORM
μPD3150GS-E1	20-pin plastic SSOP (300 mil)	Embossed tape 16 mm wide. QTY 2.5 k/reel Pin 1 is in tape pull-out direction.
μPD3150GS-E2		Embossed tape 16 mm wide. QTY 2.5 k/reel Pin 1 is in tape roll-in direction.

* To order evaluation samples, please contact your local NEC sales office (Order number: μPD3150GS).

Caution: Electro-static sensitive device

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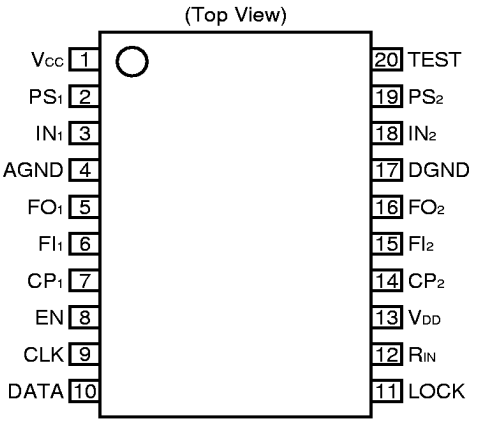
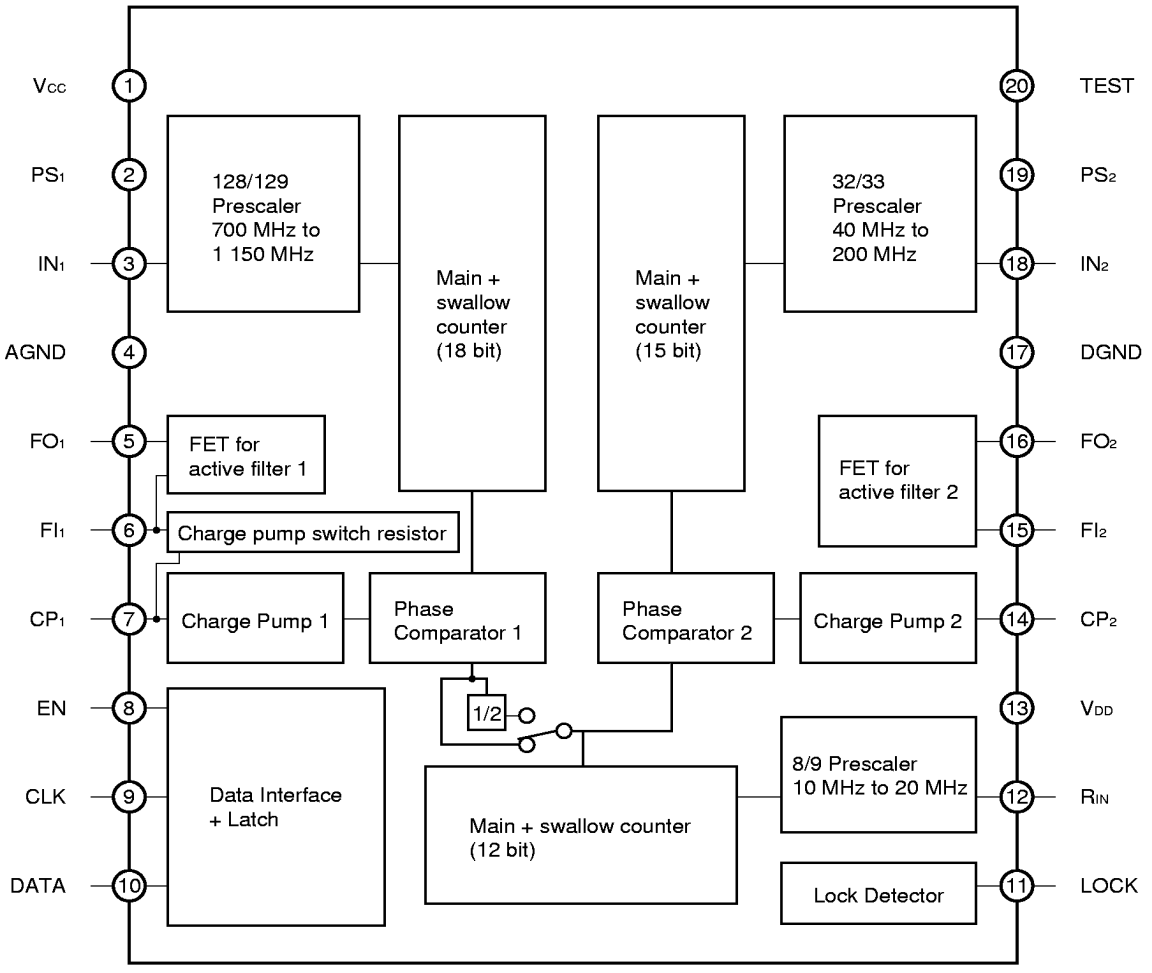
PIN ASSIGNMENT (Top View)

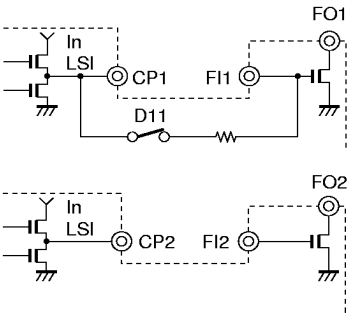


INTERNAL BLOCK DIAGRAM



PIN EXPLANATIONS

PIN No.	SYMBOL	APPLIED VOLTAGE (V)	EXPLANATIONS
1	V_{CC}	2.7 to 5.5	Supply voltage for analog block and 2 prescalers. This pin must be equipped with bypass capacitor to minimize ground impedance. (mainly high frequency)
2 19	PS_1 PS_2	HIGH or LOW	Power save control pin. PS_1: for PLL 1ch PS_2: for PLL 2ch
3 18	IN_1 IN_2	—	Inputs for internal 2 modulus prescaler. This pin must be coupled to VCO with DC cut capacitor (eg 1 000 pF). IN_1: prescaler input for PLL 1ch IN_2: prescaler input for PLL 2ch
4	AGND	GND	Ground pin of analog block and 2 prescalers. Ground pattern on the board must be formed as wide as possible to minimize ground impedance.
5 16	FO_1 FO_2	Pull up to V_{CC} with resister	Drain output of active filter's FET FO_1: for PLL 1ch FO_2: for PLL 2ch
6 15	FI_1 FI_2	—	Gate input pin of active filter's FET FI_1: for PLL 1ch FI_2: for PLL 2ch
7 14	CP_1 CP_2	—	Charge pump output pin. CP_1: Charge pump output from PLL 1ch CP_2: Charge pump output from PLL 2ch
8	EN	HIGH to LOW	Load enable data input pin
9	CLK		Clock data input pin
10	DATA		Data input pin
11	LOCK	Pull up to V_{CC} with resister	Lock detector output pin. This pin is designed as open drain. Relation between operation mode and conditions to output is as follows. (In other case, LOCK pin output high as unlock.)
12	R_{IN}	—	Reference signal input for both PLL. This pin should be coupled to TCXO with DC cut capacitor. V_{IN} = –10 to 0 dBm, f_{ref} = 10 MHz to 20 MHz
13	V_{DD}	2.7 to 5.5	Supply voltage for PLL digital block (PLL 1ch, PLL 2ch in common). This pin must be equipped with bypass capacitor to minimize ground impedance. (mainly low frequency)
17	DGND	GND	Ground pin of PLL digital block (PLL 1ch, PLL 2ch in common). Ground pattern on the board must be formed as wide as possible to minimize ground impedance.
20	TEST	—	Test pin (Refer to page 7). Used as PLL, this pin should be grounded.



OPERATE MODE	CONDITION TO OUTPUT LOCK	LOCK OUTPUT
SINGLE OPERATION	1 PLL LOCKED	LOW (SINK)
DUAL OPERATION	2 PLL LOCKED	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{DD}	–0.3 to +6.0	V
Circuit Current	I_{CC}	35	mA
Operating Temperature	$T_{A(opt)}$	–30 to +85	°C
Storage Temperature	$T_{A(stg)}$	–40 to +125	°C

GUARANTEED OPERATING RANGE

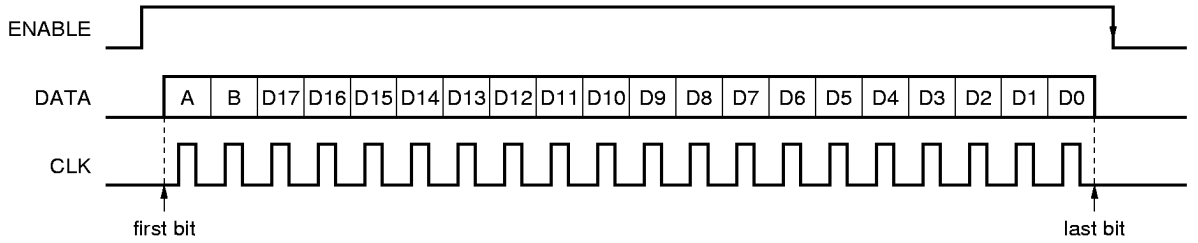
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply Voltage	V_{CC}, V_{DD}	2.7	3.0	5.5	V	$V_{CC} = V_{DD}$
Operating Temperature	$T_{A(opt)}$	–30	+25	+85	°C	

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, in the conditions of guaranteed operating range.)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Circuit Current PS	I_{CCPS}	—	—	100	μA	$V_{CC} = V_{DD}$ = 3 V, Both ch powersave
Circuit Current OP1	I_{CCOP1}	—	4.6	7.5	mA	$V_{CC} = V_{DD}$ = 3 V, PLL1ch operation
Circuit Current OP2	I_{CCOP2}	—	2.3	3.6	mA	$V_{CC} = V_{DD}$ = 3 V, PLL2ch operation
Circuit Current OP	I_{CCOP}	—	6.2	9.8	mA	$V_{CC} = V_{DD}$ = 3 V, dual ch operation
Input Operating Frequency for PLL 1ch	f_{in1}	700	—	1 150	MHz	V_{in} = –13 to 0 dBm
Input Operating Frequency for PLL 2ch	f_{in2}	40	—	100	MHz	V_{in} = –8 to 0 dBm
		100	—	200	MHz	V_{in} = –12 to 0 dBm
Reference Frequency (R_{IN})	f_{ref}	10	—	20	MHz	V_{in} = –10 to 0 dBm
High Level Input Voltage	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} +0.5	V	EN, CLK, DATA, PS1, PS2, pin, T_A = +25 °C
Low Level Input Voltage	V_{IL}	–0.5	—	0.8	V	EN, CLK, DATA, PS1, PS2, pin, T_A = +25 °C
Clock Rate	C_{rate}	1 μ	—	1	s	EN, CLK, DATA pin, T_A = +25 °C
Charge Pump Leak Current	I_{CPleak}	—	—	±100	nA	T_A = +25 °C, charge pump output: high-impedance
Charge Pump Output Current 1	CPI_{000}	10	20	40	μA	$V_{CC} = V_{DD}$ = 3 V, CP-data. 000
Charge Pump Output Current 2	CPI_{001}	30	50	80	μA	$V_{CC} = V_{DD}$ = 3 V, CP-data. 001
Charge Pump Output Current 3	CPI_{010}	60	100	160	μA	$V_{CC} = V_{DD}$ = 3 V, CP-data. 010
Charge Pump Output Current 4	CPI_{100}	120	200	320	μA	$V_{CC} = V_{DD}$ = 3 V, CP-data. 100
Charge Pump Output Voltage	CPV_{111}	—	0.1	—	V	$V_{CC} = V_{DD}$ = 3 V, CP-data. 111
Output Current of LOCK pin	LOI	300	—	—	μA	Open drain output, T_A = +25 °C, V_O = 0.5 V

Data Format



Note Data can be clocked in at falling edge of the CLK.

1. Relation between A, B data and setting data content

A	B	Setting data content
0	0	PLL 1ch (3 pin input) counter data
0	1	PLL 2ch (18 pin input) counter data
1	0	Option data
1	1	Reference counter data (PLL 1ch, 2ch, common)

2. Counter data

PLL 1ch counter Number : N1 = $D17 \times 2^{17} + D16 \times 2^{16} + D15 \times 2^{15} + D14 \times 2^{14} + D13 \times 2^{13} + D12 \times 2^{12} + D11 \times 2^{11} + D10 \times 2^{10} + D9 \times 2^{9} + D8 \times 2^{8} + D7 \times 2^{7} + D6 \times 2^{6} + D5 \times 2^{5} + D4 \times 2^{4} + D3 \times 2^{3} + D2 \times 2^{2} + D1 \times 2^{1} + D0 \times 2^{0}$

Continuous setting range = 16 384 to 262 143

PLL 2ch counter Number : N2 = $D14 \times 2^{14} + D13 \times 2^{13} + D12 \times 2^{12} + D11 \times 2^{11} + D10 \times 2^{10} + D9 \times 2^{9} + D8 \times 2^{8} + D7 \times 2^{7} + D6 \times 2^{6} + D5 \times 2^{5} + D4 \times 2^{4} + D3 \times 2^{3} + D2 \times 2^{2} + D1 \times 2^{1} + D0 \times 2^{0}$

Continuous setting range = 1 024 to 32 767

- Reference Counter Number : R = $D11 \times 2^{11} + D10 \times 2^{10} + D9 \times 2^{9} + D8 \times 2^{8} + D7 \times 2^{7} + D6 \times 2^{6} + D5 \times 2^{5} + D4 \times 2^{4} + D3 \times 2^{3} + D2 \times 2^{2} + D1 \times 2^{1} + D0 \times 2^{0}$

Continuous setting range = 64 to 4 095 (× 2)*

*

D12	Magnification of reference counter number	
	PLL 1ch	PLL 2ch
0	× 1	× 1
1	× 2	× 1

3. Option setting

<1> D0 to D5: Charge pump driving capability setting (CP data)

D2 (D5)	D1 (D4)	D0 (D3)	Charge pump driving capability	
			capability	Output current
0	0	0	weak	20 μA
0	0	1	↓	50 μA
0	1	0	↓	100 μA
1	0	0	↓	200 μA
1	1	1	strong	Voltage output

1 Values in the table are typical at $V_{CC} = V_{DD} = 3$ V

2 D0 to D2: PLL 1ch
D3 to D5: PLL 2ch

3 Other data can be set in accordance with accumration as follows
exp. Data : 011 (010 + 001)
Output current: 150 μA (100 + 50)

<2> D6: Charge pump polarity (PLL 1ch, 2ch common)

D6	Charge pump output polarity	Input phase status against reference signal phase			Required loop filter type
		phase advanced	phase delayed	Sychronized	
0	Positive	Low	High	High Impedance	Passive filter
1	Negative	High	Low	High Impedance	Active filter

<3> D7, 8: Charge pump output automatic control

D7, D8	CPout V/I control
0	Only Current output of CP data
1	Voltage output → Current output of CP data

D7: PLL 1ch
D8: PLL 2ch

<4> D9, 10: Lock phase sensitivity (PLL 1ch, 2ch in common) LOCK data

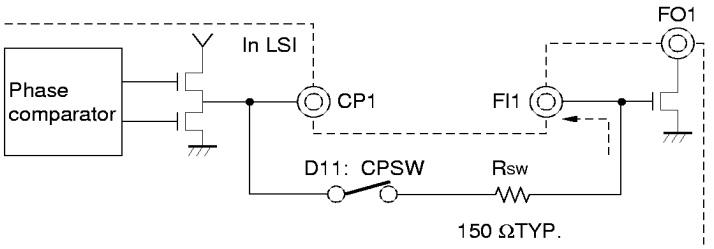
D10	D9	*
0	0	150 ns
0	1	500 ns
1	0	1.5 μs
1	1	5.0 μs

* Phase difference allowance for lock-up
Input signal phase against reference signal phase.
The values in the table are for reference.

<5> D11 to 13: Charge pump switch control setting (automatic operation by advance settings): PLL 1ch only
CPSW

D11	Output route control
0	CPout only
1	CPSWout → CPout

Internal block diagram of output stage

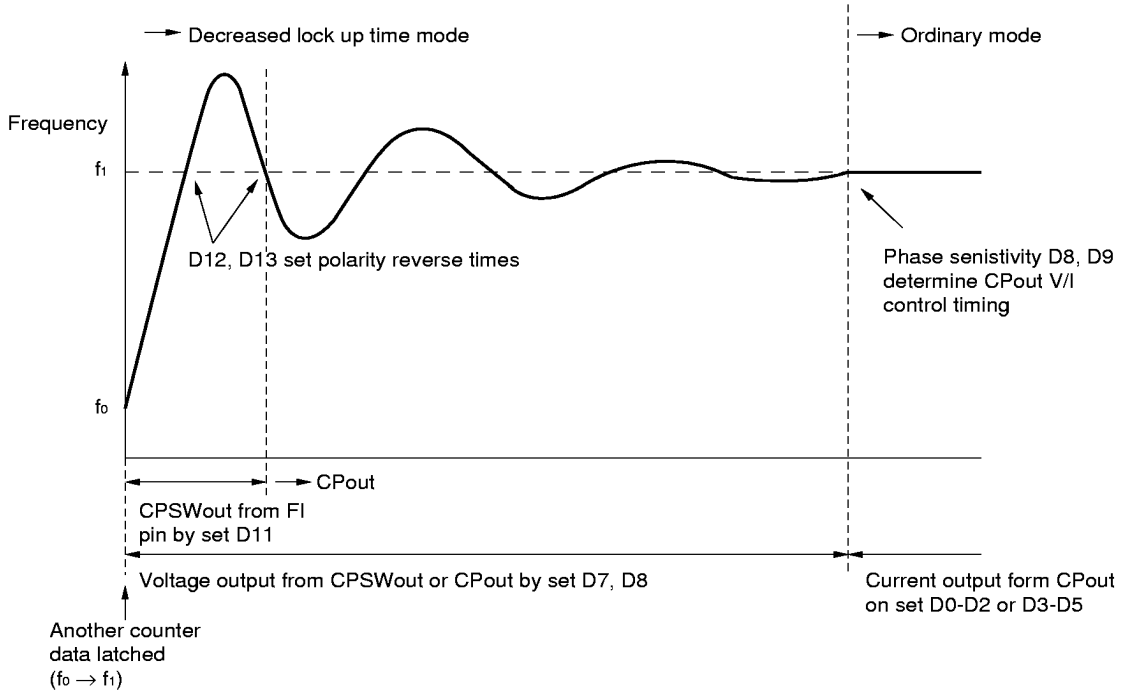


Note:
CPSWout is routed through the FI pin.

D13	D12	CPSWout polarity reverse time
0	0	1 time
0	1	2 times
1	0	4 times
1	1	8 times

Usage of decreased lock up time mode

Fig. Output locus on option data D7, D11 = 1, 1 set in advance



When another counter data is latched, lock up mode is altered automatically as shown above. On the other hand, when same counter data is latched, lock up mode keeps stable PLL loop.

Power save function

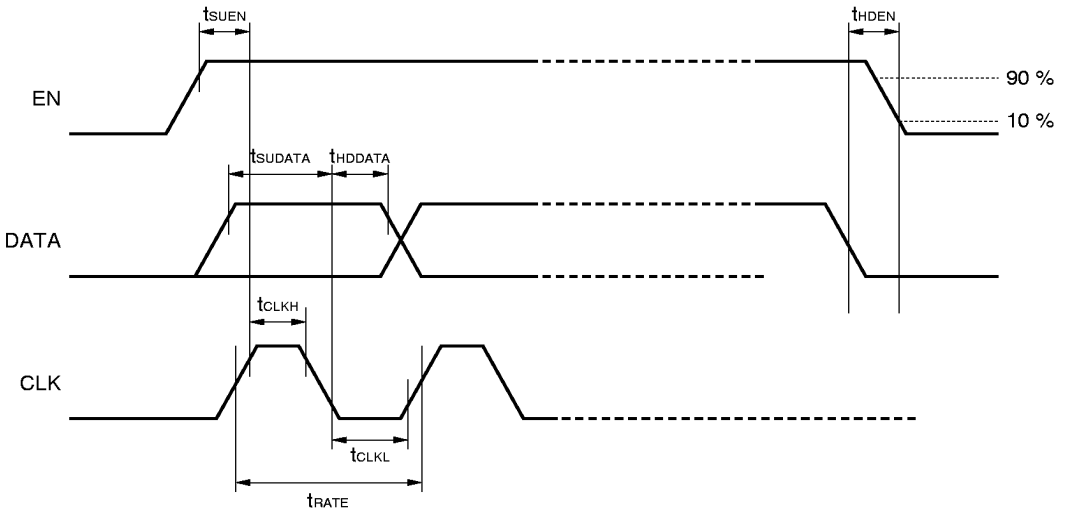
According to H/L on PS1 and PS2, prescaler of PLL 1ch and PLL 2ch can be controlled ON/OFF individually. Relation between H/L and ON/OFF is shown below. (PLL digital block is always ON.)

PS1, PS2: Prescaler operation control

PS1	PS2	PLL 1ch	PLL 2ch
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

OFF PLLch's CPout: Hi-impedance
ON PLLch's CPout: 3 state as H/L/Hi-impedance

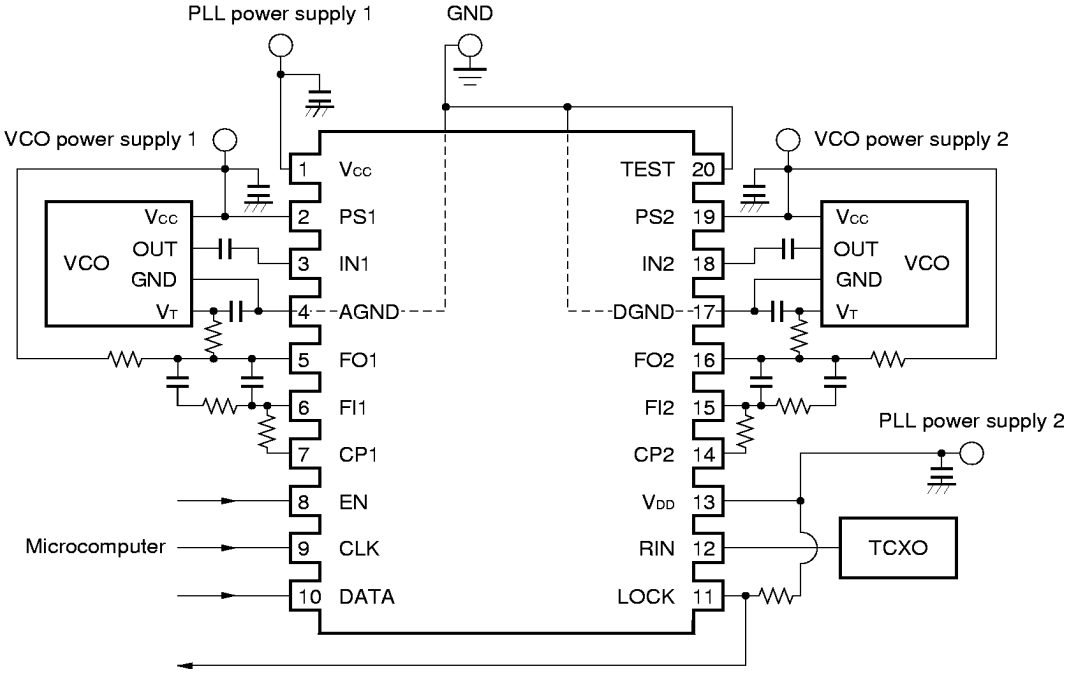
Serial data input timing



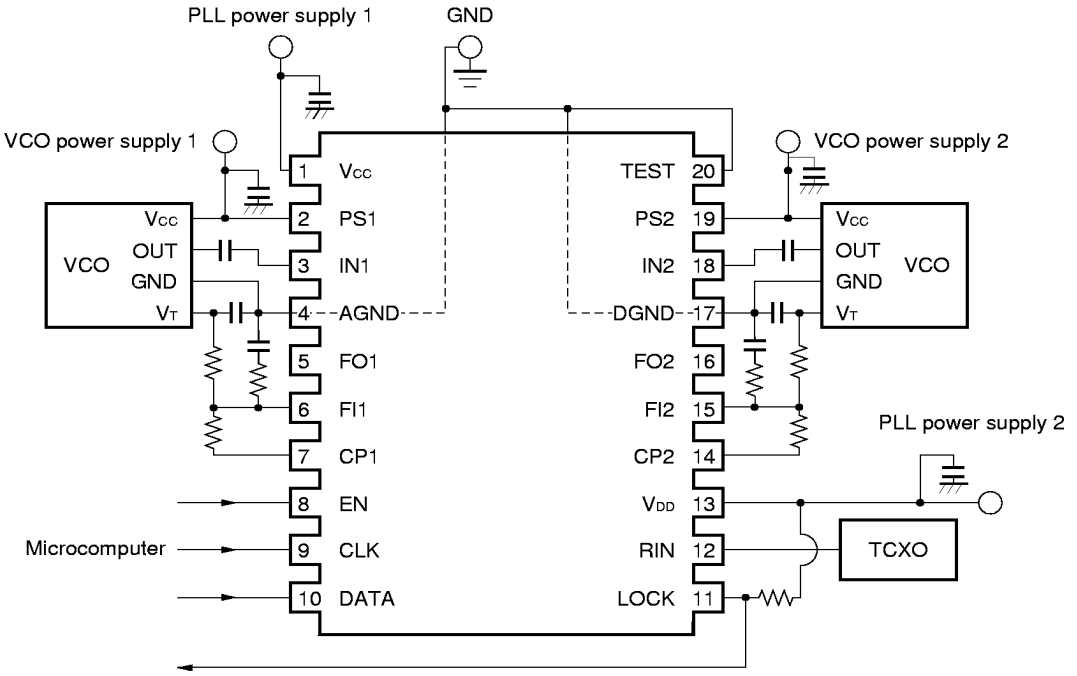
Parameter	Specification
EN set up time	$t_{SUEN} \geq 500$ ns
EN hold time	$t_{HDEN} \geq 500$ ns
DATA set up time	$t_{SUDATA} \geq 300$ ns
DATA hold time	$t_{HDDATA} \geq 300$ ns
CLK high level time	$t_{CLKH} \geq 300$ ns
CLK low level time	$t_{CLKL} \geq 300$ ns
CLK rate	1 μs $\leq t_{RATE} \leq$ 1 s

Application Circuit Examples

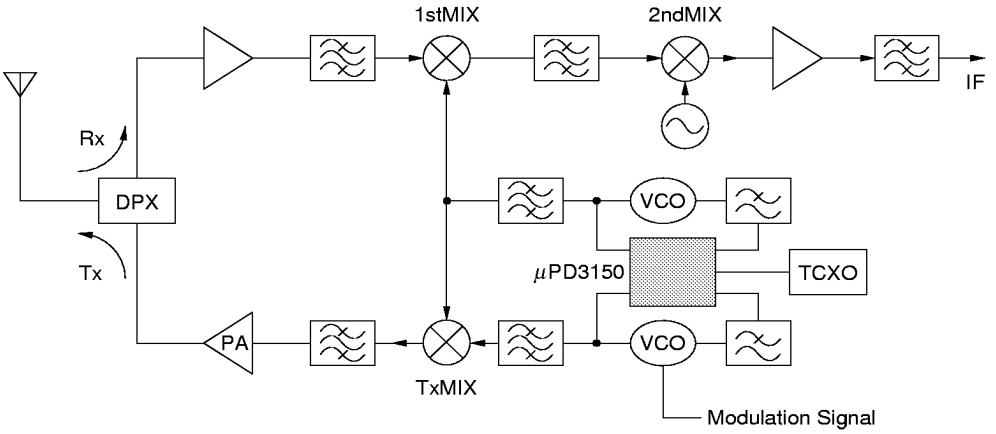
Active loop filter



Passive loop filter

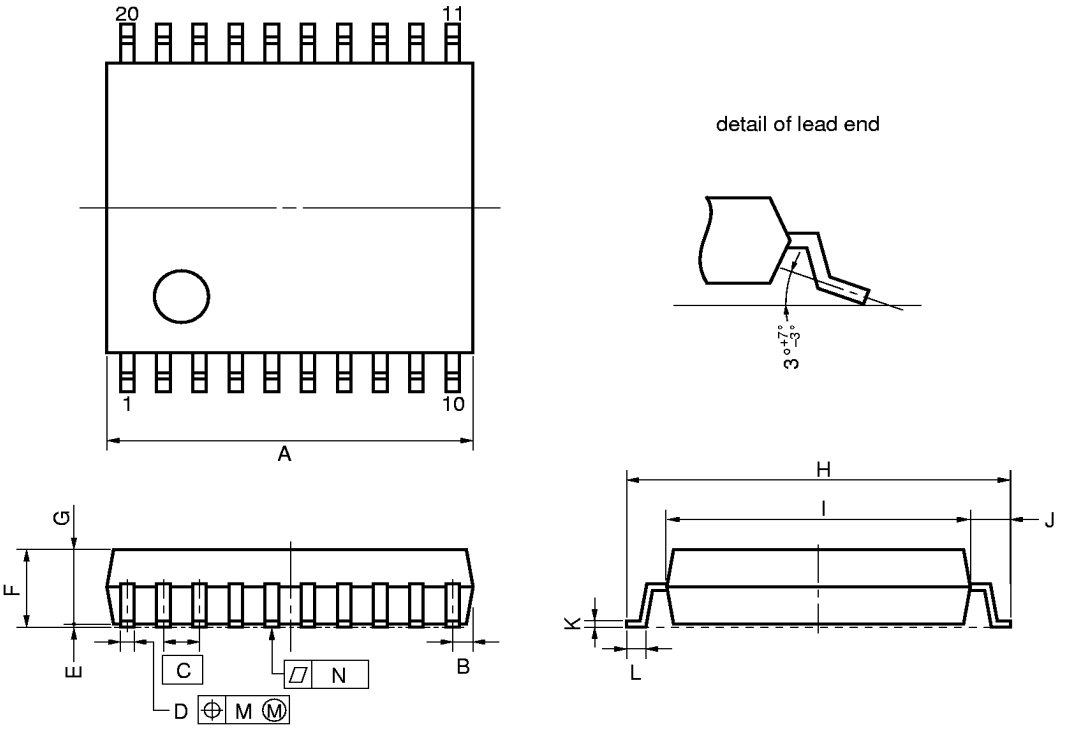


System block diagram example for analog cellular application



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

20 PIN PLASTIC SHRINK SOP (300 mil)



P20GM-65-300B-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	7.00 MAX.	0.276 MAX.
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30 ± 0.10	$0.012^{+0.004}_{-0.005}$
E	0.125 ± 0.075	0.005 ± 0.003
F	2.0 MAX.	0.079 MAX.
G	1.7	0.067
H	8.1 ± 0.3	0.319 ± 0.012
I	6.1 ± 0.2	0.240 ± 0.008
J	1.0 ± 0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5 ± 0.2	$0.020^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPD3150GS

Soldering method	Soldering conditions	Symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 2 times, Limited days: no.*	IR35-00-2
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 2 times, Limited days: no.*	VP15-00-2
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s/pin. Limited days: no.*	

*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. Apply only a single process at once (except the pin part heating method.)

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (Document No. C10535E)

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Connect a bypass capacitor (e. g. 1 000 pF) to the V_{CC} pin.
(3) External R, C values of loop filter should be determined according to the VCO specification.
(4) Form a ground pattern as wide as possible to minimize ground impedance.
(5) After initially V_{CC}, V_{DD} are supplied, serial data should be input immediately. (Before serial data input, LSI operation is unstable or undesired.)