PRELIMINARY DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8126K

900 MHz BAND DIRECT QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATION SYSTEMS

DESCRIPTION

The μPC8126K is a silicon monolithic integrated circuit designed as quadrature modulator for digital mobile communication systems. This IC integrates a pre-mixer for local signals plus a quadrature modulator operating from 889 MHz to 960 MHz. The chip which has been conventionally packaged in 20-pin SSOP is packaged in 28-pin QFN and therefore is suitable for higher density mounting. In addition, the IC has power save function and can operate 2.7 to 3.6 V supply voltage. Consequently the μPC8126K can contribute to make RF blocks smaller size, higher performance and lower power consumption.

FEATURES

- Directly modulate in 889 MHz to 960 MHz
- Built-in pre-mixer for local signals
- External IF filter can be applied between modulator output and pre-mixer input terminal.
- Current consumption I_{CC} = 35 mA TYP. @ V_{CC} = 3.0 V
- Equipped with power save function.
- 28-pin QFN suitable for higher density mounting.

APPLICATIONS

- Digital cellular phones: PDC800M

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC8126K-E1	28-pin plastic QFN (5.1 × 5.5 × 0.95 mm)	Embossed tape 12 mm wide. QTY 2.5 kp/reel. Pins 1 through 10 are in pull-out direction.

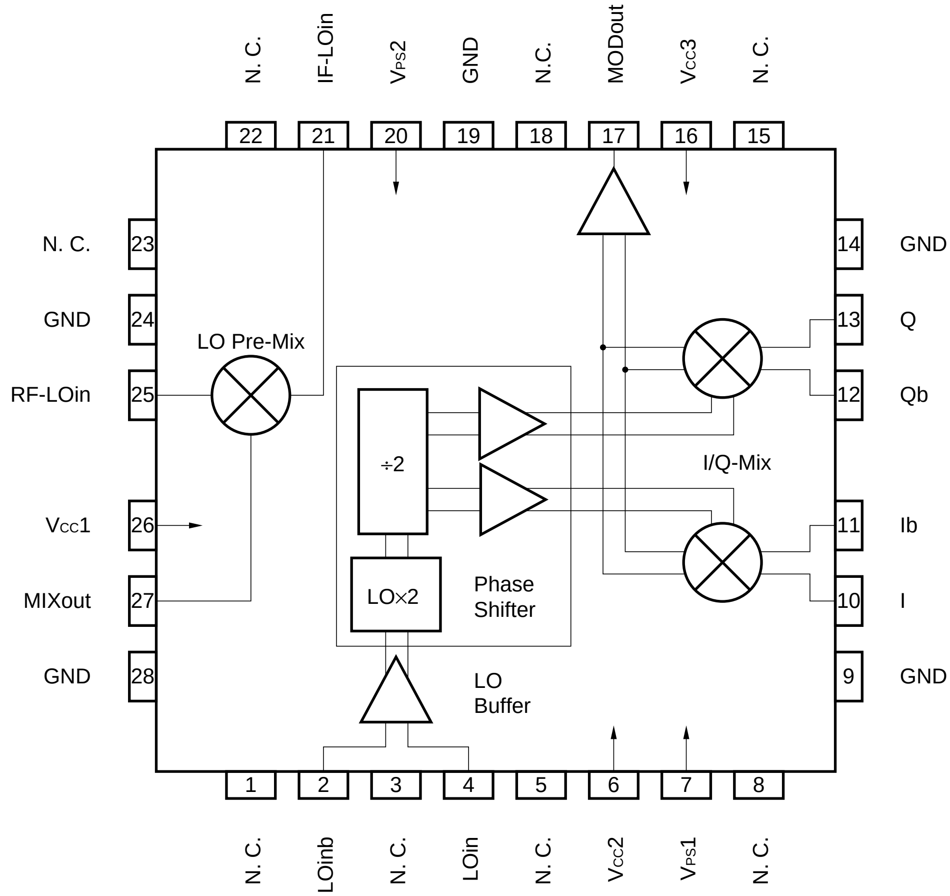
Remark To order evaluation samples, please contact your local NEC sales office .
(Part number for sample order: μPC8126K)

Caution Electro-static sensitive device

The information in this document is subject to change without notice.

Document No. P13488EJ1V0DS00 (1st edition)
Date Published February 1999 N CP(K)
Printed in Japan

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (Top View)

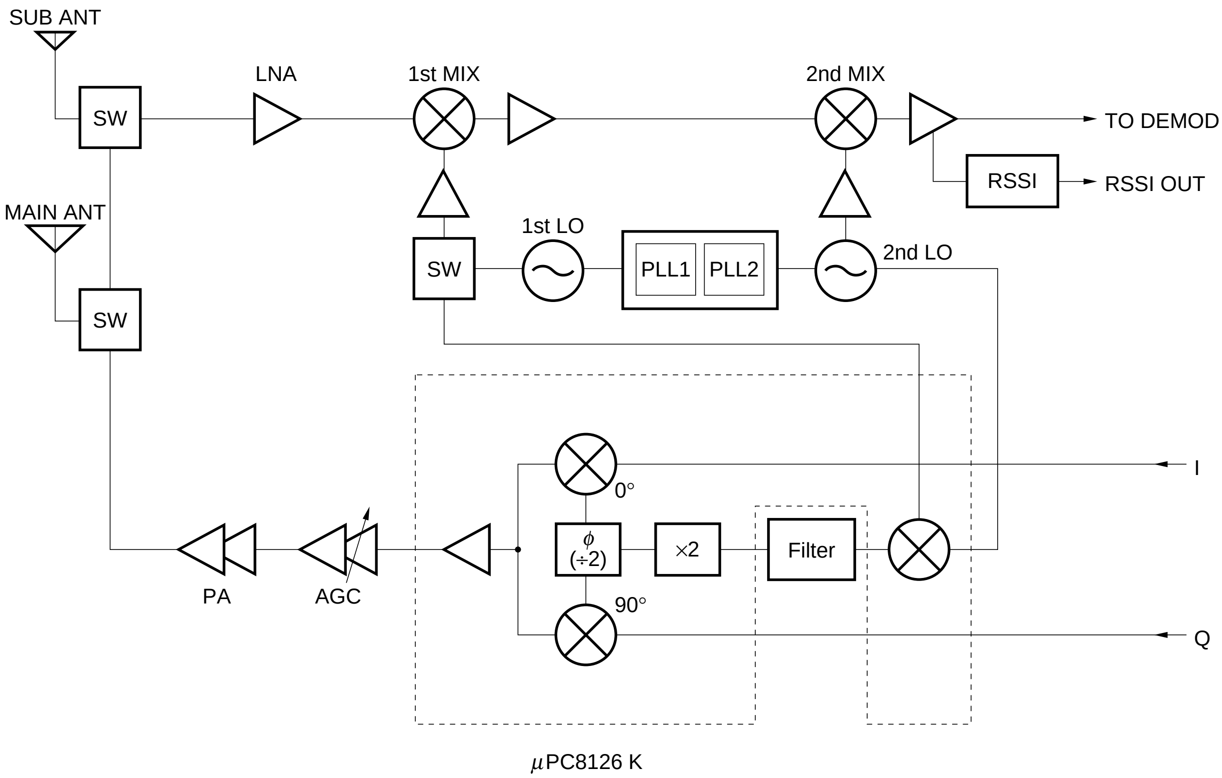


QUADRATURE MODULATOR SERIES PRODUCT

Part Number	Functions	I_{CC} (mA)	f_{LO1in} (MHz)	f_{MODout} (MHz)	Up-Converter f_{RFout} (MHz)	Phase Shifter	Package	Application
μPC8101GR	150 MHz Quad.Mod	15/@2.7 V	100 to 300	50 to 150	External	F/F	20-pin SSOP (225 mil)	CT-2 etc.
μPC8104GR	RF Up-Converter + IF Quad.Mod	28/@3.0 V	100 to 400		900 to 1 900	Doubler + F/F		Digital Comm.
μPC8105GR	400 MHz Quad.Mod	16/@3.0 V	100 to 400		External		16-pin SSOP (225 mil)	
μPC8110GR	1 GHz Direct Quad.Mod	24/@3.0 V	800 to 1 000		Direct		20-pin SSOP (225 mil)	PDC800 MHz, etc.
μPC8125GR	RF Up-Converter + IF Quad.Mod + AGC	36/@3.0 V	220 to 270		1 800 to 2 000			PHS
μPC8126GR	900 MHz Direct Quad.Mod with Offset-Mixer	35/@3.0 V	915 to 960		915 to 960 (LO pre-mixer)			PDC800 MHz
μPC8126K			889 to 960		889 to 960		28-pin QFN	
μPC8129GR	×2LO IF Quad. Mod+RF Up-Converter	28/@3.0 V	200 to 800	100 to 400	800 to 1 900	F/F	20-pin SSOP (225 mil)	GSM, DCS1800, etc.
μPC8139GR-7JH	Transceiver IC (1.9 GHz Indirect Quad. Mod + RX-IF + IF VCO)	TX: 32.5 RX: 4.8 /@3.0 V	220 to 270		1 800 to 2 000	CR	30-pin TSSOP (225 mil)	PHS
μPC8158K	RF Up-Converter + IF Quad.Mod + AGC	28/@3.0 V	100 to 300		800 to 1 500		28-pin QFN	PDC800 M/1.5 G

Remark For outline of the quadrature modulator series, please refer to the application note **Usage of μPC8101, 8104, 8105, 8125, 8129 (Document No. P13251E)** and so on.

APPLICATION EXAMPLE
[PDC800 MHz]



This block diagram presents the IC’s location example applied in the system. The system block construction herein is an example.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Voltage	V_{CC}	T_A = +25 °C	4.0	V
Power Save Control Voltage	V_{PS}	T_A = +25 °C	4.0	V
Power Dissipation	P_D	T_A = +85 °C Note	430	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

Note Mounted on a 50 × 50 × 1.6 mm double sided copper clad epoxy glass PWB.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.6	V
Operating Ambient Temperature	T_A		–25	+25	+75	°C
Pre-Mix. RF Input Frequency	f_{RFin}		689	–	1 200	MHz
Pre-Mix. RF Input Power	P_{RFin}		–13	–11	–9	dBm
Pre-Mix. IF Input Frequency	f_{IFin}	P (f_{IF} × 7) ≤ –65 dBc	120	135	270	MHz
Pre-Mix. IF Input Power	P_{IFin}		–14	–12	–10	dBm
Pre-Mix. Output Frequency (Modulator Output Frequency, Modulator LO Input Frequency)	f_{MIXout} (f_{MODout}, f_{LOin})	f_{IFin} = 200 MHz	889	–	898	MHz
		f_{IFin} = 135 MHz	915	–	960	MHz
Modulator LO Input Power	P_{LOin}		–21.5	–18.5	–15.5	dBm
I/Q Input Frequency	$f_{I/Qin}$		DC	–	10	MHz
I/Q Input Amplitude	$V_{I/Qin}$	Single ended Input	–	–	500	mV_{P-P}
		Differential Input	–	–	250	

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, $V_{CC}1$ = $V_{CC}2$ = $V_{CC}3$ = 3.0 V, $V_{PS}1$, $V_{PS}2$ ≥ 2.2 V unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
MODULATOR + PRE-MIXER TOTAL (TEST CIRCUIT 1 unless otherwise specified)						
Total Circuit Current	I_{CC} (TOTAL)	No Input Signals	24	35	44	mA
Total Circuit Current at Sleep Mode	$I_{CC\ (PS)}$ TOTAL	V_{PS} ≤ 0.5 V (Low), No Input Signals	–	0	15	μA
Modulator Output Power	P_{MODout}	f_{IFin} = 135 MHz, P_{IFin} = –12 dBm f_{RFin} = 813 MHz, P_{RFin} = –11 dBm f_{MODout} = 948 MHz + $f_{I/Q}$ $f_{I/Qin}$ = 2.625 kHz $V_{I/Qin}$ = 500 mV_{P-P} (Single ended) I/Q (DC) = Ib/Qb (DC) = V_{CC}/2 Data Rate: 42 kbps, RNYQ: α = 0.5 MOD Pattern: All Zero	–12	–9	–6	dBm
Local Oscillator Leakage	LOL[Note]		–	–35	–30	dBc
Image Rejection	ImR		–	–40	–30	dBc
I/Q 3rd Order Intermodulation	$IM_{3\ (I/Q)}$		–	–45	–30	dBc
f_{IF-LO} × 7 Harmonics	P (f_{IF} × 7)		–	–	–65	dBc
Power Save Response Time: Rise Time	T_{PS} (RISE)	V_{PS}: Low to High, TEST CIRCUIT 2	–	3	5	μs
Power Save Response Time: Fall Time	T_{PS} (FALL)	V_{PS}: High to Low, TEST CIRCUIT 2	–	3	5	μs
Error Vector Magnitude	EVM	f_{IFin} = 135 MHz, P_{IFin} = –12 dBm f_{RFin} = 813 MHz, P_{RFin} = –11 dBm f_{MODout} = 948 MHz + $f_{I/Q}$ $f_{I/Qin}$ = 2.625 kHz $V_{I/Qin}$ = 500 mV_{P-P} (Single ended) I/Q (DC) = Ib/Qb (DC) = V_{CC}/2 Data Rate: 42 kbps, RNYQ: α = 0.5 MOD Pattern: PN9 (Pseudo-random pattern)	–	1.6	3.5	%rms
Adjacent Channel Power	ACP (Δf = ±50 kHz)		–	–65	–60	dBc
Port Current-7 pin	I_{PS} (7 pin)	No Input Signals	–	–	620	μA
Port Current-17 pin	I_{PS} (17 pin)	No Input Signals	–	–	400	μA

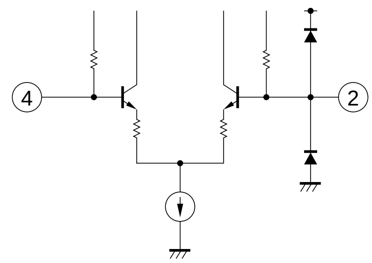
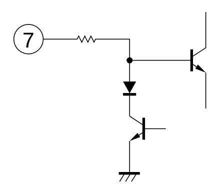
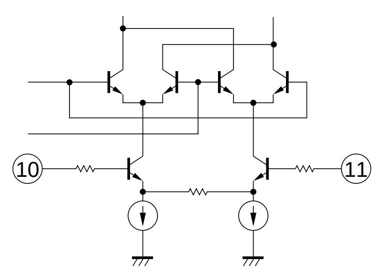
Note f_{LOL} = f_{IFin} + f_{RFin}

STANDARD CHARACTERISTICS FOR REFERENCE

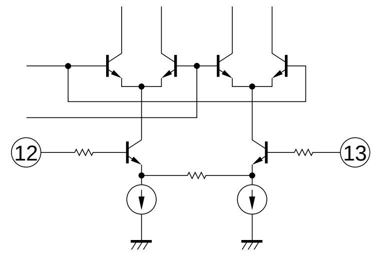
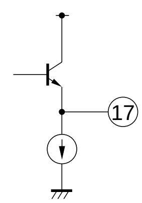
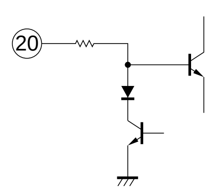
(T_A = +25°C, $V_{CC}1$ = $V_{CC}2$ = $V_{CC}3$ = 3.0 V, $V_{PS}1$, $V_{PS}2$ ≥ 2.2 V unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
MODULATOR (TEST CIRCUIT 3)						
Modulator Circuit Current	I_{CC} (MOD)	No Input Signals	–	27.5	34	mA
Modulator Circuit Current at Sleep Mode	$I_{CC\ (PS)}$ (MOD)	V_{PS} ≤ 0.5 V (Low), No Input Signals	–	0	10	μA
Input Impedance I and Q Port	$Z_{I/Qin}$	$f_{I/Q}$ = DC to 10 MHz	90	180	–	kΩ
Modulator Output Port VSWR	VSWR (MOD)	f_{MODout} = 948 MHz	–	1.5:1	–	–
PRE-MIXER (TEST CIRCUIT 4)						
Pre-Mixer Circuit Current	I_{CC} (MIX)	No Input Signals	–	7.5	10	mA
Pre-Mixer Circuit Current at Sleep Mode	$I_{CC\ (PS)}$ (MIX)	V_{PS} ≤ 0.5 V (Low), No Input Signals	–	0	5	μA
Pre-Mixer Conversion Gain	CG (MIX)	f_{RFin} = 813 MHz, P_{RFin} = –11 dBm, f_{IFin} = 135 MHz, P_{IFin} = –12 dBm, f_{MIXout} = 948 MHz	–5	–3	–1	dB
Pre-Mixer Output Power	P_{out} (MIX)		–17	–15	–13	dBm

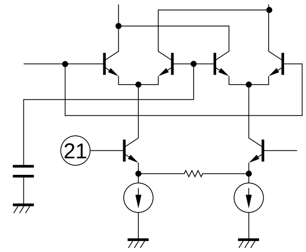
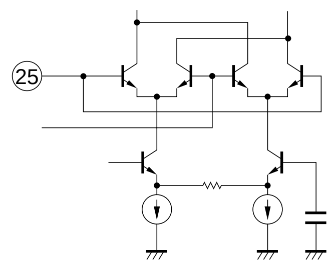
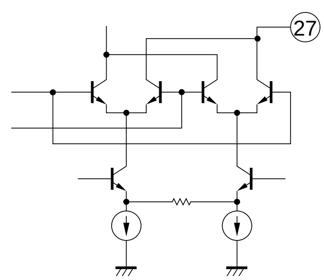
PIN EXPLANATIONS

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage (V)</th><th>Pin Voltage (V) @3 V</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>2</td><td>LOinb</td><td>–</td><td>2.6</td><td>Bypass of LO input for modulator.
This pin should be externally grounded through around 33 pF capacitor.</td><td rowspan="2"></td></tr>
<tr><td>4</td><td>LOin</td><td>–</td><td>2.6</td><td>LO input for the phase shifter.
Connect around 300 Ω between pin 4 and 5 to match to 50 Ω by LC.</td></tr>
<tr><td>6</td><td>V_{CC}2</td><td>2.7 to 3.6</td><td>–</td><td>Supply voltage pin for the phase shifter and IQ Mixer. An internal regulator helps keep the device stable against temperature or V_{CC} variation.</td><td>――――</td></tr>
<tr><td>7</td><td>V_{PS}1
(Modulator)</td><td>V_{PS}</td><td>–</td><td>Power save control pin for the modulator can control On/Sleep state with bias as follows.<table><tr><th>V_{PS} (V)</th><th>State</th></tr><tr><td>2.2 to 3.6</td><td>ON (Active Mode)</td></tr><tr><td>0 to 0.5</td><td>OFF (Sleep Mode)</td></tr></table></td><td></td></tr>
<tr><td>9</td><td>GND
(Modulator)</td><td>0</td><td>–</td><td>Ground pin for the modulator.
Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td>――――</td></tr>
<tr><td>10</td><td>I</td><td>V_{CC}/2</td><td>–</td><td>Input for I signal.
This input impedance is 180 kΩ.
In case of that I/Q input signals are single ended, amplitude of the signal is 500 mV_{P-P} max. Note</td><td rowspan="2"></td></tr>
<tr><td>11</td><td>Ib</td><td>V_{CC}/2</td><td>–</td><td>Input for I signal.
This input impedance is 180 kΩ.
In case of that I/Q input signals are single ended, V_{CC}/2 biased DC signal should be input.
In case of that I/Q input signals are differential, amplitude of the signal is 250 m V_{P-P} max. Note</td></tr>
</table>

Note Relations between amplitude and V_{CC}/2 bias of input signal are following.

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage (V)</th><th>Pin Voltage (V) @3 V</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>12</td><td>Qb</td><td>$V_{CC}/2$</td><td>–</td><td>Input for Q signal.
This input impedance is 180 kΩ.
In case of that I/Q input signals are single ended, $V_{CC}/2$ biased DC signal should be input.
In case of that I/Q input signals are differential, amplitude of the signal is 250 mV_{P-P} max. Note</td><td rowspan="2"></td></tr>
<tr><td>13</td><td>Q</td><td>$V_{CC}/2$</td><td>–</td><td>Input for Q signal.
This input impedance is 180 kΩ.
In case of that I/Q input signals are single ended, amplitude of the signal is 500 mV_{P-P} max. Note</td></tr>
<tr><td>14</td><td>GND (Modulator)</td><td>0</td><td>–</td><td>Ground pin for the modulator.
Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td>——</td></tr>
<tr><td>16</td><td>$V_{CC}3$</td><td>2.7 to 3.6</td><td>–</td><td>Supply voltage pin for the output buffer amplifier of modulator.
An internal regulator helps keep the device stable against temperature or V_{CC} variation.</td><td>——</td></tr>
<tr><td>17</td><td>MODout</td><td>–</td><td>1.6</td><td>Output pin from the modulator.
This is emitter follower output.
So this output impedance is low.</td><td></td></tr>
<tr><td>19</td><td>GND (Modulator)</td><td>0</td><td>–</td><td>Ground pin for the modulator.
Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td>——</td></tr>
<tr><td>20</td><td>$V_{PS}2$ (Pre-Mix)</td><td>V_{PS}</td><td>–</td><td>Power save control pin can control the On/Sleep state with bias as follows.<table><tr><th>V_{PS} (V)</th><th>State</th></tr><tr><td>2.2 to 3.6</td><td>ON (Active Mode)</td></tr><tr><td>0 to 0.5</td><td>OFF (Sleep Mode)</td></tr></table></td><td></td></tr>
</table>

Note Relations between amplitude and $V_{CC}/2$ bias of input signal are following.

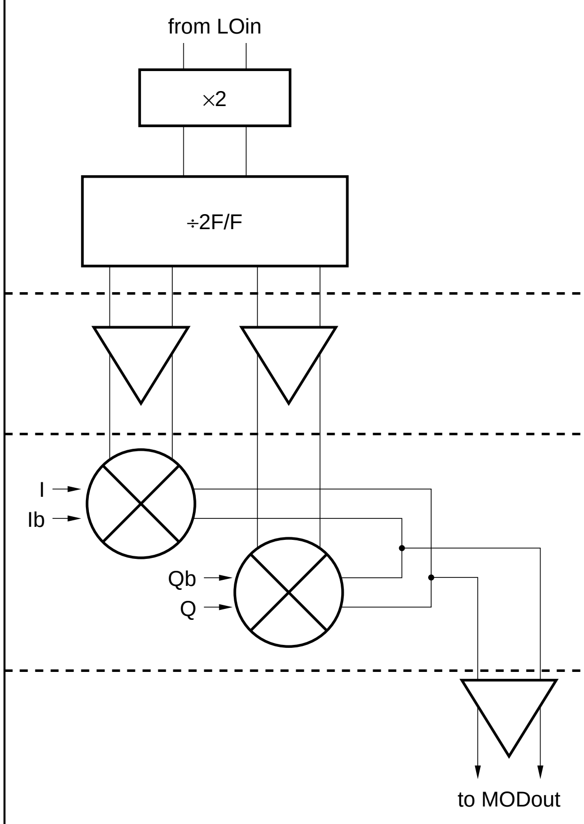
Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V) @3 V	Description	Equivalent Circuit
21	IF-LOin	–	1.3	IF input pin for the Pre-Mixer. This pin is biased internally. Capacitor should be connected in series, and grounded through 51 Ω.	
24	GND (Pre-Mix)	0	–	Ground pin for Pre-Mixer. Connect to the ground with minimum inductance. Track length should be kept as short as possible.	—
25	RF-LOin	–	2.3	RF input pin for the Pre-Mixer. This pin is biased internally. Capacitor should be connected in series, and grounded through 51 Ω.	
26	$V_{CC}1$ (Pre-Mix)	2.7 to 3.6	–	Supply voltage pin for the Pre-Mixer. An internal regulator helps keep the device stable against temperature or V_{CC} variation.	—
27	Pre-Mixout	2.7 to 3.6	–	Output from the Pre-Mixer. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.	
28	GND (Modulator)	0	–	Ground pin for the modulator. Connect to the ground with minimum inductance. Track length should be kept as short as possible.	—
1, 3, 5, 8, 15, 18, 22, 23	N.C.	–	–	Non connection pins.	—

RELATION BETWEEN I/Q PIN INPUT DC VOLTAGE AND AMPLITUDE

Supply Voltage (V) V_{CC}	I/Q DC Voltage (V) $V_{CC}/2$ = I = Ib = Q = Qb	I/Q input signal (mV_{P-P})	
		Single ended input I = Q	Differential input I = Ib = Q = Qb
2.7 to 3.6	1.35 to 1.8	≤ 500	≤ 250

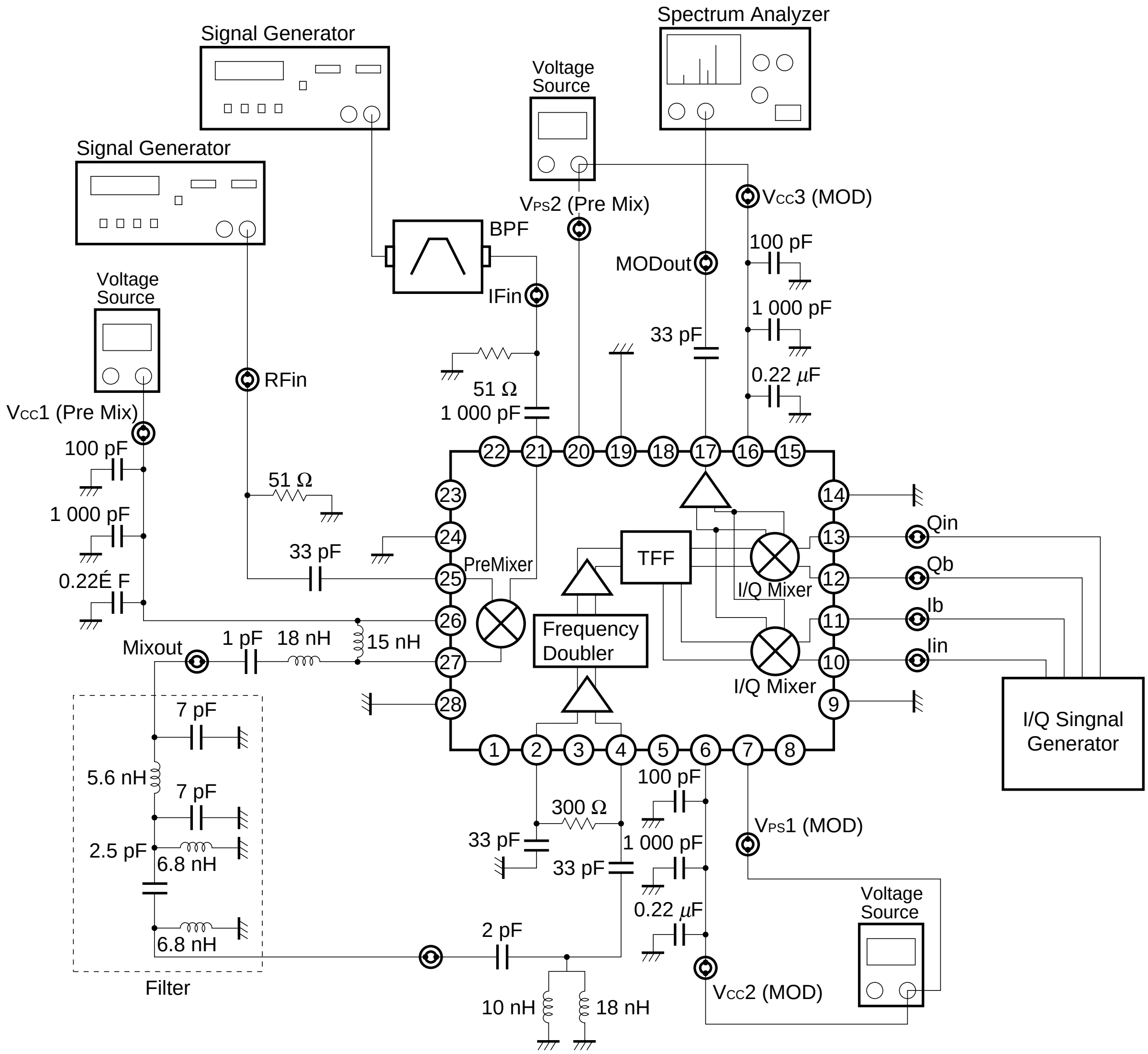
EXPLANATION OF INTERNAL FUNCTION

Block	Function/Operation	Block Diagram
90° PHASE SHIFTER	Input signal from LO is send to digital circuit of T-type flip-flop through frequency doubler. Output signal from T-type F/F is changed to same frequency as LO input and that have quadrature phase shift, 0°, 90 °, 180°, 270°. These circuits have function of self phase correction to make correctly quadrature signals.	
BUFFER AMP.	Buffer amplifiers for each phase signals to send to each mixers.	
MIXER	Each signals from buffer amp. are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to good performance for image rejection.	
ADDER	Output signals from each mixers are added with adder and send to final amplifier.	



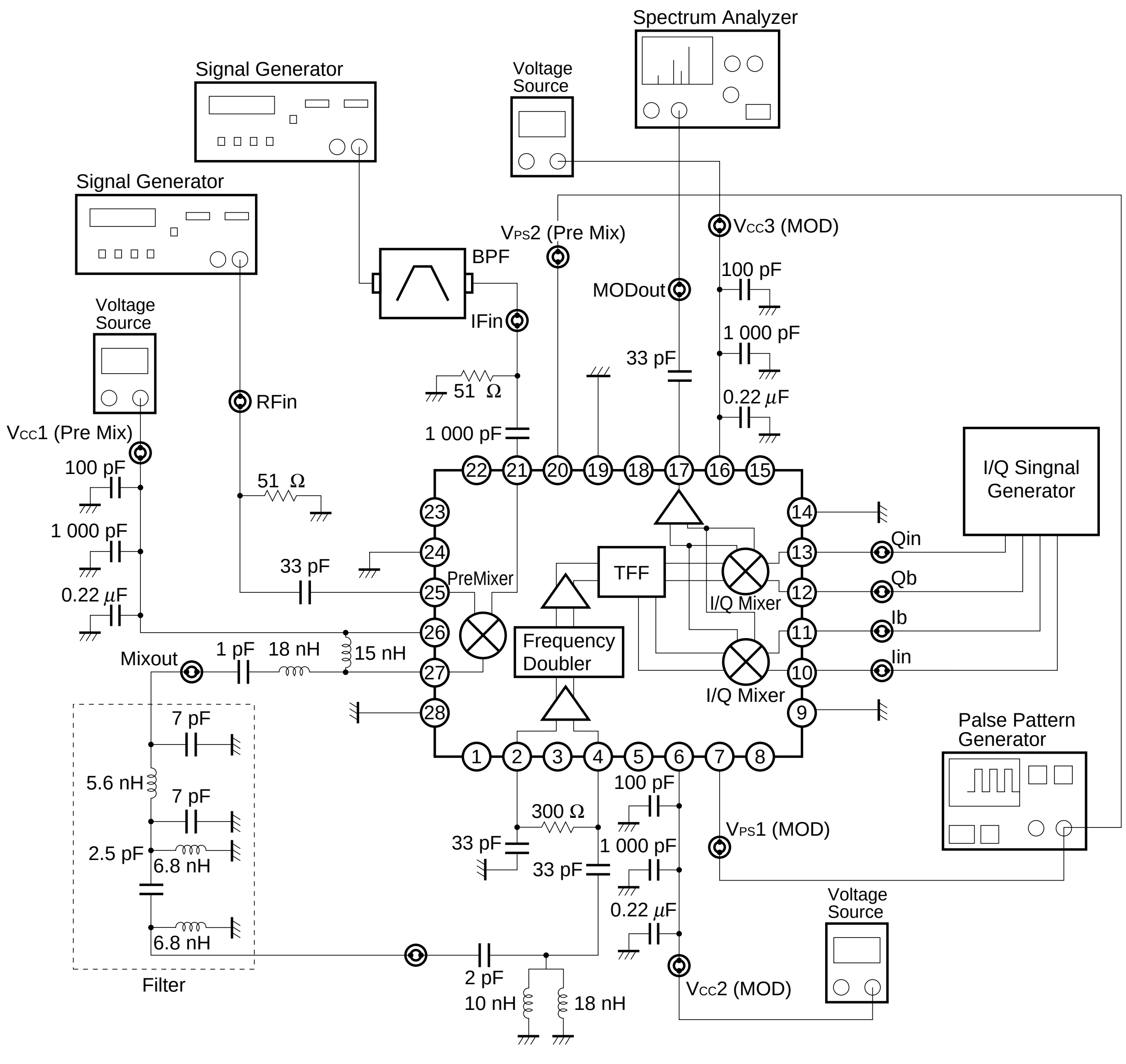
TEST CIRCUIT 1

Pre-mixer + Quadrature modulator (except Power save response time)



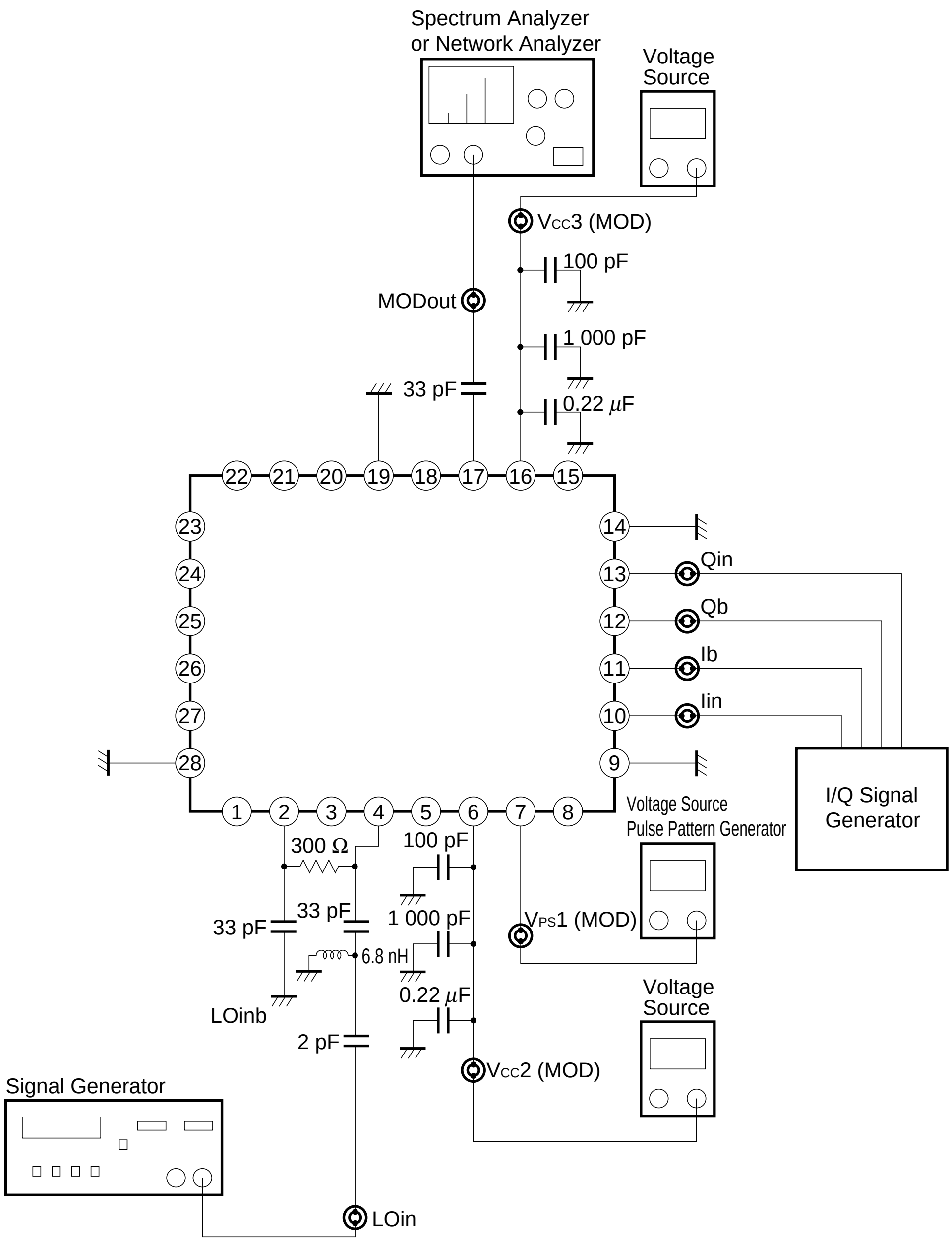
TEST CIRCUIT 2

Pre-mixer + Quadrature modulator (for Power save response time)



TEST CIRCUIT 3

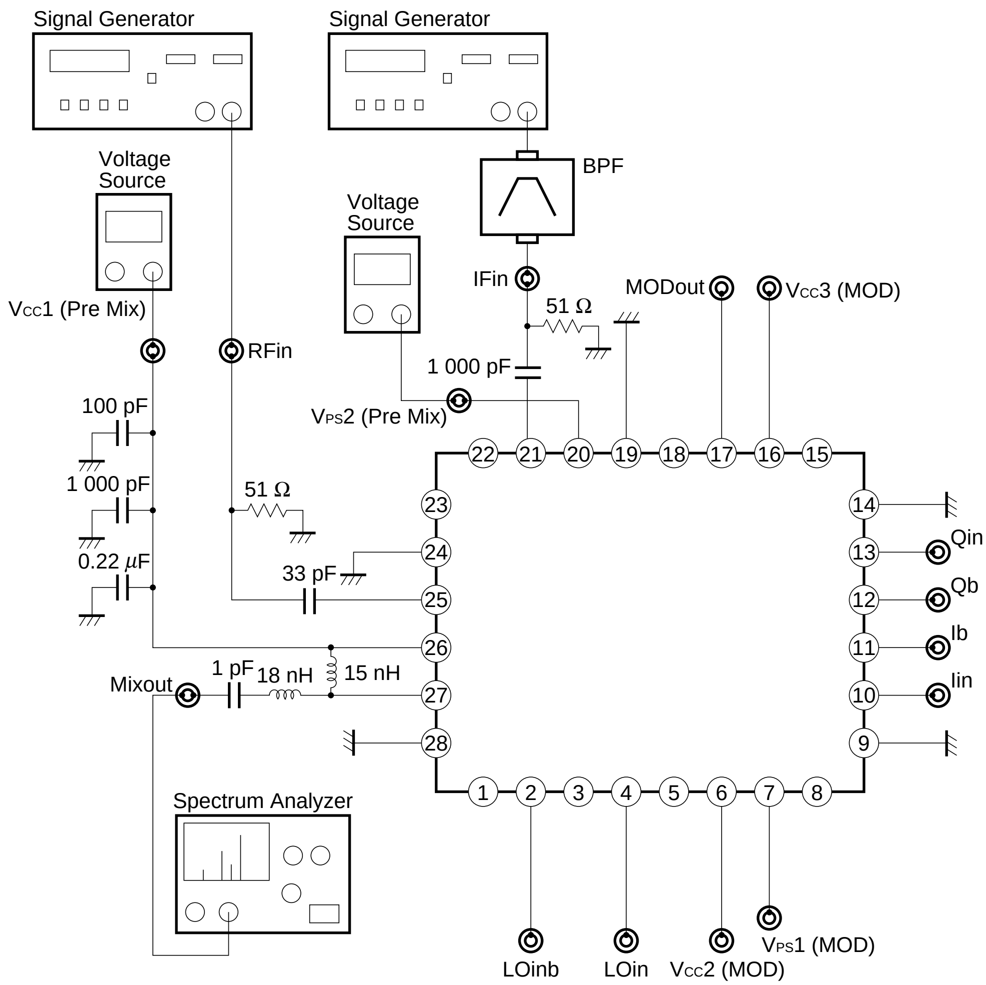
Quadrature modulator block



In this case, pin 20 to 27 should be opened or grounded.

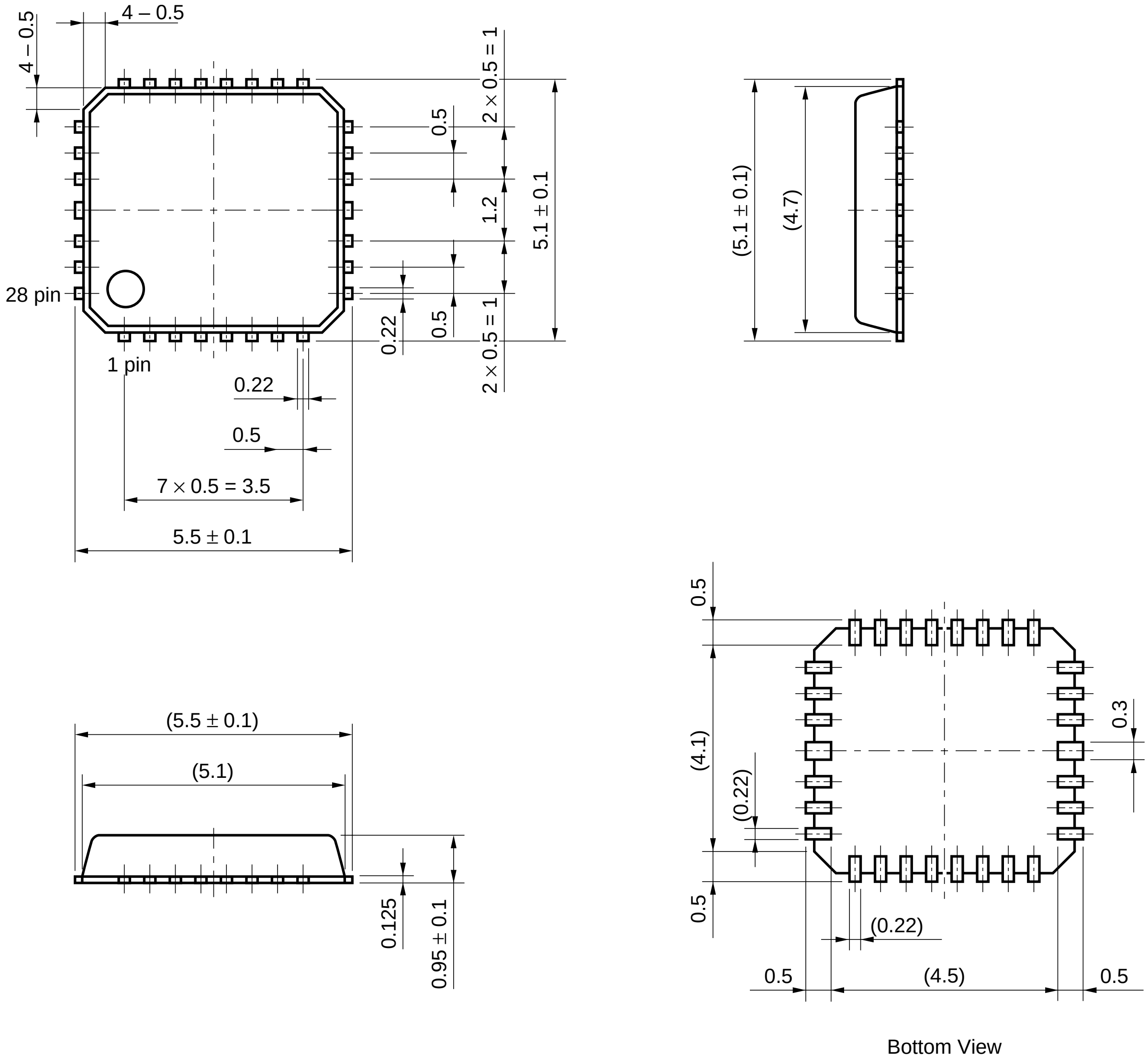
TEST CIRCUIT 4

Pre-mixer block



PACKAGE DIMENSIONS

28 pin plastic QFN (UNIT: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired operation).
(3) Keep the track length between the ground pins as short as possible.
(4) Connect a bypass capacitor (example 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended condition. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 2, Exposure limit[Note]: None	IR35-00-2
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit[Note]: None	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.