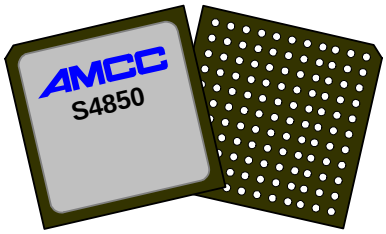

Description

The function of the S4850 clock and data recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S4850 receives an OC-48 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential bit clock and retimed data. Figure 1 shows a typical network application.

The S4850 utilizes two on-chip PLLs which consist of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage.

The S4850 is packaged in a 121 Plastic Ball Grid Array (PBGA), offering designers a small package outline.

Overview

The dual S4850 supports clock recovery for the OC-48 (+ FEC) data rates. The differential serial data is input to the chip and clock recovery is performed on the incoming data stream. An external reference clock is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S4850.

The S4850 is divided into two independent clock recovery modules.

Individual channel power off capability.

Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation.

Suggested Interface Device

- SONET/SDH OC-192/4xOC-48 Framer/ Pointer Processor
- FPGAs
- ASIC
- SERDES without CDR

Applications

- SONET/SDH/ATM/OC-48 with FEC rate Support
- SONET/SDH modules
- SONET/SDH test equipment
- Repeaters

– At a Glance –

Features

- CMOS 0.13 micron technology
- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports clock recovery for 2.488 Gbps (OC-48) with FEC
- Selectable reference clock source (155.52 MHz for SONET or equivalent for FEC)
- Directly compatible with 1.2 V CML I/O
- 1.2 V, 3.3 V, 2.5 V and 1.8 V supply
- Lock detect
- Signal detect input (SD[B:A])
- Bypass Mode
- Individual channel power off capability
- Typical 400 mW
- 121 Plastic Ball Grid Array Package

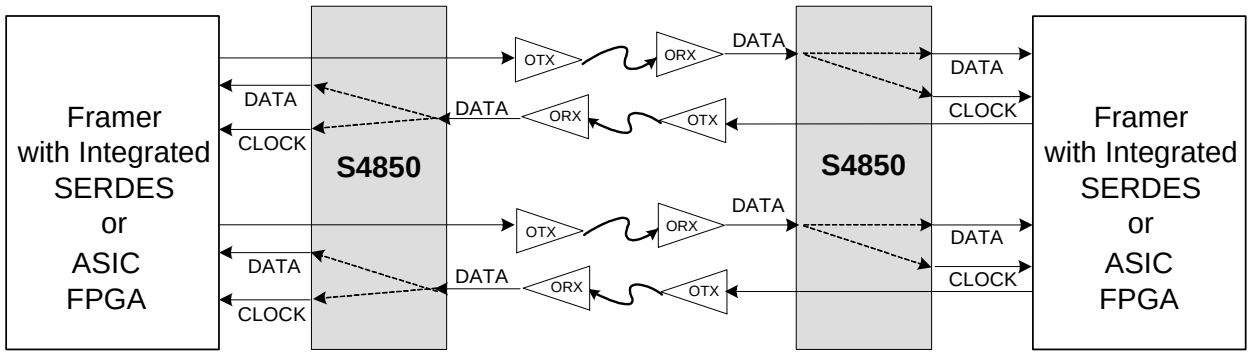

Figure 1. System Block Diagram

Prefix	Device	Package
S - Integrated Circuit	4850	PB -121 PBGA

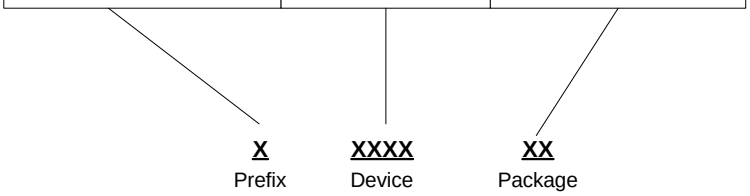

Figure 2. S4850 Ordering Information

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