MC74AC109, MC74ACT109

Dual JK̄ Positive Edge-Triggered Flip-Flop

The MC74AC109/74ACT109 consists of two high–speed completely independent transition clocked JK flip–flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip–flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and K inputs together.

Asynchronous Inputs:

       LOW input to $\overline{S_D}$ (Set) sets Q to HIGH level
       LOW input to $\overline{C_D}$ (Clear) sets Q to LOW level
       Clear and Set are independent of clock
       Simultaneous LOW on $\overline{C_D}$ and $\overline{S_D}$ makes both Q and $\overline{Q}$ HIGH

- Outputs Source/Sink 24 mA
- ′ACT109 Has TTL Compatible Inputs
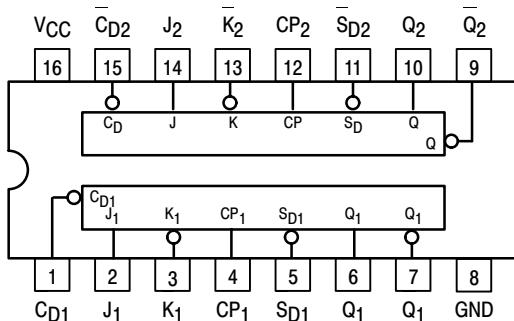
**Figure 1. Pinout; 16–Lead Packages Conductors**
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
J_1, J_2, K_1, K_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
C_{D1}, C_{D2}	Direct Clear Inputs
S_{D1}, S_{D2}	Direct Set Inputs
Q_1, Q_2, $\overline{Q_1}$, $\overline{Q_2}$	Outputs
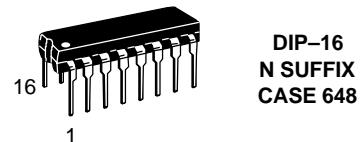
DIP–16
N SUFFIX
CASE 648
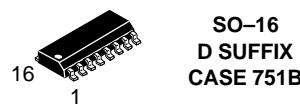
SO–16
D SUFFIX
CASE 751B

TSSOP–16
DT SUFFIX
CASE 948F

EIAJ–16
M SUFFIX
CASE 966

ORDERING INFORMATION

Device	Package	Shipping
MC74AC109N	PDIP–16	25 Units/Rail
MC74ACT109N	PDIP–16	25 Units/Rail
MC74AC109D	SOIC–16	48 Units/Rail
MC74ACT109D	SOIC–16	48 Units/Rail
MC74AC109DR2	SOIC–16	2500 Tape & Reel
MC74ACT109DR2	SOIC–16	2500 Tape & Reel
MC74AC109DT	TSSOP–16	96 Units/Rail
MC74ACT109DT	TSSOP–16	96 Units/Rail
MC74AC109DTR2	TSSOP–16	2500 Tape & Reel
MC74ACT109DTR2	TSSOP–16	2500 Tape & Reel
MC74AC109M	EIAJ–16	50 Units/Rail
MC74ACT109M	EIAJ–16	50 Units/Rail
MC74AC109MEL	EIAJ–16	2000 Tape & Reel
MC74ACT109MEL	EIAJ–16	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

MC74AC109, MC74ACT109

TRUTH TABLE

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0-$
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0-$

H = HIGH Voltage Level
L = LOW Voltage Level
⌐ = LOW–to–HIGH Clock Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before
   LOW–to–HIGH Transition of Clock
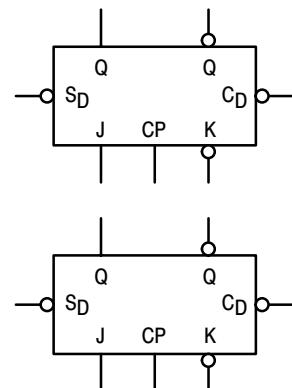
Figure 2. Logic Symbol
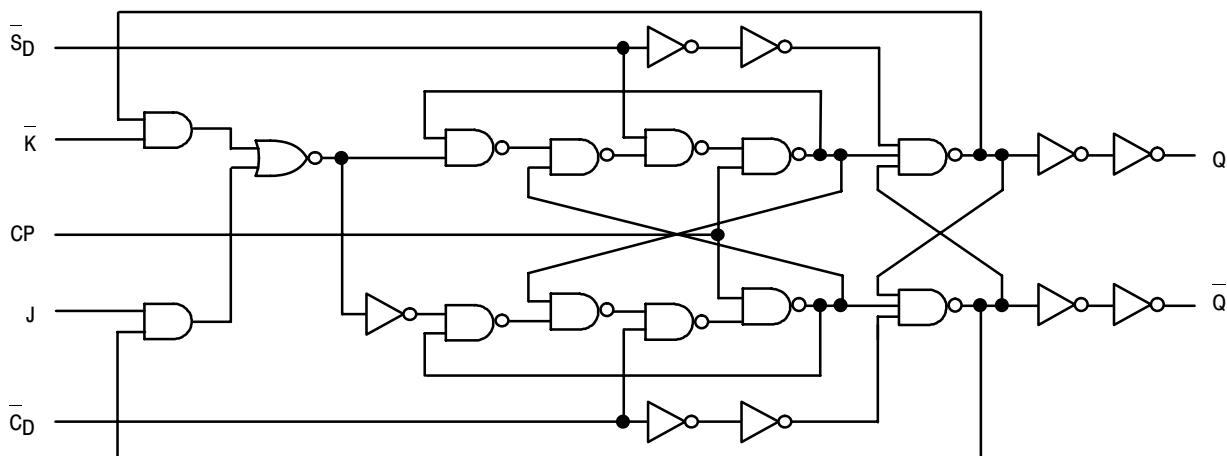
NOTE: This diagram is provided only for the understanding of logic
        operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram
(One Half Shown)

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recom-
  mended Operating Conditions.

MC74AC109, MC74ACT109

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – High		–	–	–24	mA
I_{OL}	Output Current – Low		–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C Typ	74AC T_A = +25°C Guaranteed Limits	74AC T_A = –40°C to +85°C	Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = –50 μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –12 mA –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC109, MC74ACT109

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150	– –	– –	100 125	– –	MHz	3–3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 2.5	– –	13.5 10.0	3.5 2.0	16.0 10.5	ns	3–6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	14.0 10.0	3.0 1.5	14.5 10.5	ns	3–6
t_{PLH}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.5	– –	12.0 9.0	2.5 2.0	13.0 10.0	ns	3–6
t_{PHL}	Propagation Delay $\overline{CD}_n$ or $\overline{S_{Dn}}$ to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	12.0 9.5	3.0 2.0	13.5 10.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Unit	Fig. No.
			Typ	Guaranteed Minimum		
t_S	Set–up Time, HIGH or LOW J_n or K_n to CP_n	3.3 5.0	– –	6.5 4.5	7.5 5.0	ns	3–9
t_h	Hold Time, HIGH or LOW J_n or K_n to CP_n	3.3 5.0	– –	0 0.5	0 0.5	ns	3–9
t_w	Pulse Width CP_n or $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$	3.3 5.0	– –	4.0 3.5	4.5 3.5	ns	3–6
t_{rec}	Recovery TIme $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to CP	3.3 5.0	– –	0 0	0 0	ns	3–9

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$	74ACT $T_A = -40°C$ to $+85°C$	Unit	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50$ μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -24 mA -24 mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

DC CHARACTERISTICS (continued)

Symbol	Parameter	V_CC (V)	74ACT T_A = +25°C		74ACT T_A = −40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	µA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	µA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_CC* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	–	–	125	–	MHz	3–3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	–	11.0	3.5	13.0	ns	3–6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.0	–	10.0	2.5	11.5	ns	3–6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	–	9.5	2.0	10.5	ns	3–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	–	10.0	2.0	11.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_CC* (V)	74ACT T_A = +25°C C_L = 50 pF	74ACT T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum		
t_s	Set–up Time, HIGH or LOW J_n or K_n to CP_n	5.0	–	2.0	2.5	ns	3–9
t_h	Hold Time, HIGH or LOW J_n or K_n to CP_n	5.0	–	2.0	2.0	ns	3–9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	–	5.0	6.0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS (continued)

Symbol	Parameter	V_{CC}*(V)	74ACT $T_A = +25°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Unit	Fig. No.
			Typ	Guaranteed Minimum		
t_{rec}	Recovery TIme C_{Dn} or S_{Dn} to CP	5.0	–	0 0	ns	3–9

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0$ V
C_{PD}	Power Dissipation Capacitance	35	pF	$V_{CC} = 5.0$ V

MARKING DIAGRAMS

DIP–16

MC74AC109N
AWLYYWW

MC74ACT109N
AWLYYWW

SO–16

AC109
AWLYWW

ACT109
AWLYWW

TSSOP–16

AC
109
ALYW

ACT
109
ALYW

EIAJ–16

74AC109
ALYW
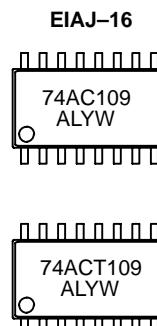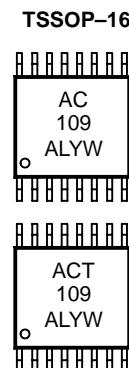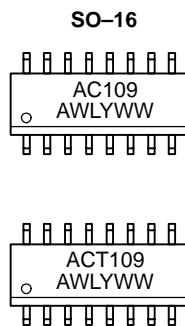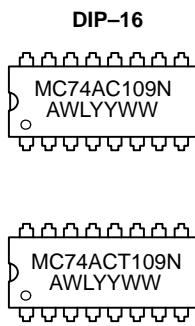
74ACT109
ALYW

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

PDIP–16
N SUFFIX
16 PIN PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R
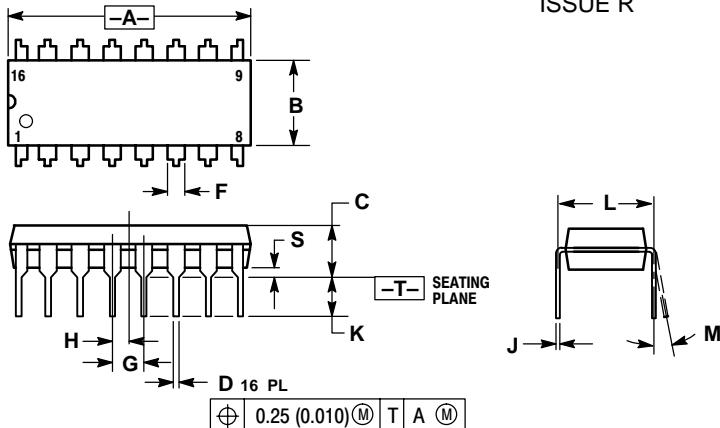
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SO–16
D SUFFIX
16 PIN PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
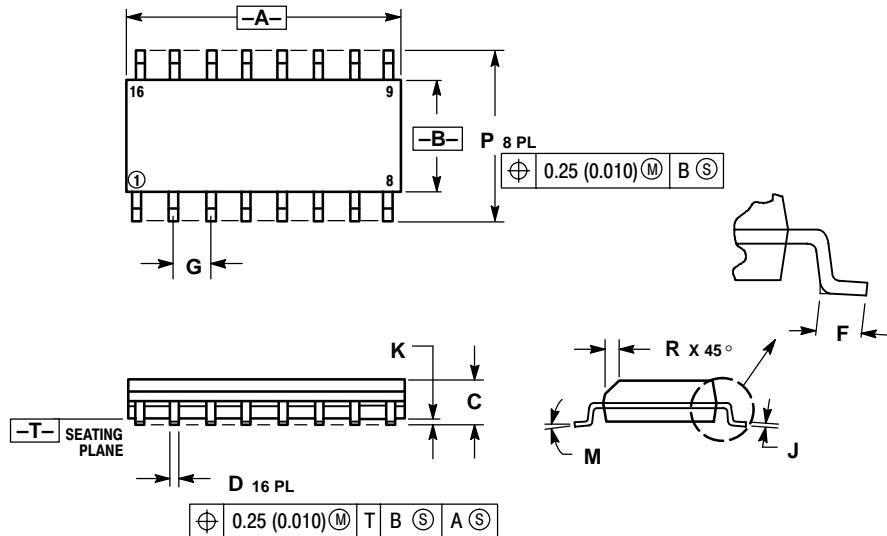
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP–16
DT SUFFIX
16 PIN PLASTIC TSSOP PACKAGE
CASE948F–01
ISSUE O
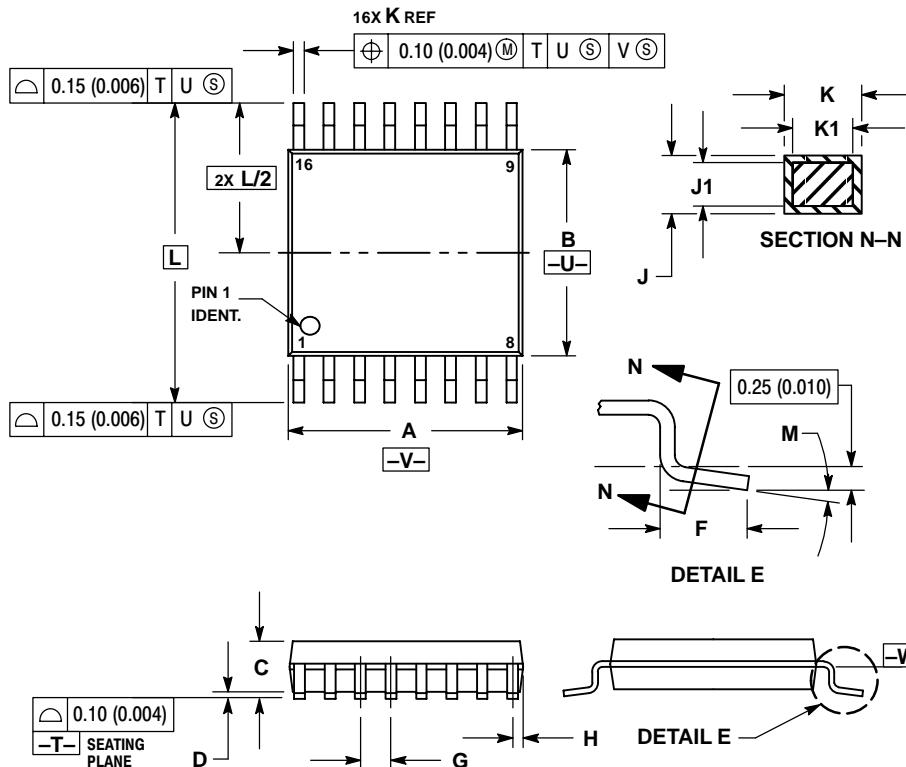
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

EIAJ–16
M SUFFIX
16 PIN PLASTIC EIAJ PACKAGE
CASE966–01
ISSUE O
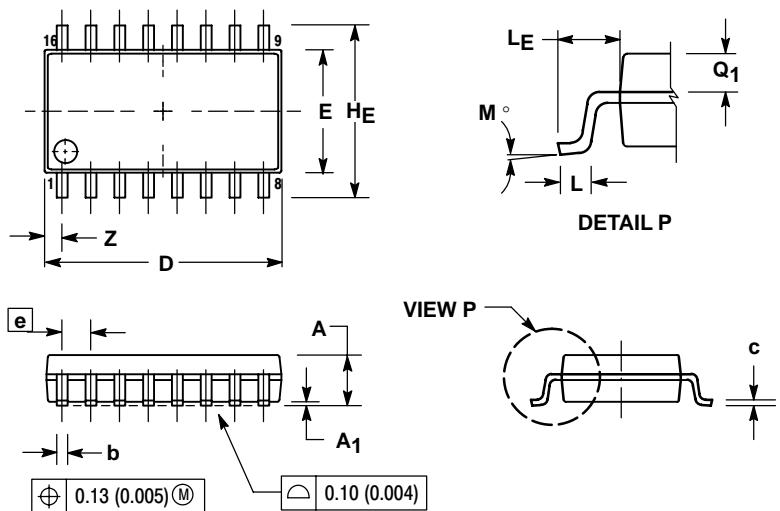
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

Notes

Notes

<u>Notes</u>