To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK1151(L)(S), 2SK1152(L)(S)

Silicon N-Channel MOS FET

ADE-208-1245 (Z)
1st. Edition
Mar. 2001

Application

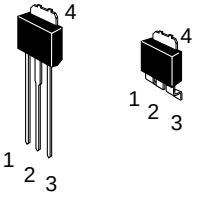
High speed power switching

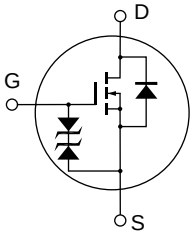
Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

Outline

DPAK-1





1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1151	V_{DSS}	450	V
	2SK1152		500	
Gate to source voltage		V_{GSS}	±30	V
Drain current		I_D	1.5	A
Drain peak current		$I_{D(pulse)}$*[1]	6	A
Body to drain diode reverse drain current		I_{DR}	1.5	A
Channel dissipation		Pch*[2]	20	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	–55 to +150	°C

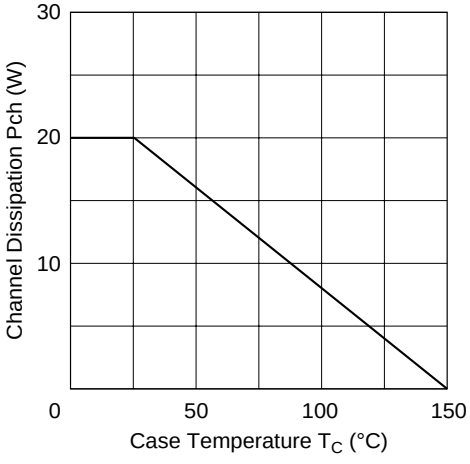
Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at T_C = 25°C

Electrical Characteristics (Ta = 25°C)

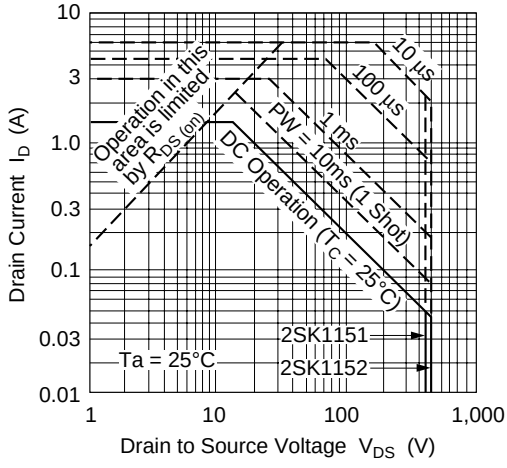
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	2SK1151	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0
	2SK1152		500				
Gate to source breakdown voltage		$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current		I_{GSS}	—	—	±10	µA	V_{GS} = ±25 V, V_{DS} = 0
Zero gate voltage drain current	2SK1151	I_{DSS}	—	—	100	µA	V_{DS} = 360 V, V_{GS} = 0
	2SK1152						V_{DS} = 400 V, V_{GS} = 0
Gate to source cutoff voltage		$V_{GS(off)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Static Drain to source on stateresistance	2SK1151	$R_{DS(on)}$	—	3.5	5.5	Ω	I_D = 1 A, V_{GS} = 10 V *[1]
	2SK1152		—	4.0	6.0		
Forward transfer admittance		|yfs|	0.6	1.1	—	S	I_D = 1 A, V_{DS} = 20 V *[1]
Input capacitance		Ciss	—	160	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance		Coss	—	45	—	pF	
Reverse transfer capacitance		Crss	—	5	—	pF	
Turn-on delay time		$t_{d(on)}$	—	5	—	ns	I_D = 1 A, V_{GS} = 10 V, R_L = 30 Ω
Rise time		t_r	—	10	—	ns	
Turn-off delay time		$t_{d(off)}$	—	20	—	ns	
Fall time		t_f	—	10	—	ns	
Body to drain diode forward voltage		V_{DF}	—	1.0	—	V	I_F = 1.5 A, V_{GS} = 0
Body to drain diode reverse recovery time		t_{rr}	—	220	—	ns	I_F = 1.5 A, V_{GS} = 0, di_F/dt = 100 A/µs

Note: 1. Pulse test

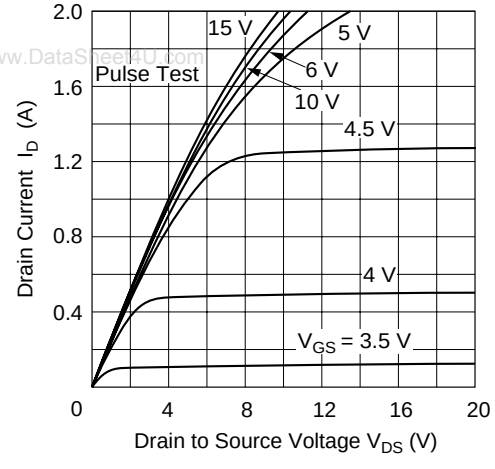
Power vs. Temperature Derating



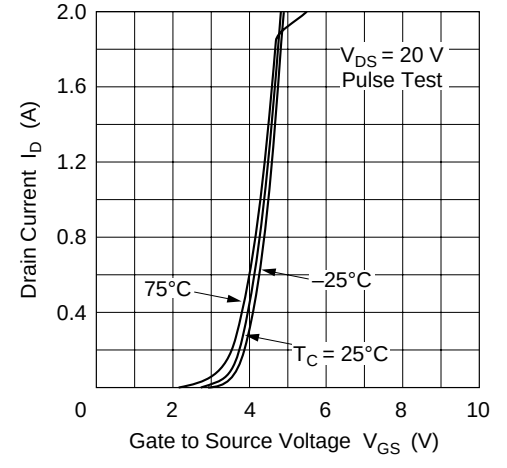
Maximum Safe Operation Area



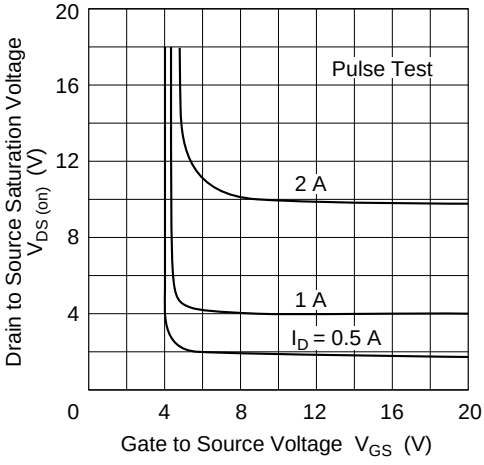
Typical Output Characteristics



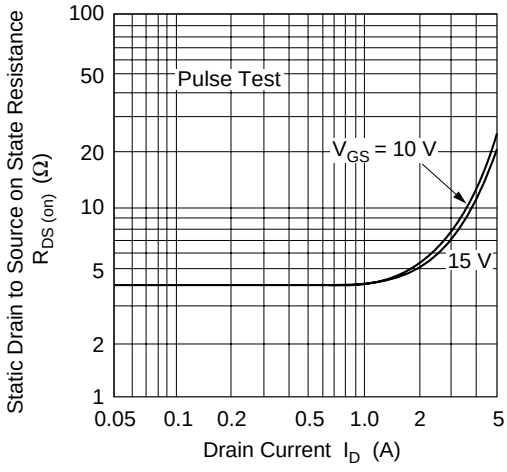
Typical Transfer Characteristics



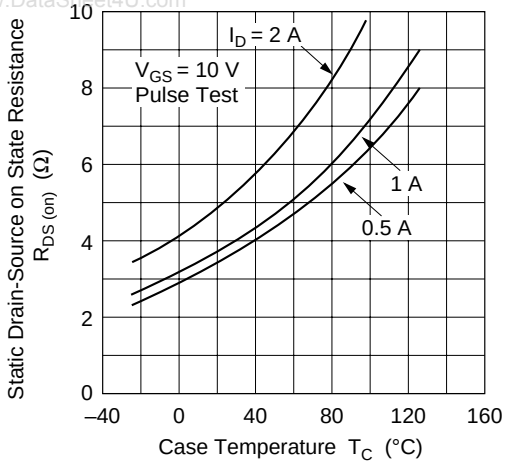
Drain to Source Saturation Voltage vs. Gate to Source Voltage



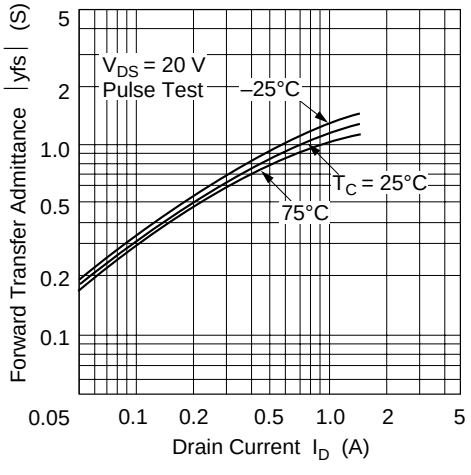
Static Drain to Source on State Resistance vs. Drain Current



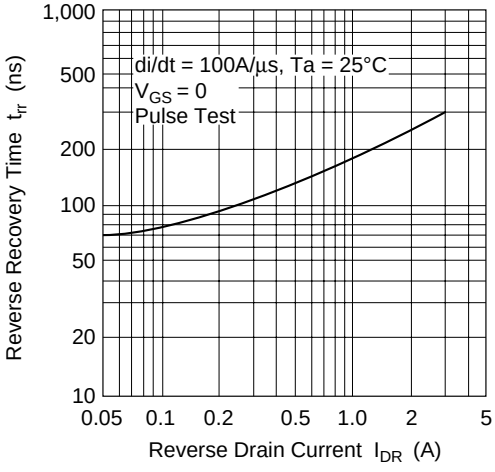
Static Drain to Source on State Resistance vs. Temperature



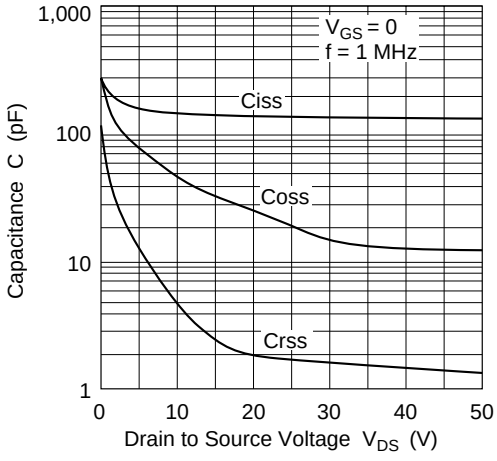
Forward Transfer Admittance vs. Drain Current



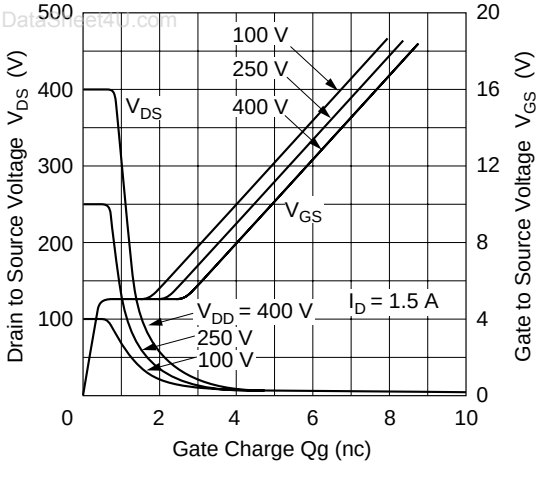
Body to Drain Diode Reverse Recovery Time



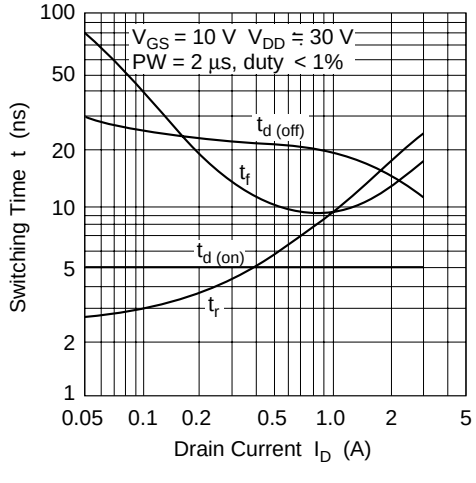
Typical Capacitance vs. Drain to Source Voltage



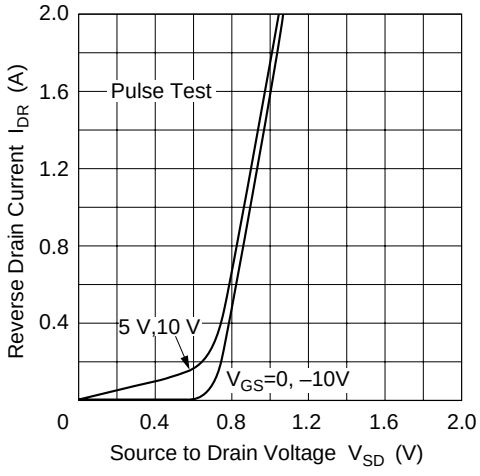
Dynamic Input Characteristics



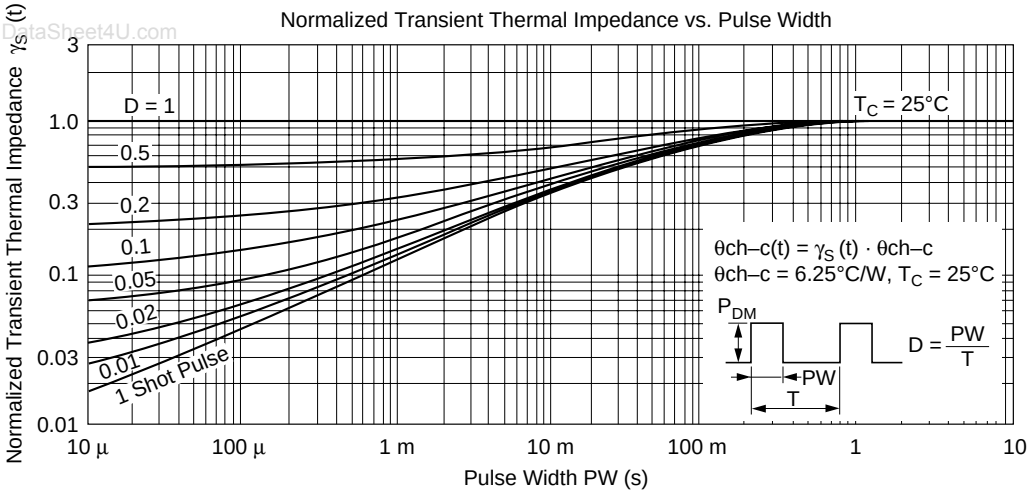
Switching Characteristics



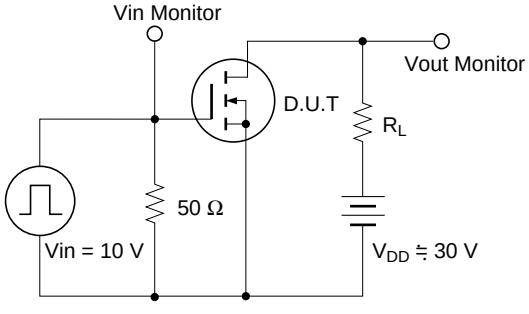
Reverse Drain Current vs.
Source to Drain Voltage



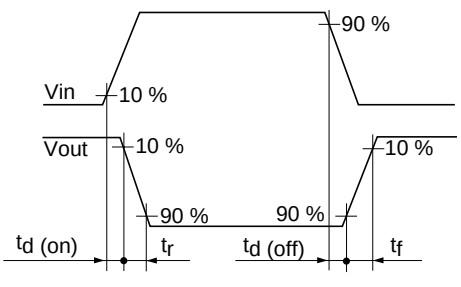
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



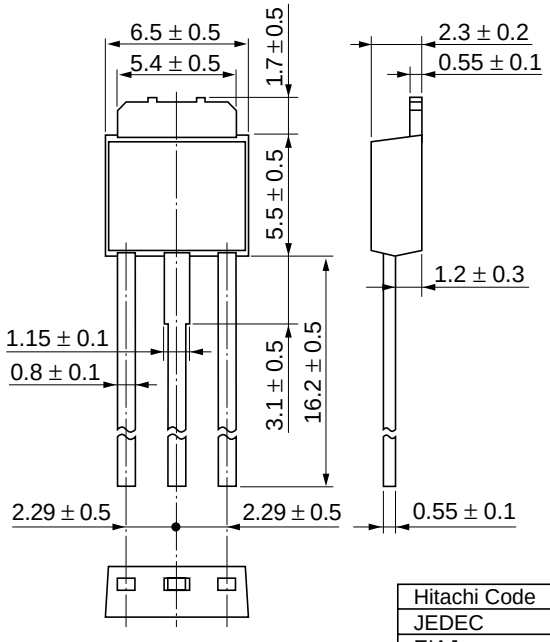
Wavewforms

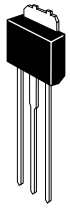


Package Dimensions

As of January, 2001

Unit: mm

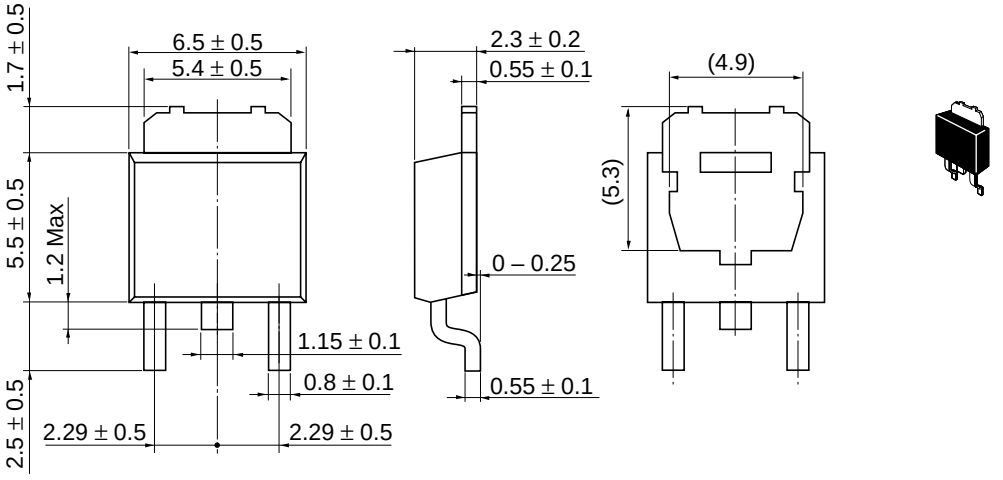




Hitachi Code	DPAK (L)-(1)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.42 g

As of January, 2001

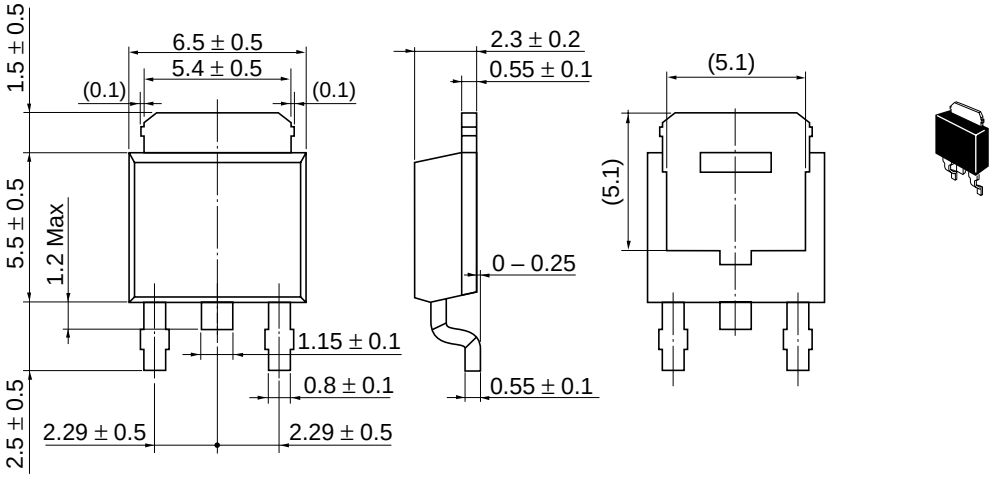
Unit: mm

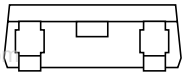


Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001

Unit: mm





Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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