

**Radiation Hardened 3.3V Quad Differential Line Receiver**

The Intersil HS-26CLV32RH is a radiation hardened 3.3V quad differential line receiver designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV32RH has an input sensitivity of 200mV (Typ) over a common mode input voltage range of -4V to +7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. The device has unique inputs that remain high impedance when the receiver is disabled or powered-down, maintaining signal integrity in multi-receiver applications.

**Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.**

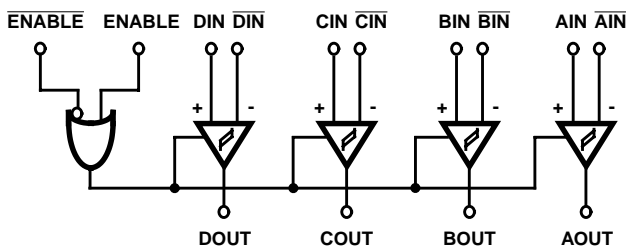
Detailed Electrical Specifications for these devices are contained in SMD 5962-95689. A "hot-link" is provided on our homepage for downloading.

[www.intersil.com/spacedefense/space.asp](http://www.intersil.com/spacedefense/space.asp)

**Ordering Information**

ORDERING NO.	INTERNAL MKT. NO.	TEMP. RANGE (°C)
5962F9568902QEC	HS1-26CLV32RH-8	-55 to 125
5962F9568902QXC	HS9-26CLV32RH-8	-55 to 125
5962F9568902V9A	HS0-26CLV32RH-Q	25
5962F9568902VEC	HS1-26CLV32RH-Q	-55 to 125
5962F9568902VXC	HS9-26CLV32RH-Q	-55 to 125
HS1-26CLV32RH/PROTO	HS1-26CLV32RH/PROTO	-55 to 125
HS9-26CLV32RH/PROTO	HS9-26CLV32RH/PROTO	-55 to 125

**Logic Diagram**

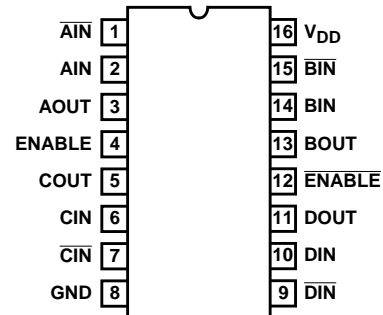


**Features**

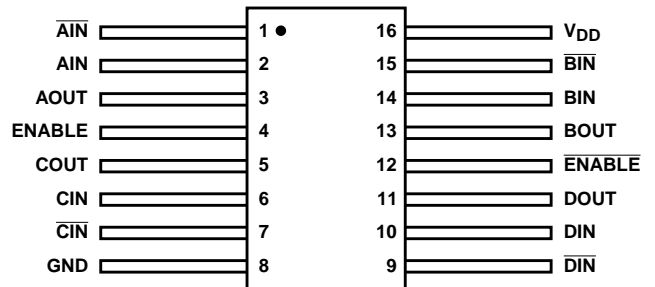
- Electrically Screened to SMD # 5962-95689
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
  - Total Dose . . . . . 300 krad(Si)(Max)
  - Single Event Upset LET . . . . . 100MeV/mg/cm<sup>2</sup>
  - Single Event Latch-up Immune
- Low Stand-by Current. . . . . 13mA(Max)
- Operating Supply Range . . . . . 3.0V to 3.6V
- Enable Input Levels . . . .  $V_{IH} > (.7)(V_{DD})$ ;  $V_{IL} < (.3)(V_{DD})$
- CMOS Output Levels . . . . .  $V_{OH} > 2.55V$ ;  $V_{OL} < 0.4V$
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered-down
- Full -55°C to 125°C Military Temperature Range

**Pinouts**

**HS1-26CLV32RH 16 LEAD CERAMIC SIDEBRAZE DIP  
MIL-STD-1835: CDIP2-T16  
TOP VIEW**



**HS9-26CLV32RH 16 LEAD FLATPACK  
MIL-STD-1835: CDFP4-F16  
TOP VIEW**



# HS-26CLV32RH

## Die Characteristics

### DIE DIMENSIONS:

84 mils x 130 mils x 21 mils  
(2140 $\mu$ m x 3290 $\mu$ m)

### INTERFACE MATERIALS:

#### Glassivation:

Type: PSG (Phosphorus Silicon Glass)  
Thickness: 8k $\text{\AA}$   $\pm$  1k $\text{\AA}$

#### Substrate:

AVLS11RA, Silicon backside, V<sub>DD</sub> backside potential

### Metallization:

Bottom: Mo/Tiw  
Thickness: 5800 $\text{\AA}$   $\pm$  1k $\text{\AA}$   
Top: Al/Si/Cu  
Thickness: 10k $\text{\AA}$   $\pm$  1k $\text{\AA}$

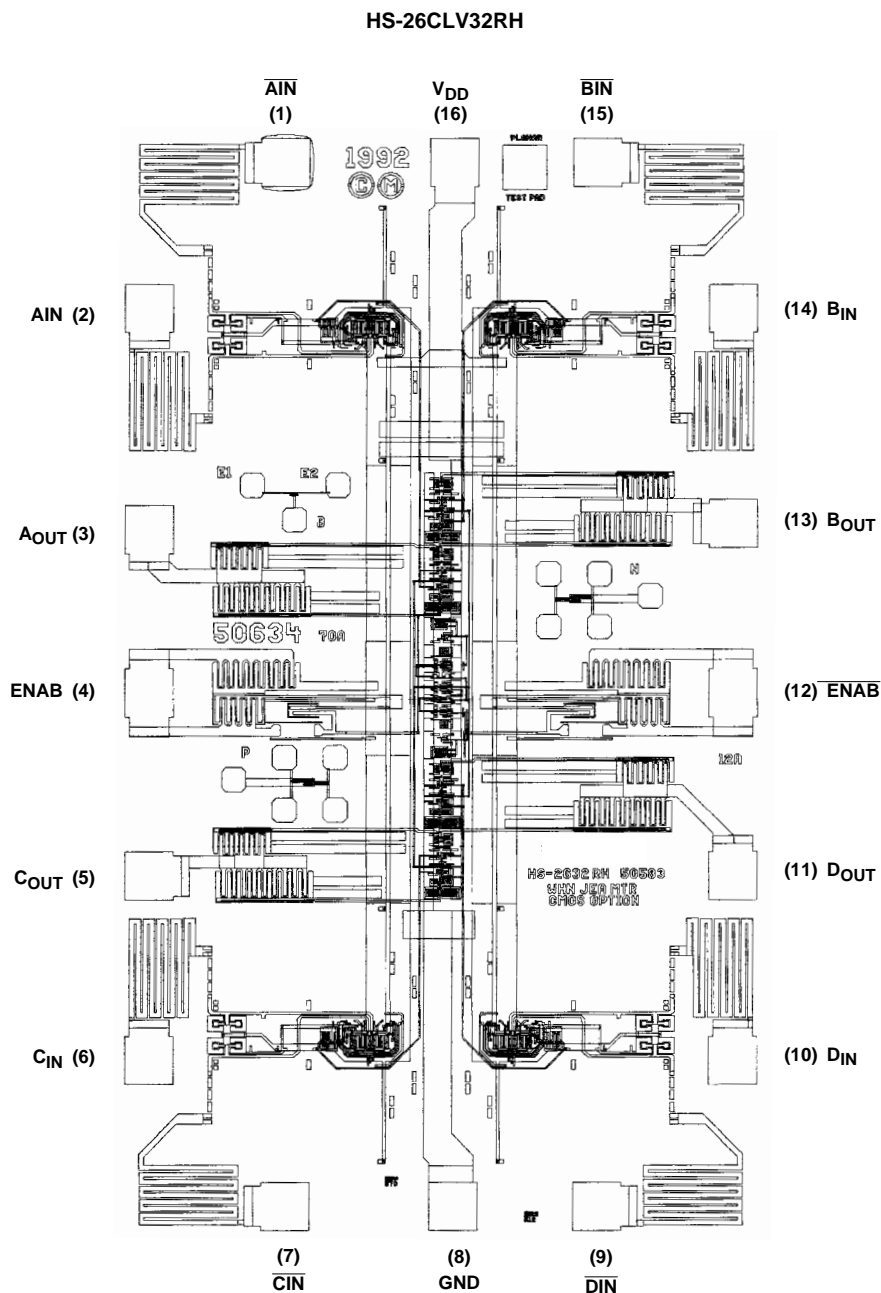
### Worst Case Current Density:

<2.0 x 10<sup>5</sup>A/cm<sup>2</sup>

### Bond Pad Size:

110 $\mu$ m x 100 $\mu$ m

## Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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