T-46-23-12

CY7C132/CY7C136
CY7C142/CY7C146

CYPRESS SEMICONDUCTOR

2048 x 8 Dual-Port Static RAM

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- MASTER CY7C132/CY7C136 easily expands data bus width to 16 or more bits using SLAVE CY7C142/CY7C146
- $\overline{BUSY}$ output flag on CY7C132/CY7C136; $\overline{BUSY}$ input on CY7C142/CY7C146
- $\overline{INT}$ flag for port-to-port communication (52-pin LCC/PLCC versions)

Functional Description

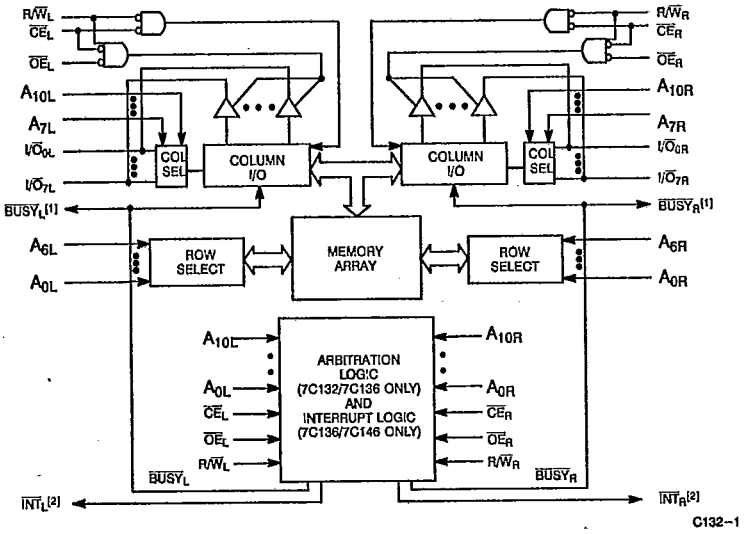
The CY7C132/CY7C136/CY7C142/CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided permitting independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin LCC and PLCC versions. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in both 52-pin LCC and 52-pin PLCC.

Logic Block Diagram



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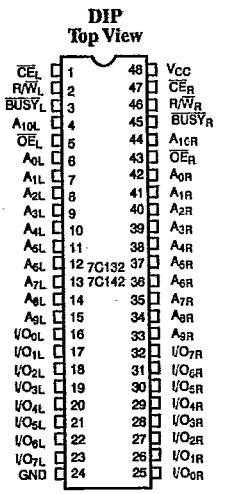
Pin Configuration



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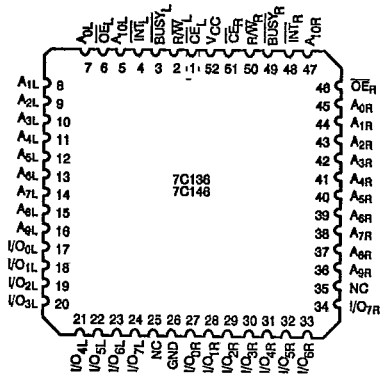
Notes:
1. CY7C132/CY7C136 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C142/CY7C146 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs; pull-up resistor required.

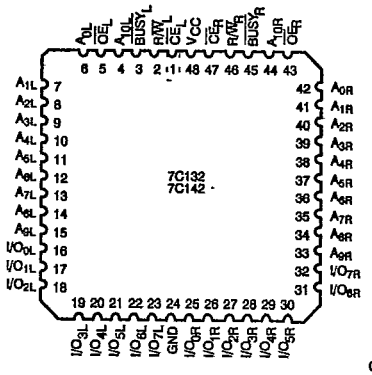
Pin Configurations (continued)

52-Pin LCC/PLCC
Top View



C132-3

48-Pin LCC
Top View



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Selection Guide

		7C132-25[3] 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available in LCC and PLCC packages only.

4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C13225,30[3] 7C136-25,30 7C142-25,30 7C146-25,30		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45,55 7C136-45,55 7C142-45,55 7C146-45,55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[7]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[6]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[6]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V or $V_{IN} \le$ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		105		85		70	mA
			Mil				105		85	

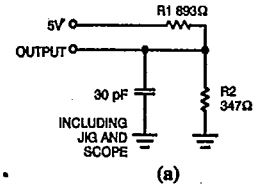
Capacitance[9]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

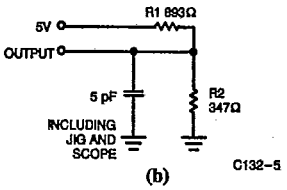
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.
7. $\overline{BUSY}$ and $\overline{INT}$ pins only.
8. Duration of the short circuit should not exceed 30 seconds.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
11. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV form steady state voltage.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

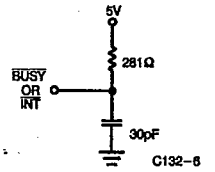
AC Test Loads and Waveforms



(a)



(b) C132-5



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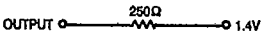
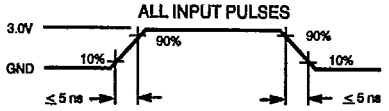
BUSY Output Load (CY7C132/CY7C136 ONLY)

Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[5,10]

Parameters	Description	7C132-25[3] 7C136-25 7C142-25 7C146-25		7C132-30 7C136-30 7C142-30 7C146-30		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45 7C136-45 7C142-45 7C146-45		7C132-55 7C136-55 7C142-55 7C146-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[13]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12,13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

Switching Characteristics Over the Operating Range[5,10] (continued)

Parameters	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING[18]												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns

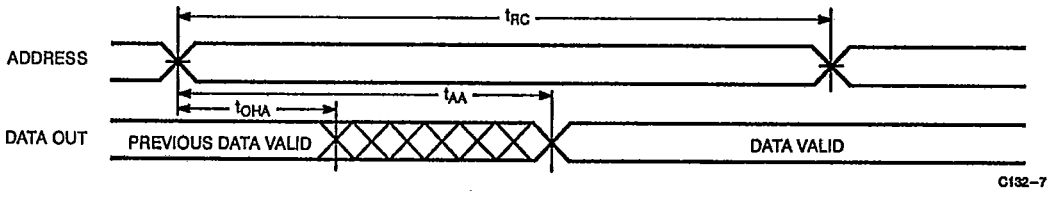
Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
18. 52-pin LCC/PLCC versions only.
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms

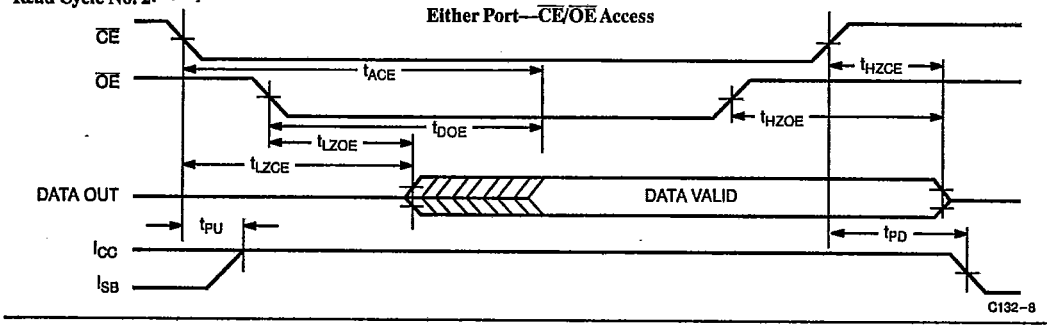
Read Cycle No. 1[19, 20]

Either Port—Address Access



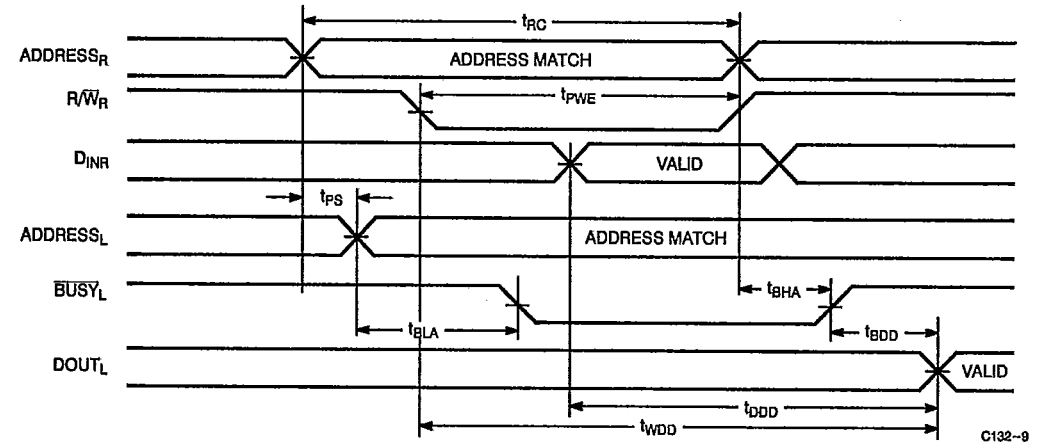
Switching Waveforms (continued)

Read Cycle No. 2[19, 21]

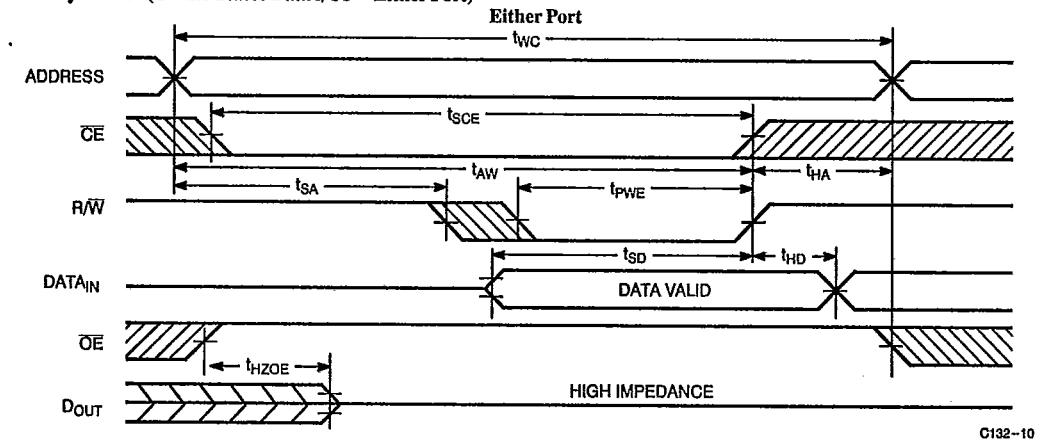


Read Cycle No. 3

Read with BUSY Master: CY7C132 and 7C136[20]



Write Cycle No.1 (OE Tri-States Data I/Os – Either Port) [14,22]



Switching Waveforms (continued)

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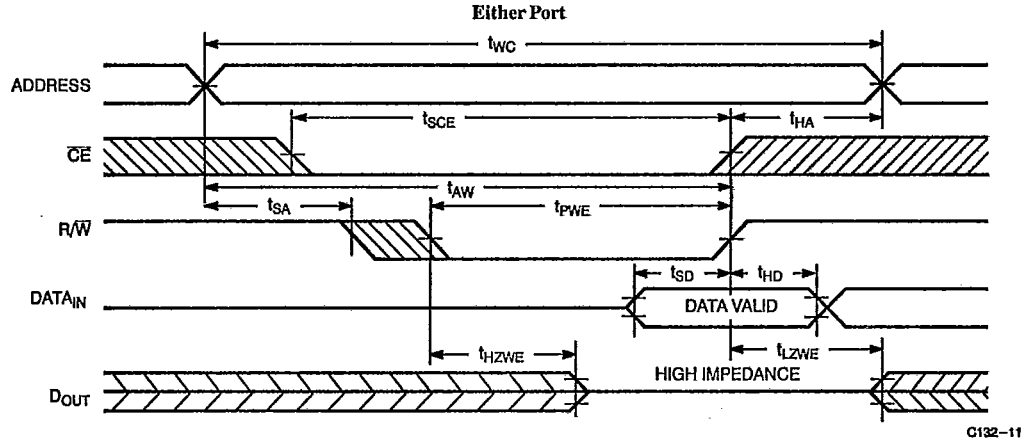
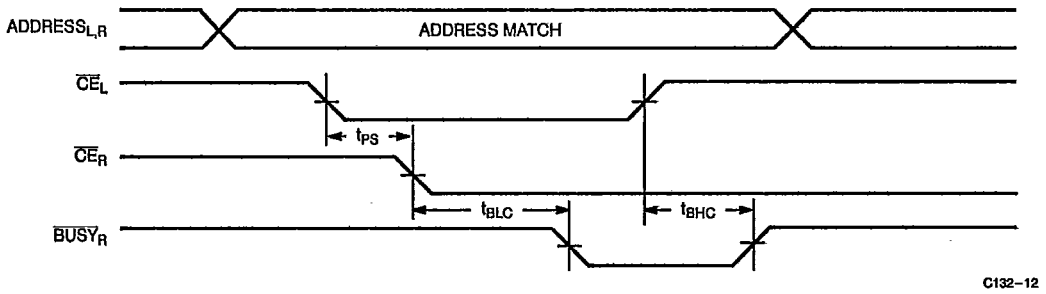
Write Cycle No. 2 ($R/\overline{W}$ Tri-States Data I/Os – Either Port)[14,23]

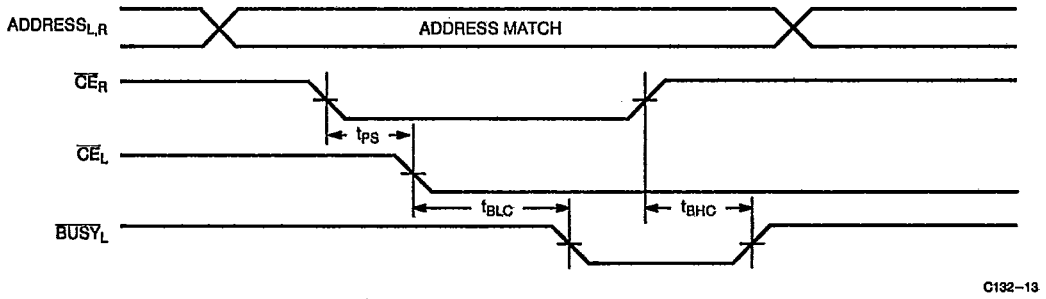


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:



Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

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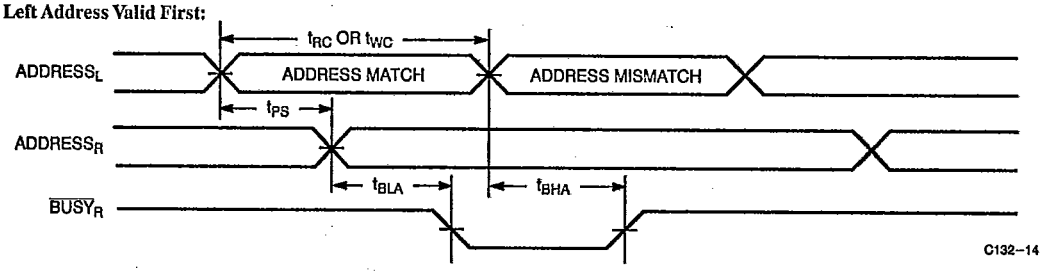
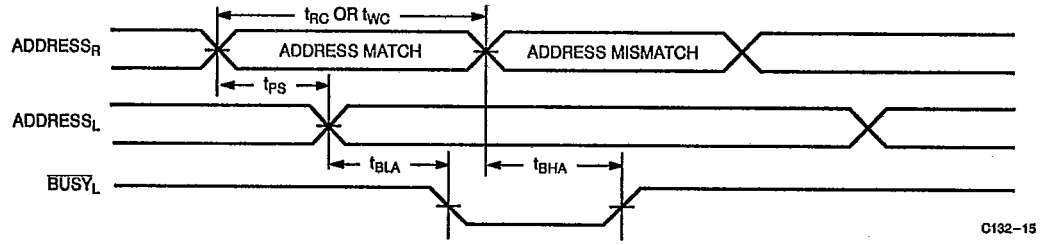
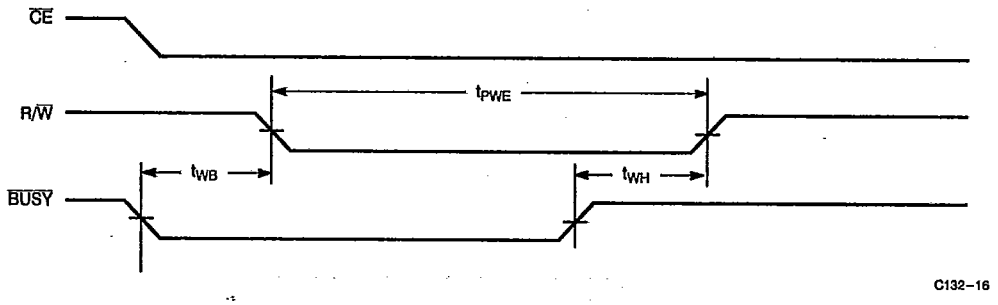
Left Address Valid First:



Right Address Valid First:



Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave: CY7C142/CY7C146)



Switching Waveforms (continued)

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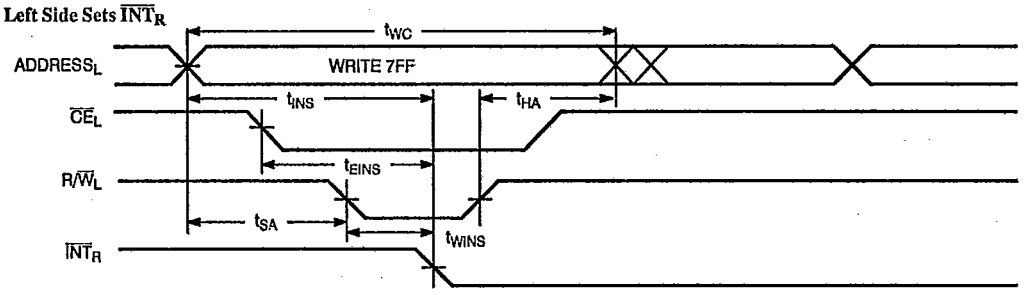
Interrupt Timing Diagrams[18]

Left Side Sets $\overline{INT}_R$



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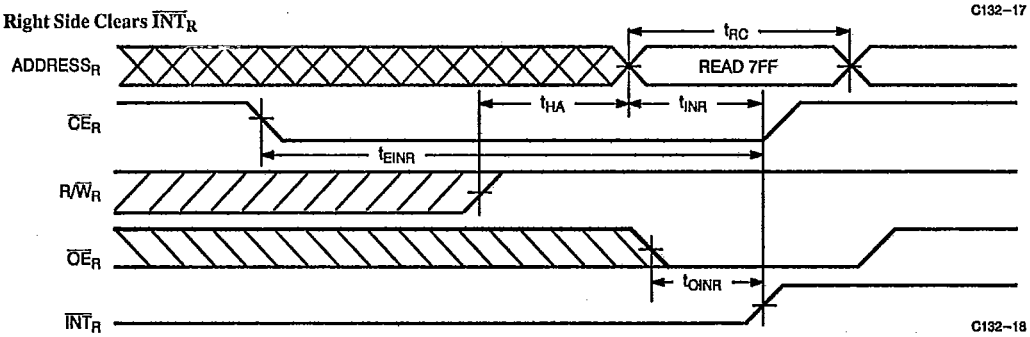
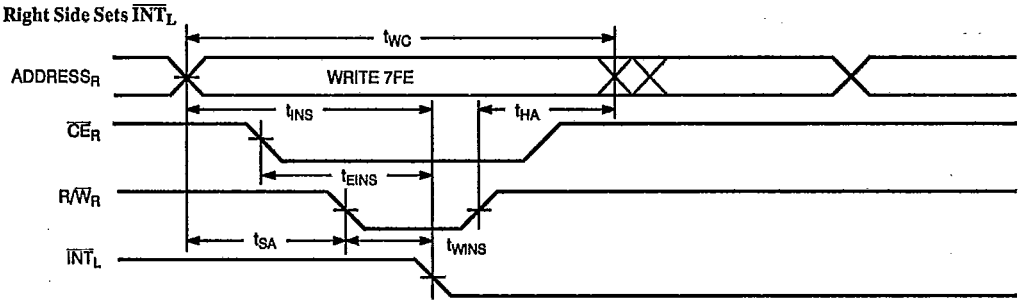
Right Side Clears $\overline{INT}_R$



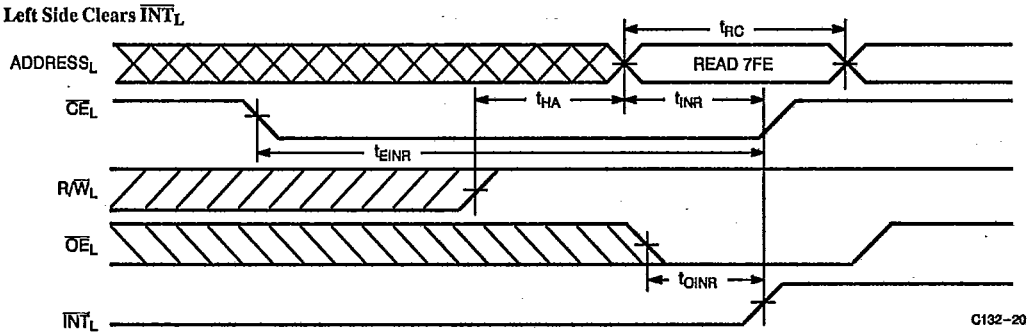
C132–18

Right Side Sets $\overline{INT}_L$



C132–19

Left Side Clears $\overline{INT}_L$



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SRAMs

Typical DC and AC Characteristics

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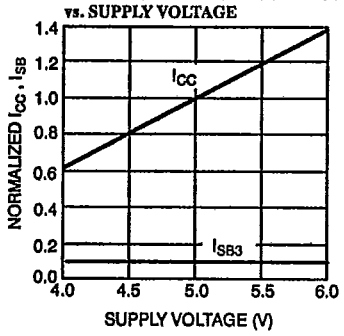
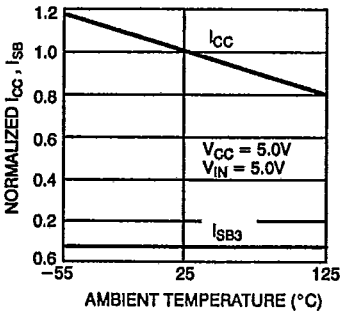
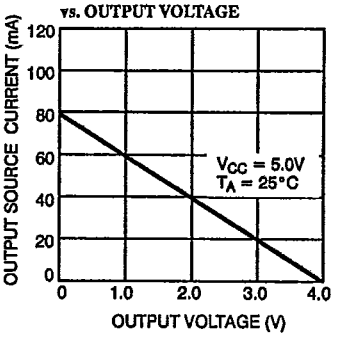
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



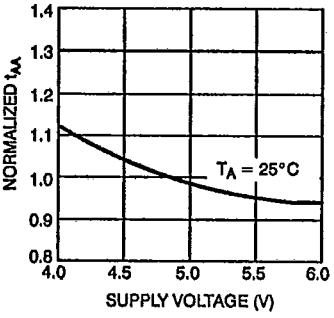
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



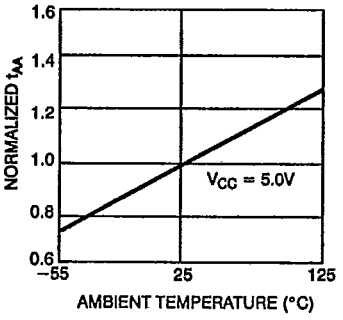
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



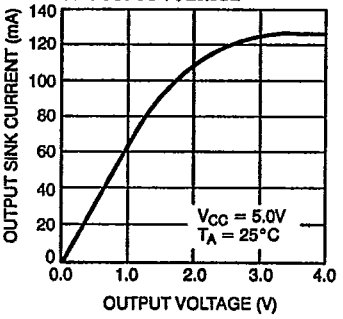
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



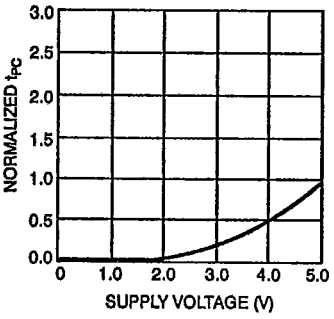
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



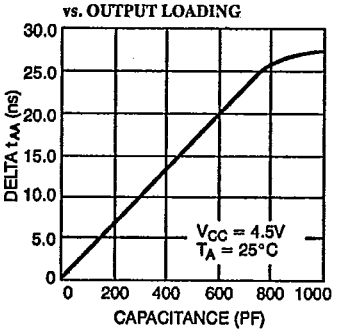
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



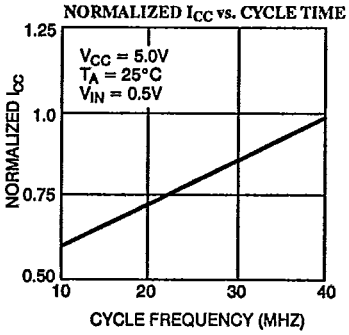
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



CYPRESS SEMICONDUCTOR

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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C132–25LC	L68	Commercial
30	CY7C132–30DC	D26	Commercial
	CY7C132–30LC	L68	
	CY7C132–30PC	P25	
	CY7C132–30DI	D26	Industrial
	CY7C132–30PI	P25	
35	CY7C132–35DC	D26	Commercial
	CY7C132–35LC	L68	
	CY7C132–35PC	P25	
	CY7C132–35DI	D26	Industrial
	CY7C132–35PI	P25	
	CY7C132–35DMB	D26	Military
	CY7C132–35FMB	F78	
	CY7C132–35LMB	L68	
45	CY7C132–45DC	D26	Commercial
	CY7C132–45LC	L68	
	CY7C132–45PC	P25	
	CY7C132–45DI	D26	Industrial
	CY7C132–45PI	P25	
	CY7C132–45DMB	D26	Military
	CY7C132–45FMB	F78	
	CY7C132–45LMB	L68	
55	CY7C132–55DC	D26	Commercial
	CY7C132–55LC	L68	
	CY7C132–55PC	P25	
	CY7C132–55DI	D26	Industrial
	CY7C132–55PI	P25	
	CY7C132–55DMB	D26	Military
	CY7C132–55FMB	F78	
	CY7C132–55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C136–25JC	J69	Commercial
	CY7C136–25LC	L69	
30	CY7C136–30JC	J69	Commercial
	CY7C136–30LC	L69	
	CY7C136–30JI	J69	Industrial
35	CY7C136–35JC	J69	Commercial
	CY7C136–35LC	L69	
	CY7C136–35JI	J69	Industrial
	CY7C136–35LMB	L69	Military
45	CY7C136–45JC	J69	Commercial
	CY7C136–45LC	L69	
	CY7C136–45JI	J69	Industrial
	CY7C136–45LMB	L69	Military
55	CY7C136–55JC	J69	Commercial
	CY7C136–55LC	L69	
	CY7C136–55JI	J69	Industrial
	CY7C136–55LMB	L69	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C142–25LC	L68	Commercial
30	CY7C142–30DC	D26	Commercial
	CY7C142–30LC	L68	
	CY7C142–30PC	P25	
	CY7C142–30DI	D26	Industrial
	CY7C142–30PI	P25	
35	CY7C142–35DC	D26	Commercial
	CY7C142–35LC	L68	
	CY7C142–35PC	P25	
	CY7C142–35DI	D26	Industrial
	CY7C142–35PI	P25	
	CY7C142–35DMB	D26	Military
	CY7C142–35FMB	F78	
	CY7C142–35LMB	L68	
45	CY7C142–45DC	D26	Commercial
	CY7C142–45LC	L68	
	CY7C142–45PC	P25	
	CY7C142–45DI	D26	Industrial
	CY7C142–45PI	P25	
	CY7C142–45DMB	D26	Military
	CY7C142–45FMB	F78	
	CY7C142–45LMB	L68	
55	CY7C142–55DC	D26	Commercial
	CY7C142–55LC	L68	
	CY7C142–55PC	P25	
	CY7C142–55DI	D26	Industrial
	CY7C142–55PI	P25	
	CY7C142–55DMB	D26	Military
	CY7C142–55FMB	F78	
	CY7C142–55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C146–25JC	J69	Commercial
	CY7C146–25LC	L69	
30	CY7C146–30JC	J69	Commercial
	CY7C146–30LC	L69	
	CY7C146–30JI	J69	Industrial
35	CY7C146–35JC	J69	Commercial
	CY7C146–35LC	L69	
	CY7C146–35JI	J69	Industrial
	CY7C146–35LMB	L69	Military
45	CY7C146–45JC	J69	Commercial
	CY7C146–45LC	L69	
	CY7C146–45JI	J69	Industrial
	CY7C146–45LMB	L69	Military
55	CY7C146–55JC	J69	Commercial
	CY7C146–55LC	L69	
	CY7C146–55JI	J69	Industrial
	CY7C146–55LMB	L69	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameters	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
24. CY7C142/CY7C146 only.

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