

DATA SHEET

SA5219

Wideband variable gain amplifier

Product specification
Replaces data of 1993 Dec 10
IC17 Data Handbook

1997 Nov 07

Philips Semiconductors



PHILIPS

Wideband variable gain amplifier

SA5219

DESCRIPTION

The SA5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The SA5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1k Ω) differential inputs. The output is 50 Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50 Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL} / V_{GAIN}$ linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	-40 to +85 $^{\circ}$ C	SA5219D	SOT109-1
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85 $^{\circ}$ C	SA5219N	SOT38-4

PIN CONFIGURATION

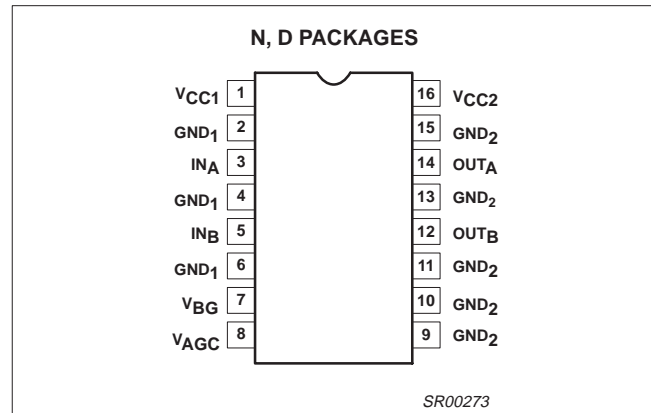


Figure 1. Pin Configuration

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, $T_A = 25^\circ\text{C}$ (still air) ¹ 16-Pin Plastic DIP 16-Pin Plastic SO	1450 1100	mW mW
T_{JMAX}	Maximum operating junction temperature	150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-65 to +150	$^\circ\text{C}$

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA} :
 16-Pin DIP: $\theta_{JA} = 85^\circ\text{C/W}$
 16-Pin SO: $\theta_{JA} = 110^\circ\text{C/W}$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	$V_{CC1} = V_{CC2} = 4.5$ to 7.0V	V
T_A	Operating ambient temperature range SA Grade	-40 to +85	$^\circ\text{C}$
T_J	Operating junction temperature range SA Grade	-40 to +105	$^\circ\text{C}$

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = +5\text{V}$, $V_{AGC} = 1.0\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, $R_L = 10\text{k}\Omega$	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, $R_L = 10\text{k}\Omega$	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at $\pm 50\mu\text{A}$	0.8	1.2	1.6	$\text{k}\Omega$
R_{OUT}	Output resistance (single-ended)	DC tested at $\pm 1\text{mA}$	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			± 20	± 150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	$4.5\text{V} < V_{CC} < 7\text{V}$ $R_{BG} = 10\text{k}\Omega$	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		$\text{k}\Omega$
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	$0\text{V} < V_{AGC} < 1.3\text{V}$		-0.7	-6	μA

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AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = +5.0\text{V}$, $V_{AGC} = 1.0\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		± 0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation ¹			200		mV _{p-p}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation ¹	$R_L = 50\Omega$		400		mV _{p-p}
		$R_L = 1k\Omega$		1.9		V _{p-p}
NF	Noise figure (unmatched configuration)	$R_S = 50\Omega$, $f = 50\text{MHz}$		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	$f = 100\text{MHz}$		2.5		nV/ $\sqrt{\text{Hz}}$
S12	Reverse isolation	$f = 100\text{MHz}$		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	$R_L = 50\Omega$		0.013		dB/ $^\circ\text{C}$
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	$f = 100\text{MHz}$		-3		dBm
P_{I-1dB}	1dB gain compression point at input	$f = 100\text{MHz}$, $V_{AGC} = 0.1\text{V}$		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	$f = 100\text{MHz}$, $V_{AGC} > 0.5\text{V}$		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	$f = 100\text{MHz}$, $V_{AGC} < 0.5\text{V}$		+5		dBm
ΔG_{AB}	Gain match output A to output B	$f = 100\text{MHz}$, $V_{AGC} = 1\text{V}$		0.1		dB

NOTE:

1. With $R_L > 1k\Omega$, overload occurs at input for single-ended gain $< 13\text{dB}$ and at output for single-ended gain $> 13\text{dB}$. With $R_L = 50\Omega$, overload occurs at input for single-ended gain $< 6\text{dB}$ and at output for single-ended gain $> 6\text{dB}$.

SA5219 APPLICATIONS

The SA5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 2. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The SA5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about $1k\Omega$. The main advantage to a differential input configuration is to provide the balun function.

Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about $1k\Omega$. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω . A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The SA5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The SA5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the SA5219. A

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maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the SA5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the SA5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the SA5219 is shown in Figure 3. Three SA5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes

BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An SA5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three SA5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three SA5219s will give a dynamic range in excess of 60dB.

The SA5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

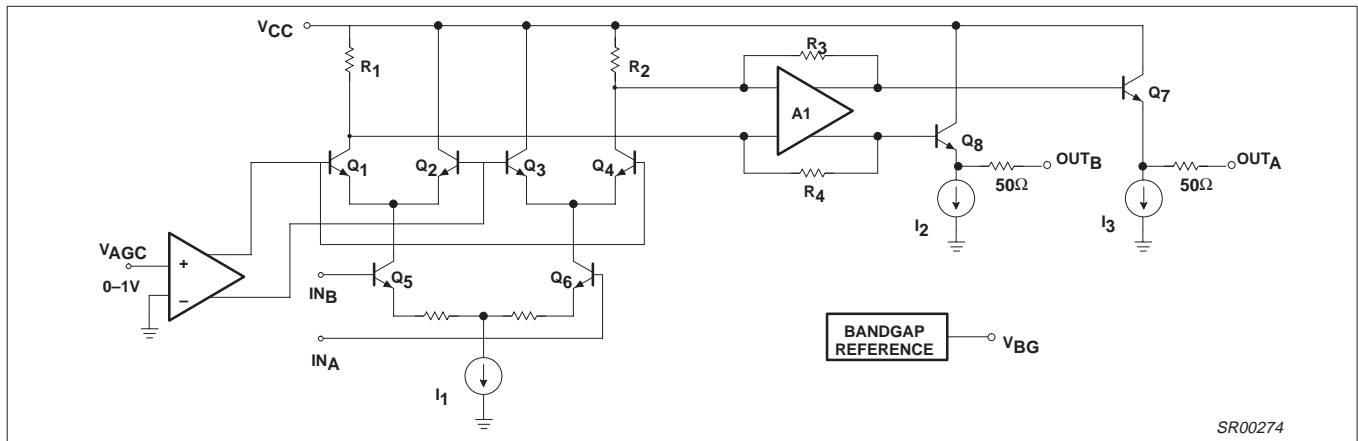


Figure 2. Equivalent Schematic of VGA

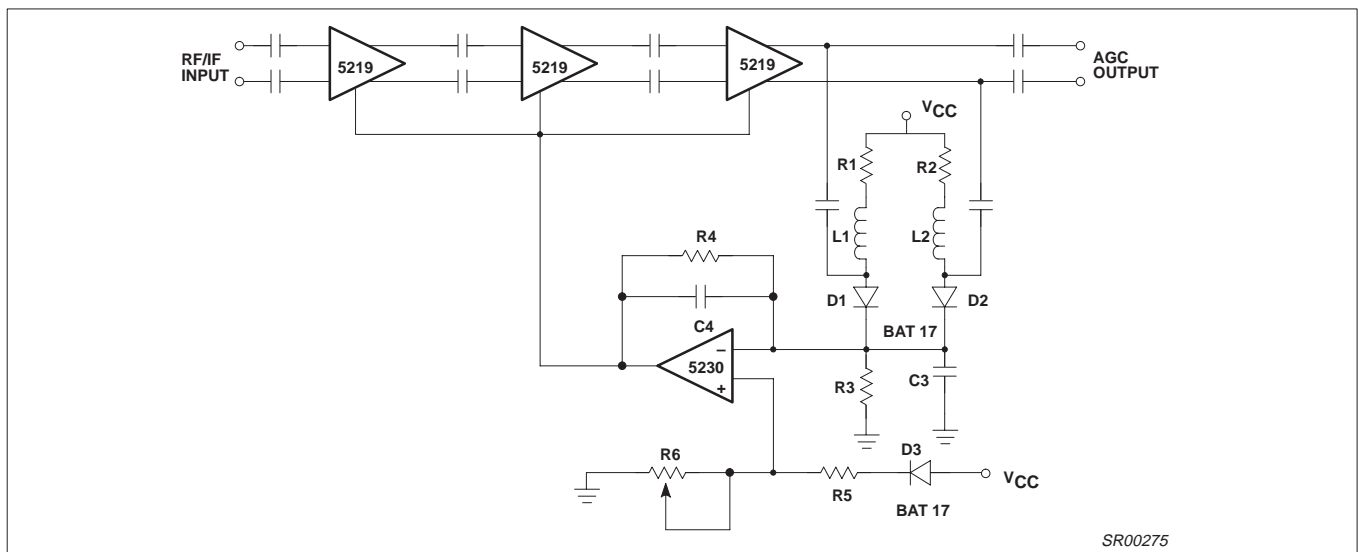


Figure 3. AGC Configuration Using Cascaded SA5219s

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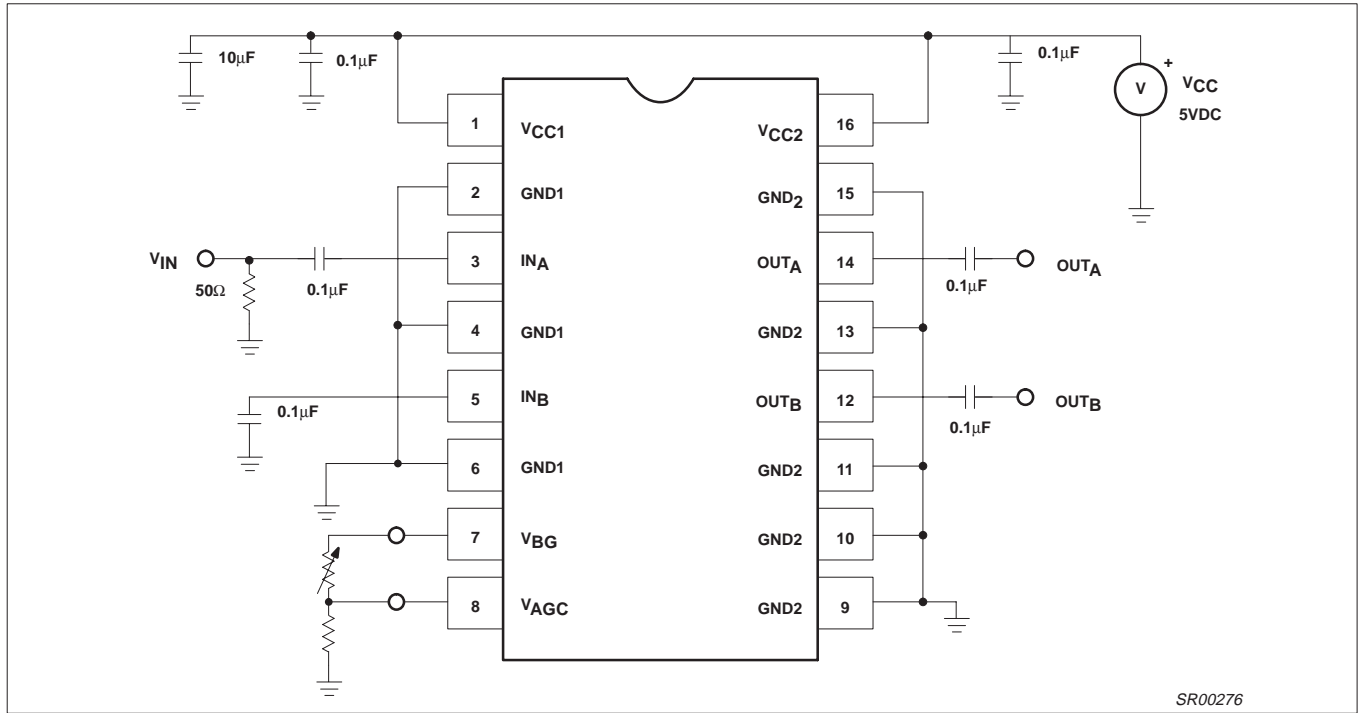


Figure 4. VGA AC Evaluation Board

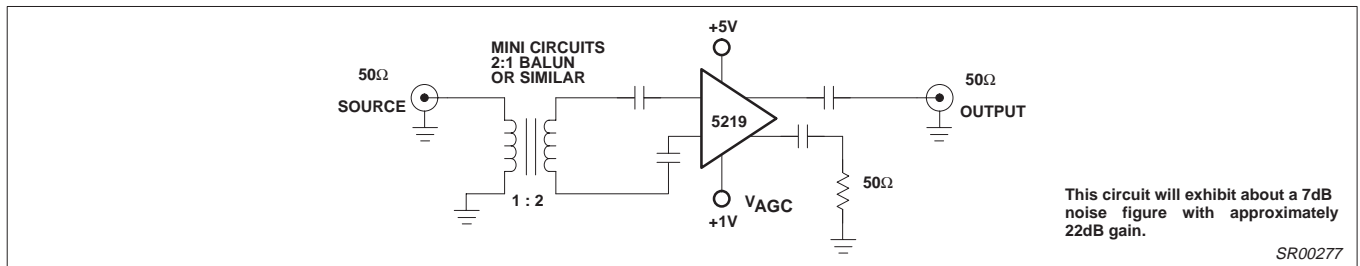


Figure 5. Broadband Noise Optimization

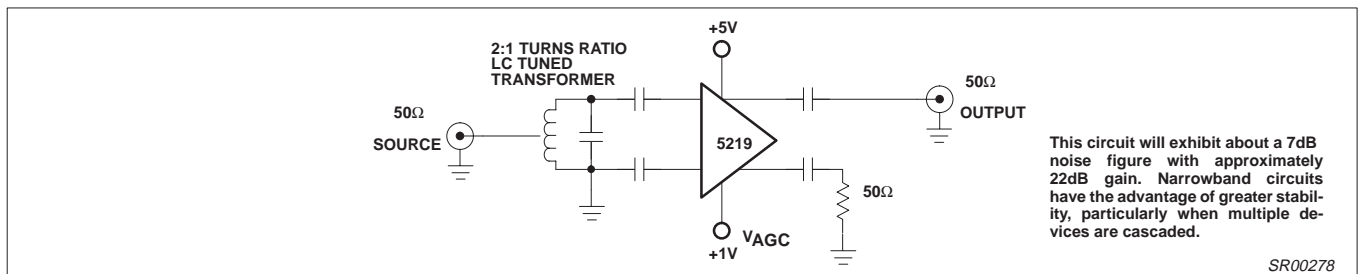


Figure 6. Narrowband Noise Optimization

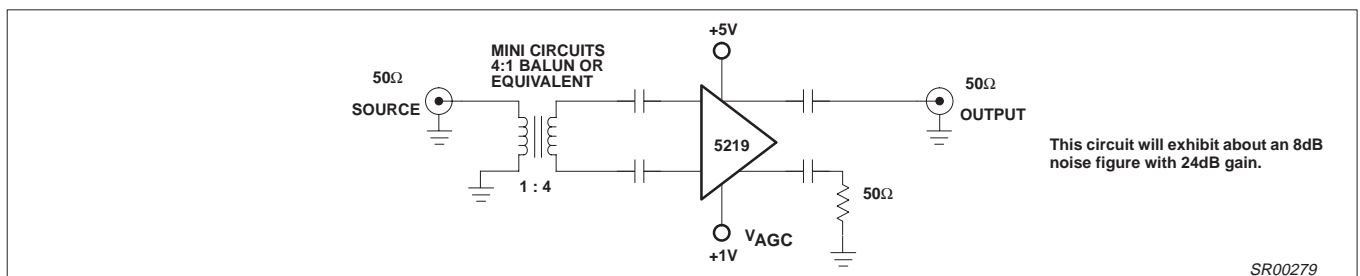


Figure 7. Broadband Gain Optimization

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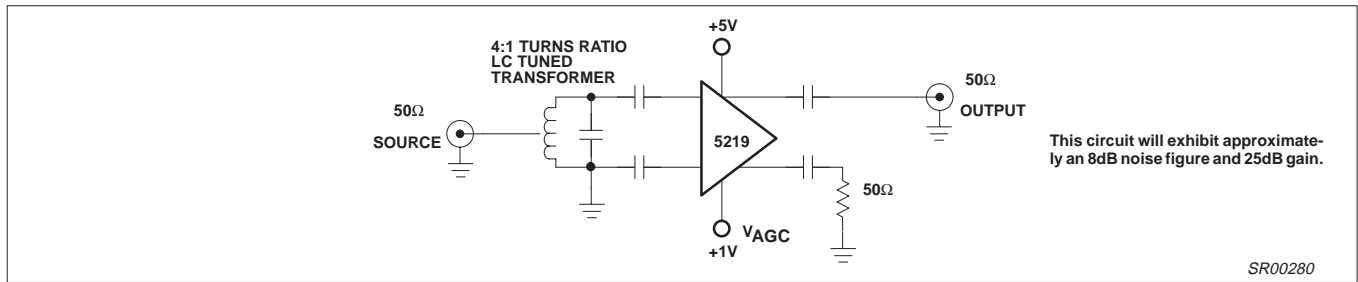


Figure 8. Narrowband Gain Optimization

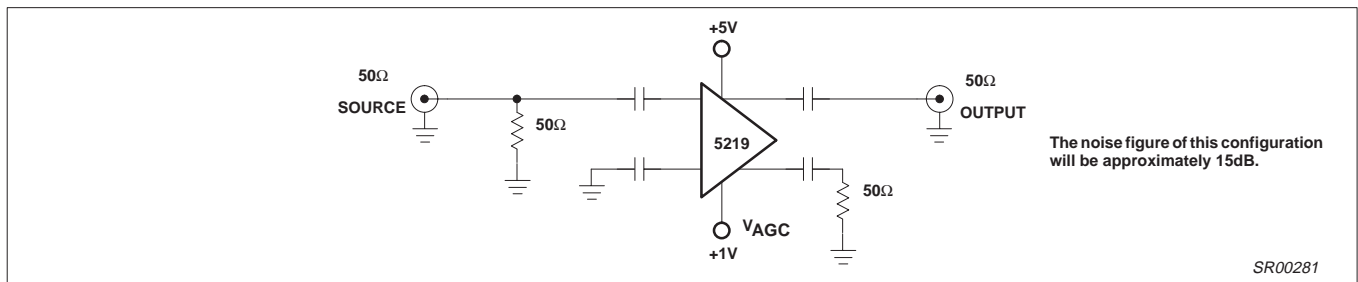


Figure 9. Simple Amplifier Configuration

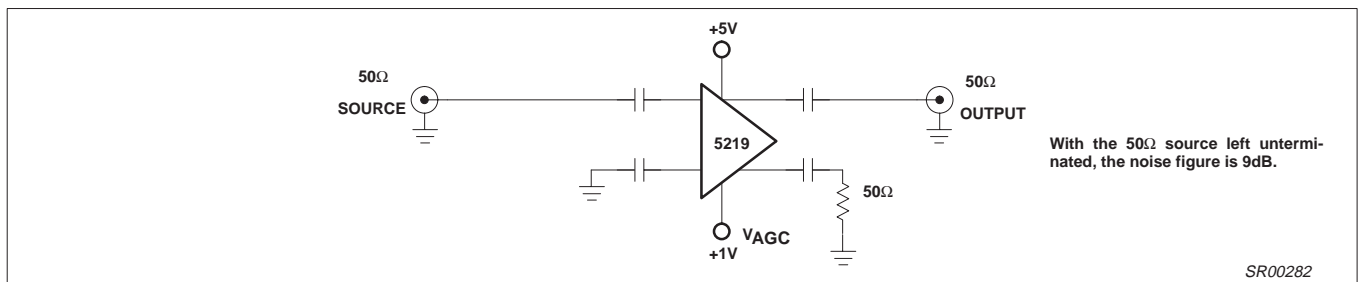


Figure 10. Underterminated Configuration

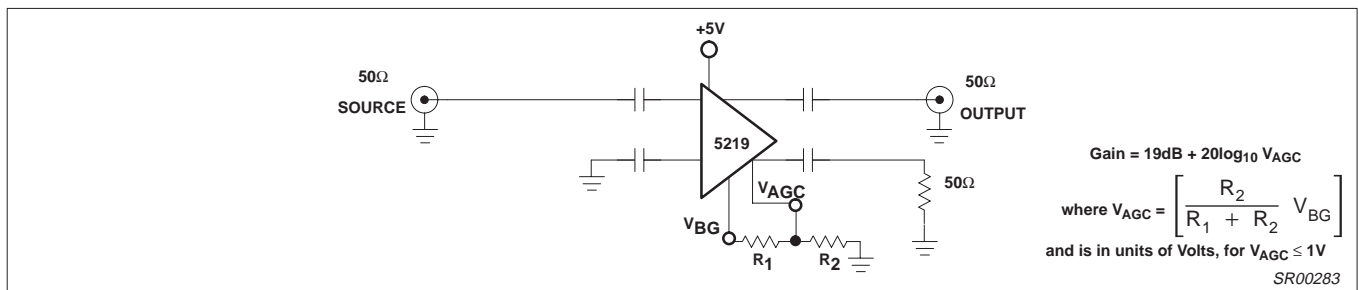


Figure 11. User-Programmable Fixed Gain Block

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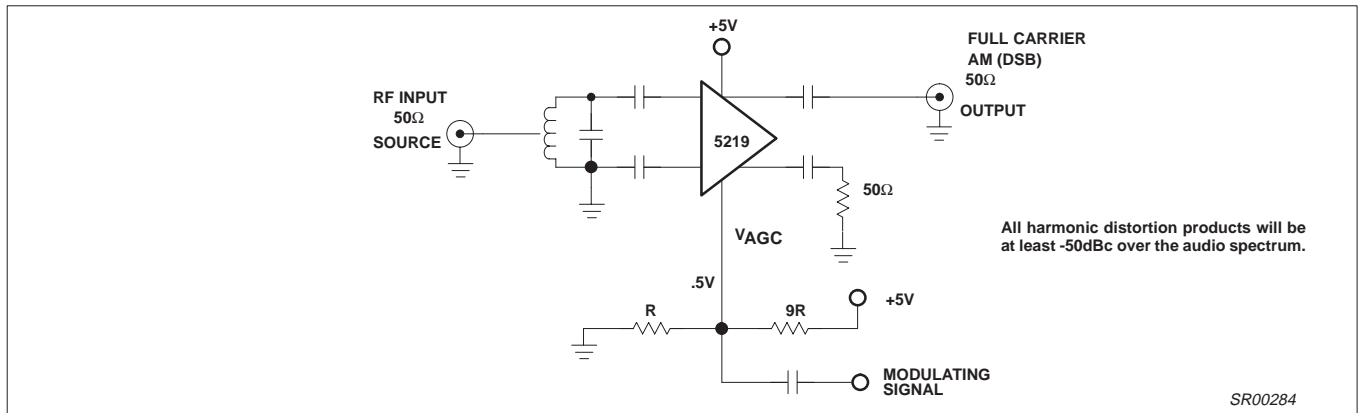


Figure 12. AM Modulator

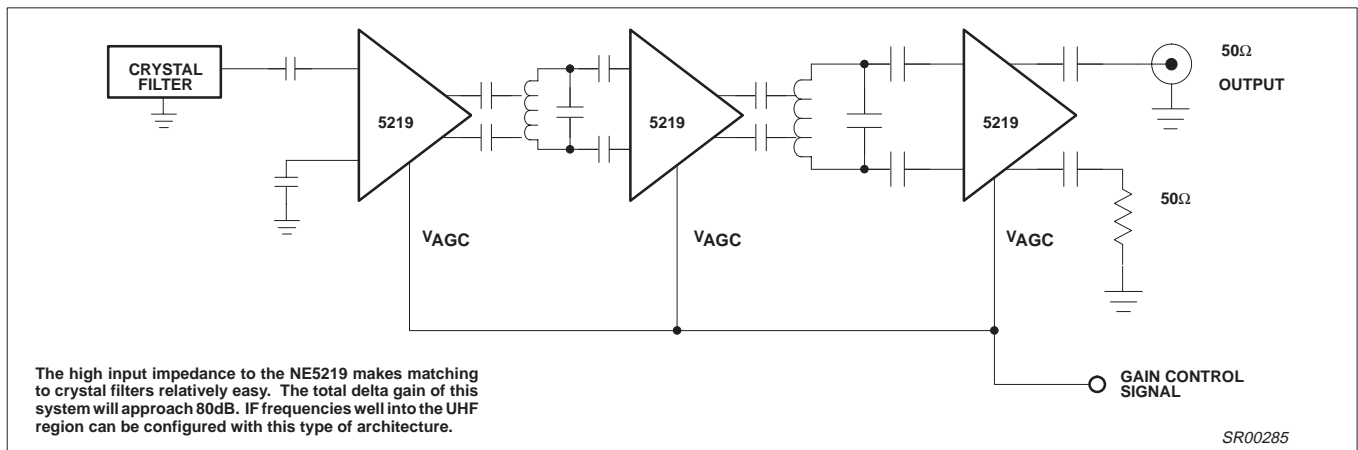


Figure 13. Receiver AGC IF Gain

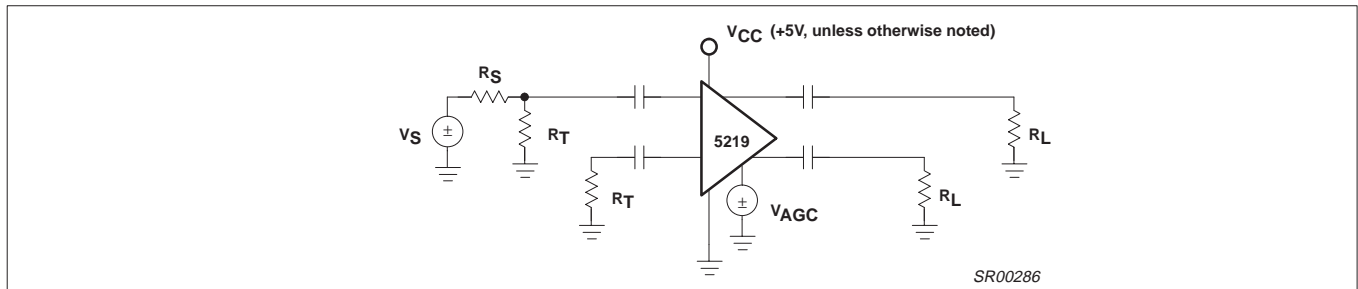


Figure 14. Test Set-up 1 (Used for all Graphs)

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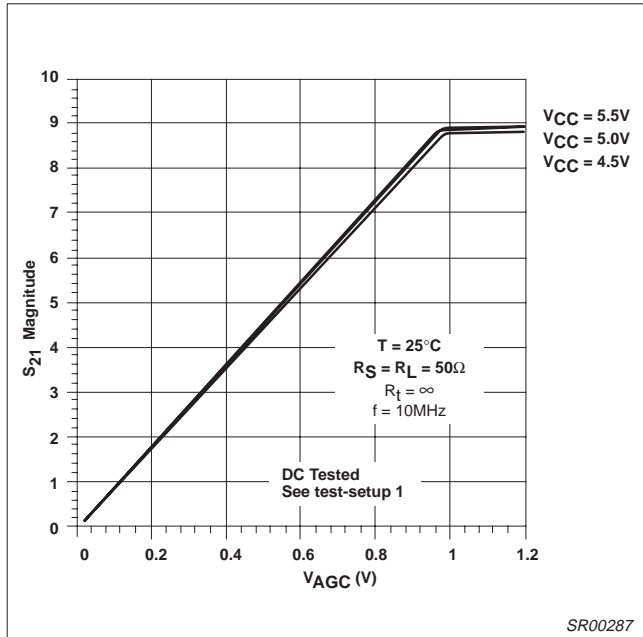


Figure 15. Gain vs V_{AGC} and V_{CC}

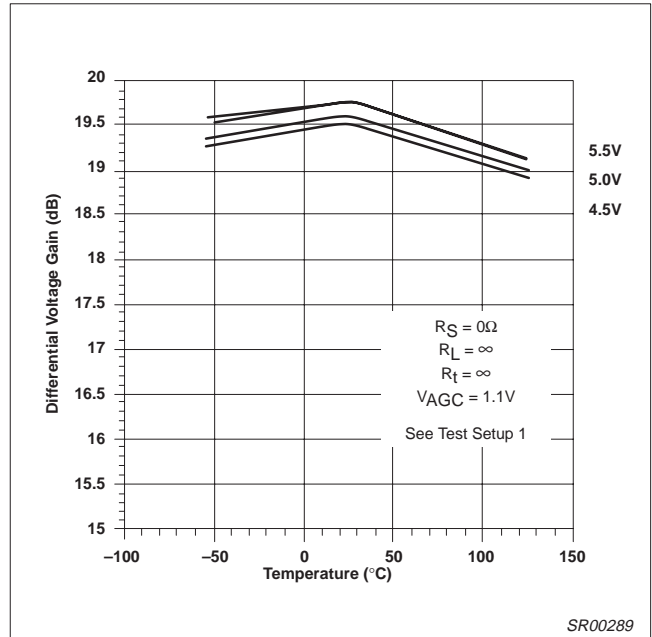


Figure 17. Voltage Gain vs Temperature and V_{CC}

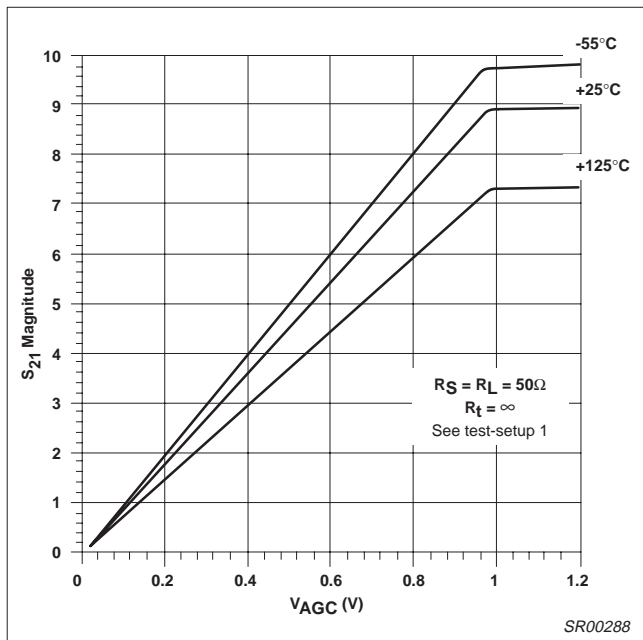


Figure 16. Insertion Gain vs V_{AGC} and Temperature

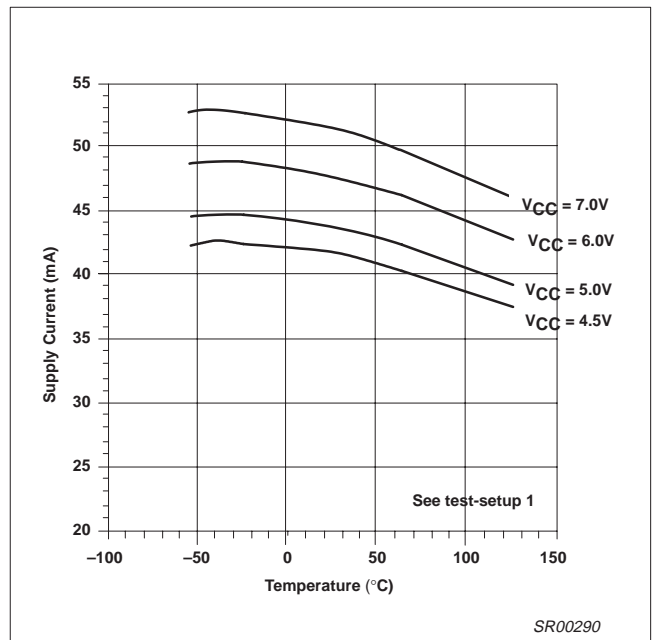


Figure 18. Supply Current vs Temperature and V_{CC}

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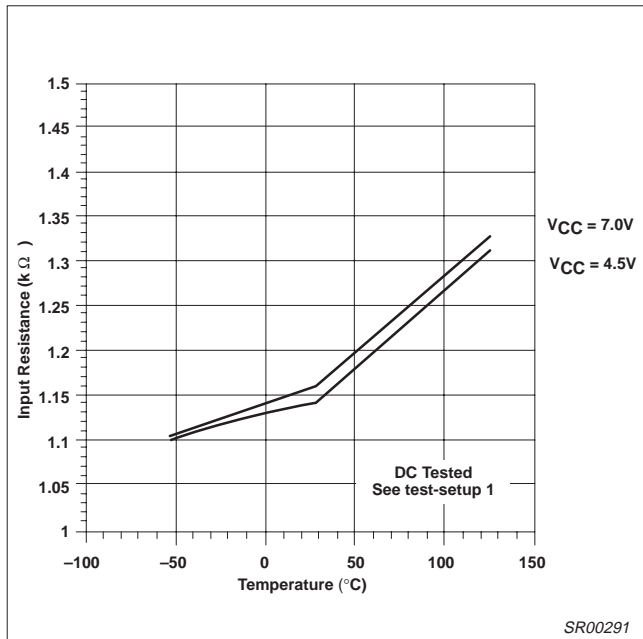


Figure 19. Input Resistance vs Temperature

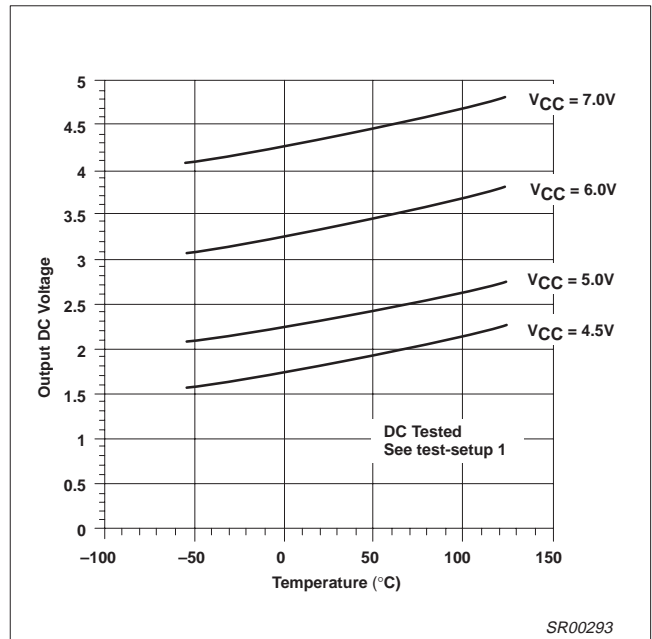


Figure 21. Output Bias Voltage vs Temperature and V_{CC}

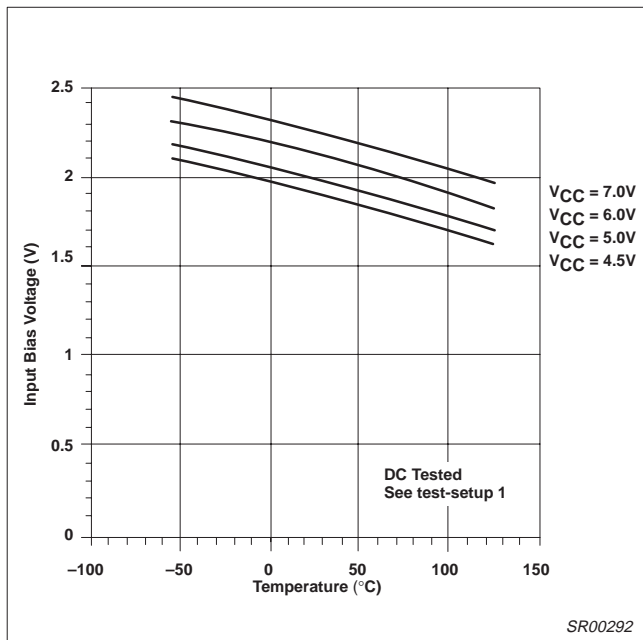


Figure 20. Input Bias Voltage vs Temperature

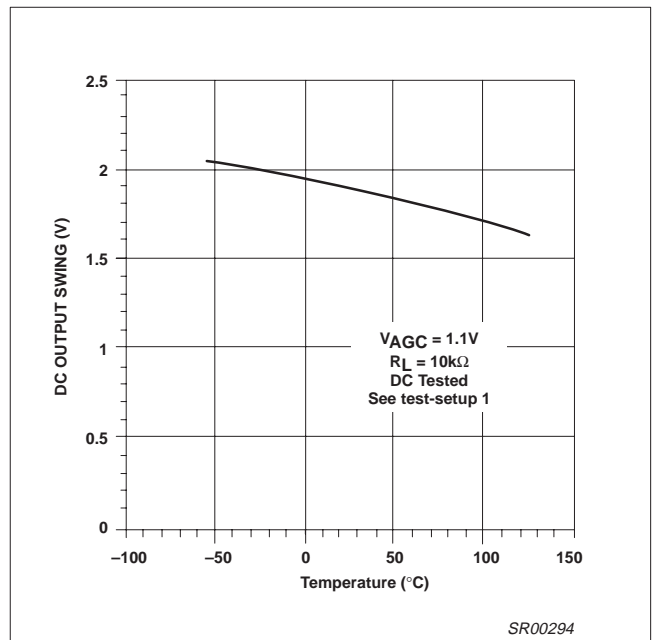


Figure 22. DC Output Swing vs Temperature

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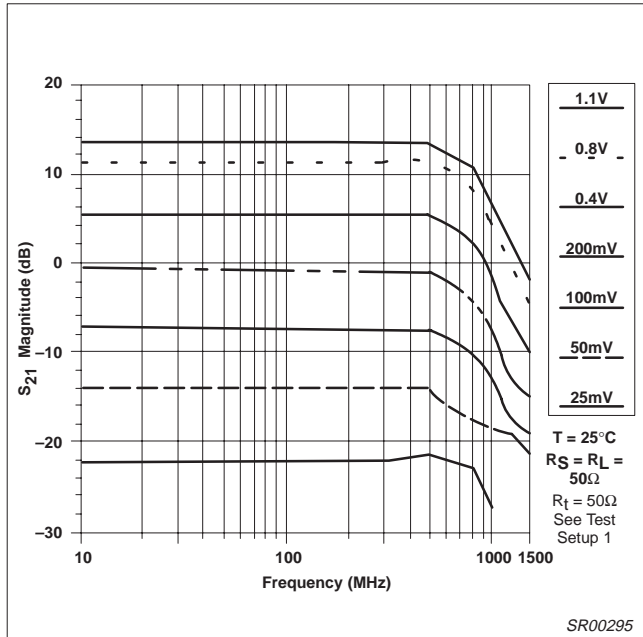


Figure 23. Insertion Gain vs Frequency and V_{AGC}

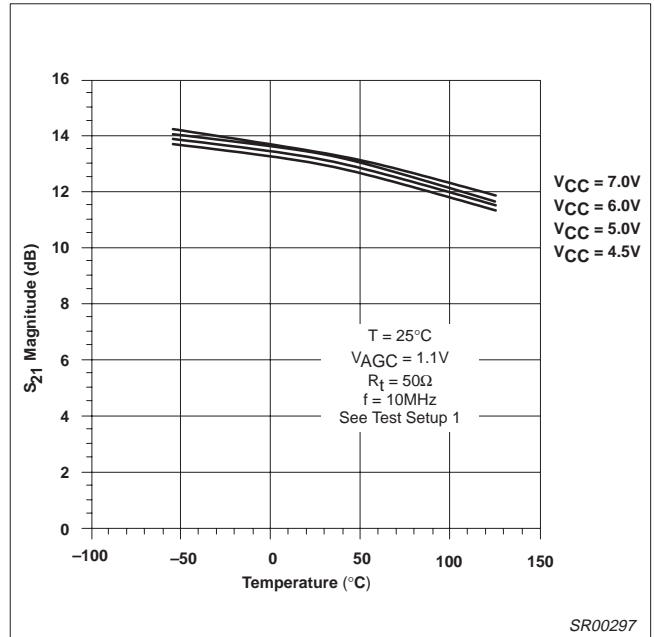


Figure 25. Insertion Gain vs Temperature and V_{CC}

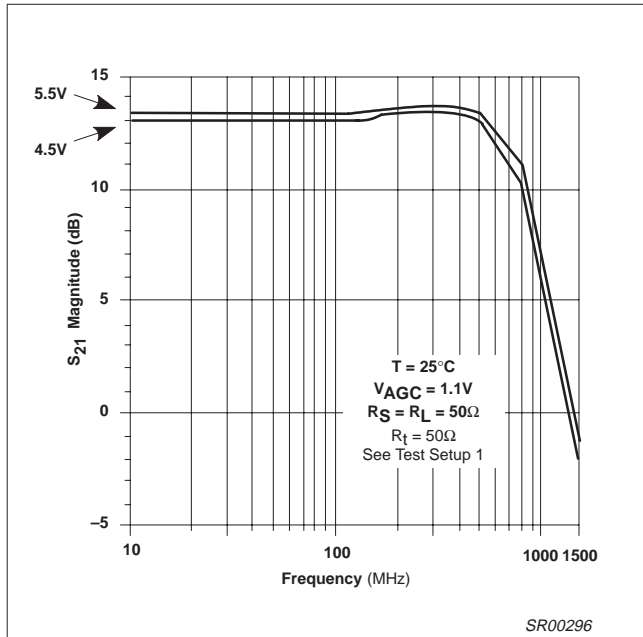


Figure 24. Insertion Gain vs Frequency and V_{CC}

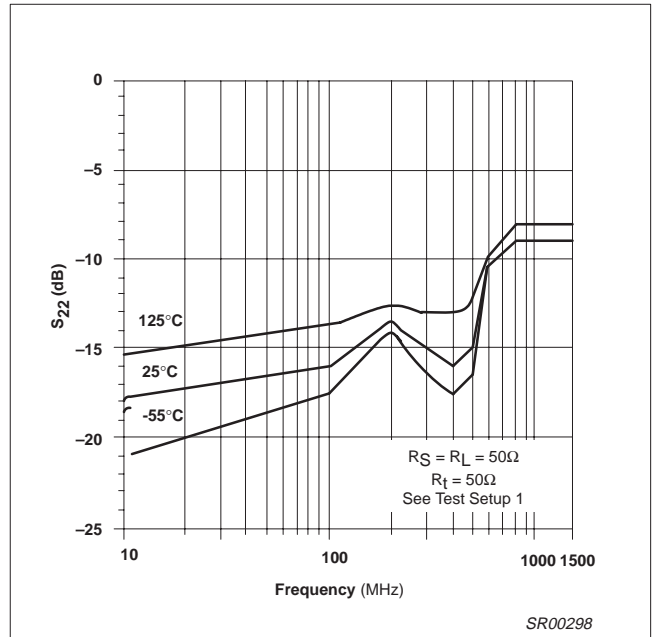


Figure 26. Output Return Loss vs Frequency

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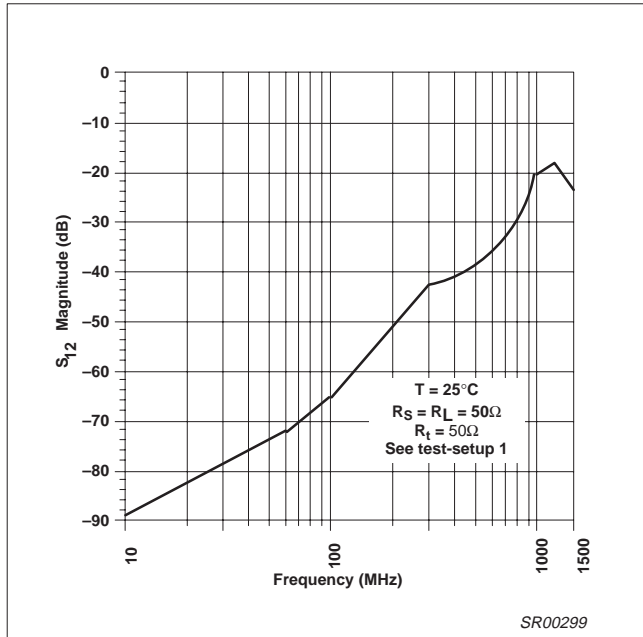


Figure 27. Reverse Isolation vs Frequency

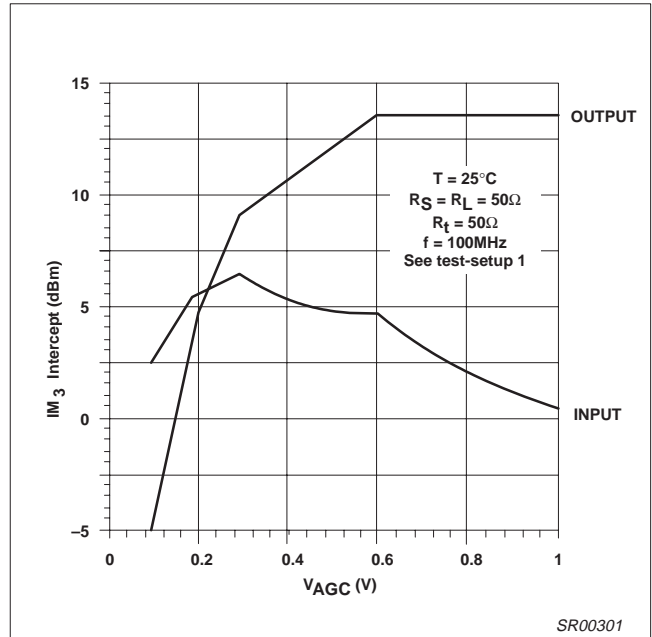


Figure 29. Third-Order Intermodulation Intercept vs V_{AGC}

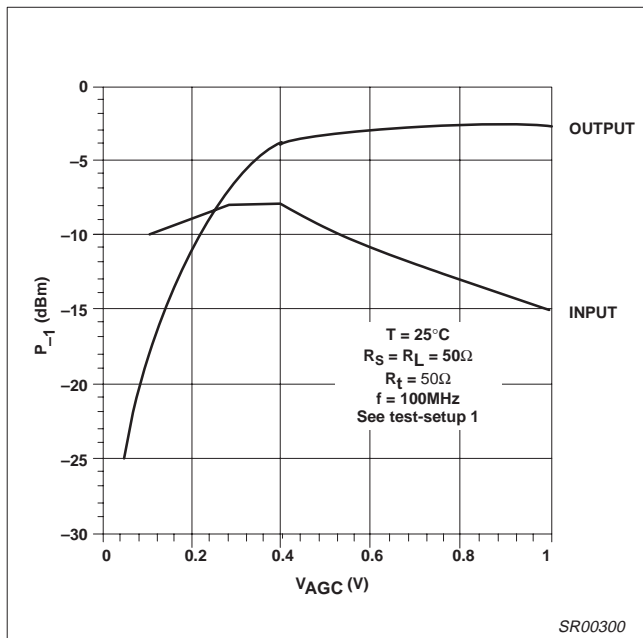


Figure 28. 1dB Gain Compression vs V_{AGC}

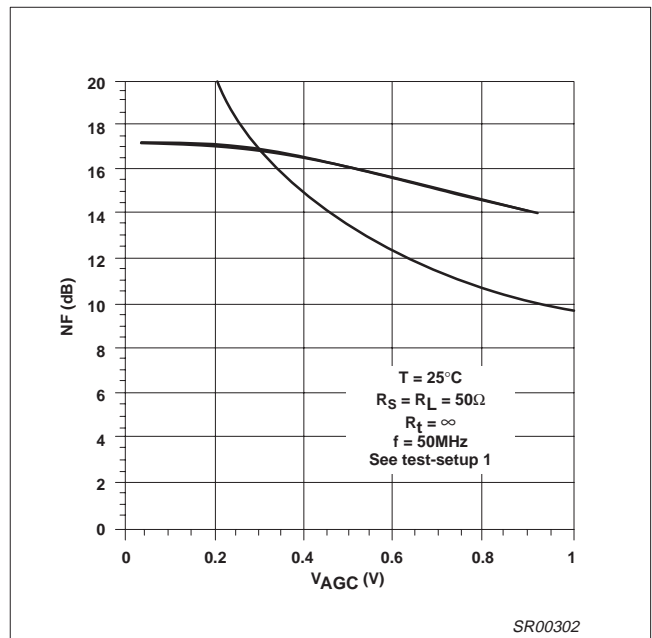


Figure 30. Noise Figure vs V_{AGC}

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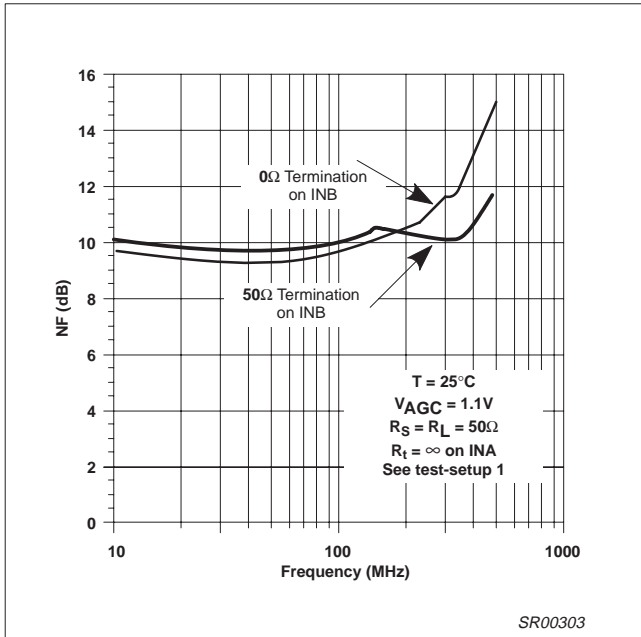


Figure 31. Noise Figure vs Frequency

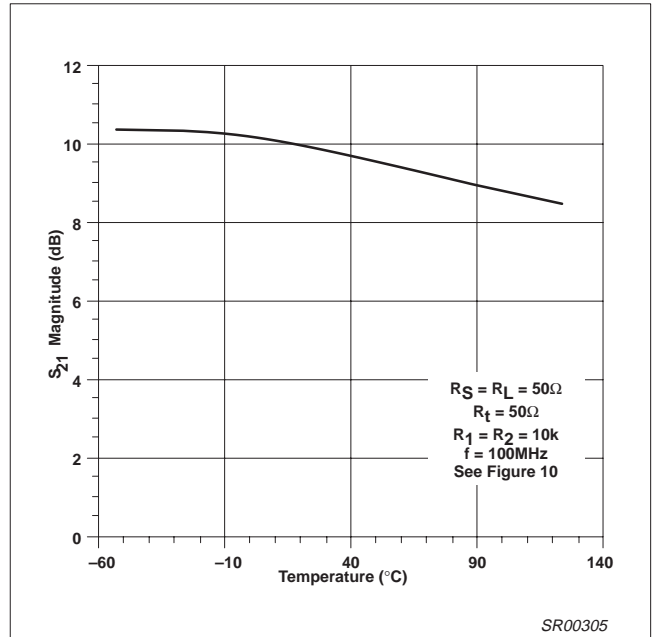


Figure 33. Fixed Gain vs Temperature

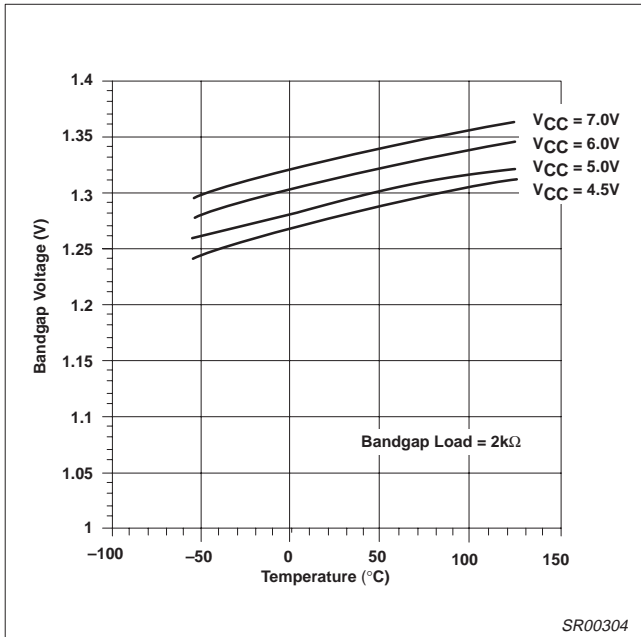


Figure 32. Bandgap Voltage vs Temperature and V_{CC}

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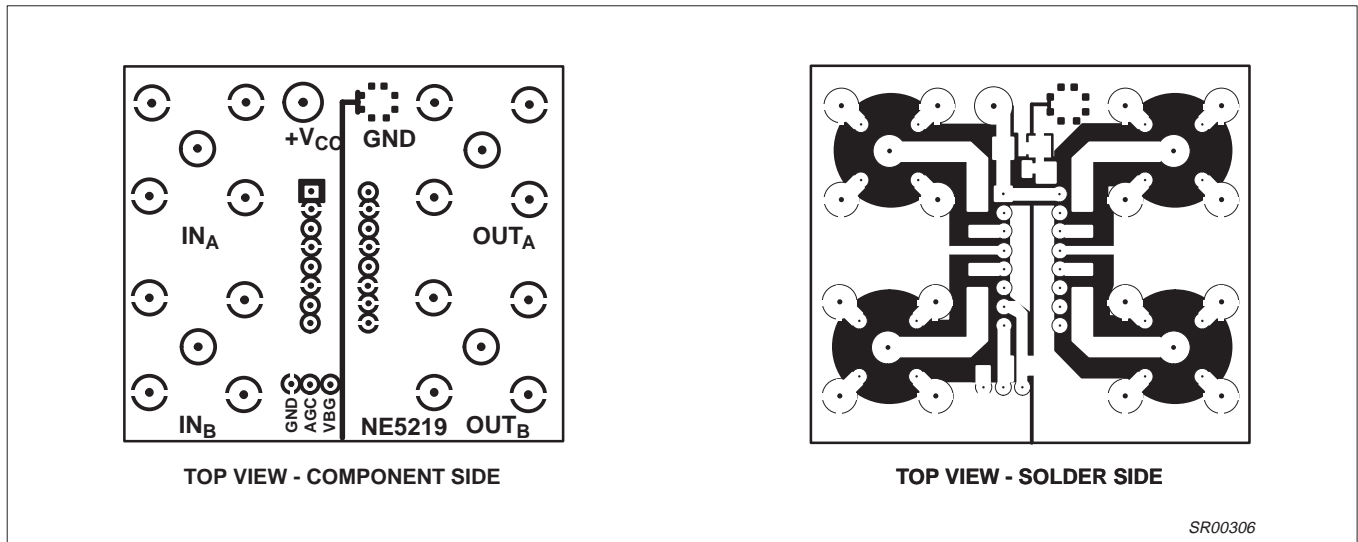


Figure 34. VGA AC Evaluation Board Layout (DIP Package)

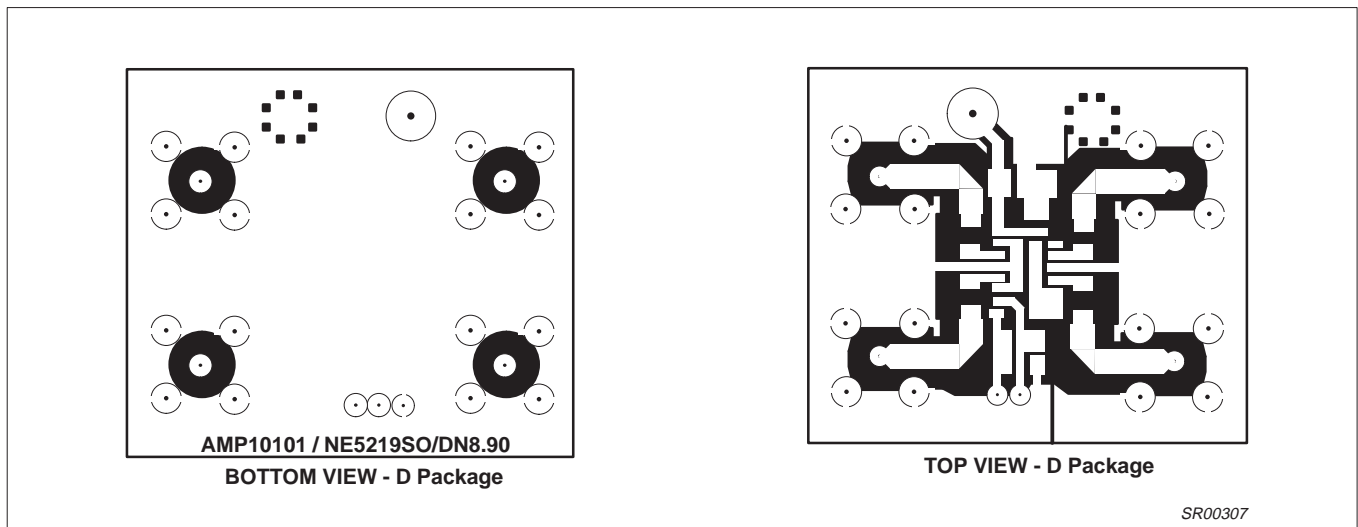


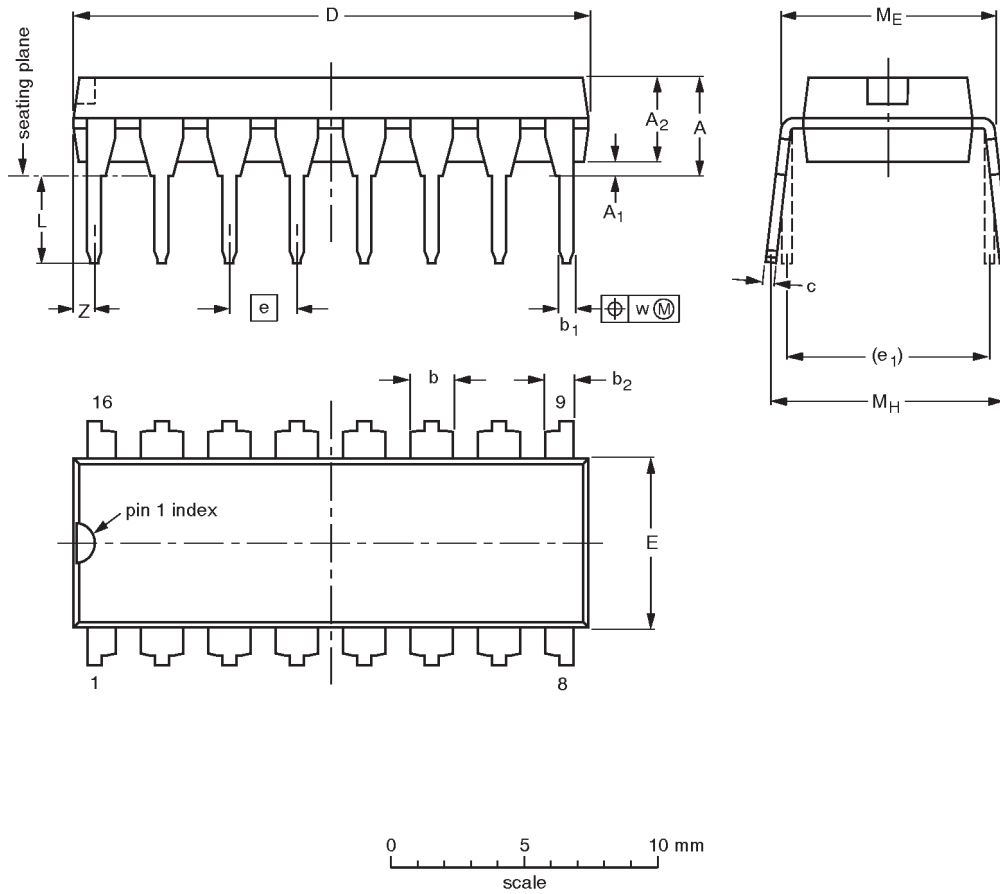
Figure 35. VGA AC Evaluation Board Layout (SO Package)

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

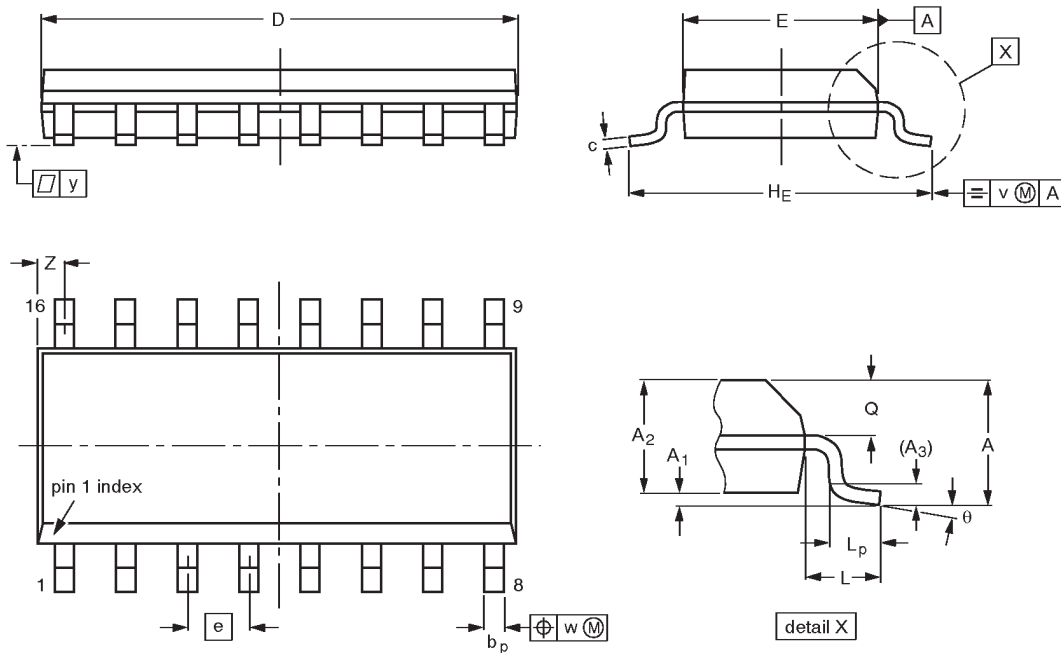
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

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NOTES

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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