

300mA Dual LDO Regulator with POR

General Description

RT9012 is a dual channel, low noise, and low dropout with the sourcing ability up to 300mA and power-on reset function. The range of output voltage is from 1.2V to 3.6V by operating from 2.5V to 5.5V input.

RT9012 offers 2% accuracy, extremely low dropout voltage (240mV @ 300mA), and extremely low ground current, only 27μA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection.

RT9012 is short circuit thermal folded back protected. RT9012 lowers its OTP trip point from 165°C to 110°C when output short circuit occurs (VOUT < 0.4V) providing maximum safety to end users.

RT9012 can operate stably with very small ceramic output capacitors, reducing required board space and component cost. RT9012 is available in fixed output voltages in the WDFN-8L 2x2 package.

Ordering Information

RT9012-□□□□	
Package Type	QW : WDFN-8L 2x2 (W-Type)
Operating Temperature Range	P : Pb Free with Commercial Standard G : Green (Halogen Free with Commercial Standard)
Output Voltage : VOUT1/VOUT2	CM : 1.20V/2.80V, FM : 1.50V/2.80V FS : 1.50V/3.30V, GK : 1.80V/2.60V GM : 1.80V/2.80V, GP : 1.80V/3.00V GS : 1.80V/3.30V, JG : 2.50V/1.80V JM : 2.50V/2.80V, JP : 2.50V/3.00V JS : 2.50V/3.30V, JN : 2.50V/2.85V MG : 2.80V/1.80V, MM : 2.80V/2.80V NN : 2.85V/2.85V, PP : 3.00V/3.00V

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

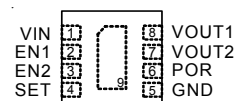
- Wide Operating Voltage Ranges : 2.5V to 5.5V
- Low-Noise for RF Application
- No Noise Bypass Capacitor Required
- Fast Response in Line/Load Transient
- TTL-Logic-Controlled Shutdown Input
- Low Temperature Coefficient
- Dual LDO Outputs (300mA/300mA)
- Ultra-low Quiescent Current 27μA/LDO
- High Output Accuracy 2%
- Short Circuit Protection
- Thermal Shutdown Protection
- Current Limit Protection
- Short Circuit Thermal Folded Back Protection
- Tiny 8-Lead WDFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- CDMA/GSM Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

Pin Configurations

(TOP VIEW)

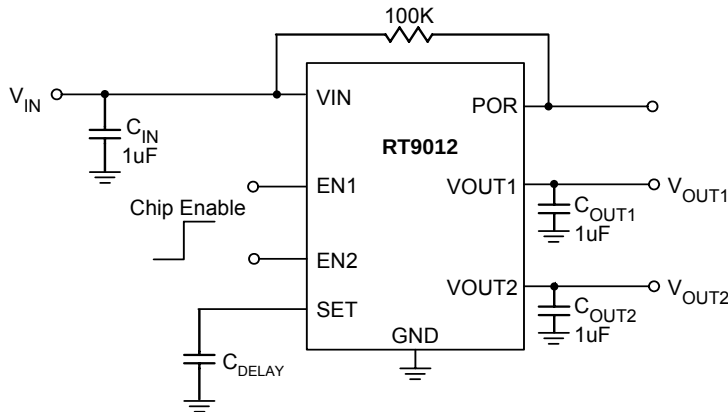


WDFN-8L 2x2

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

Typical Application Circuit



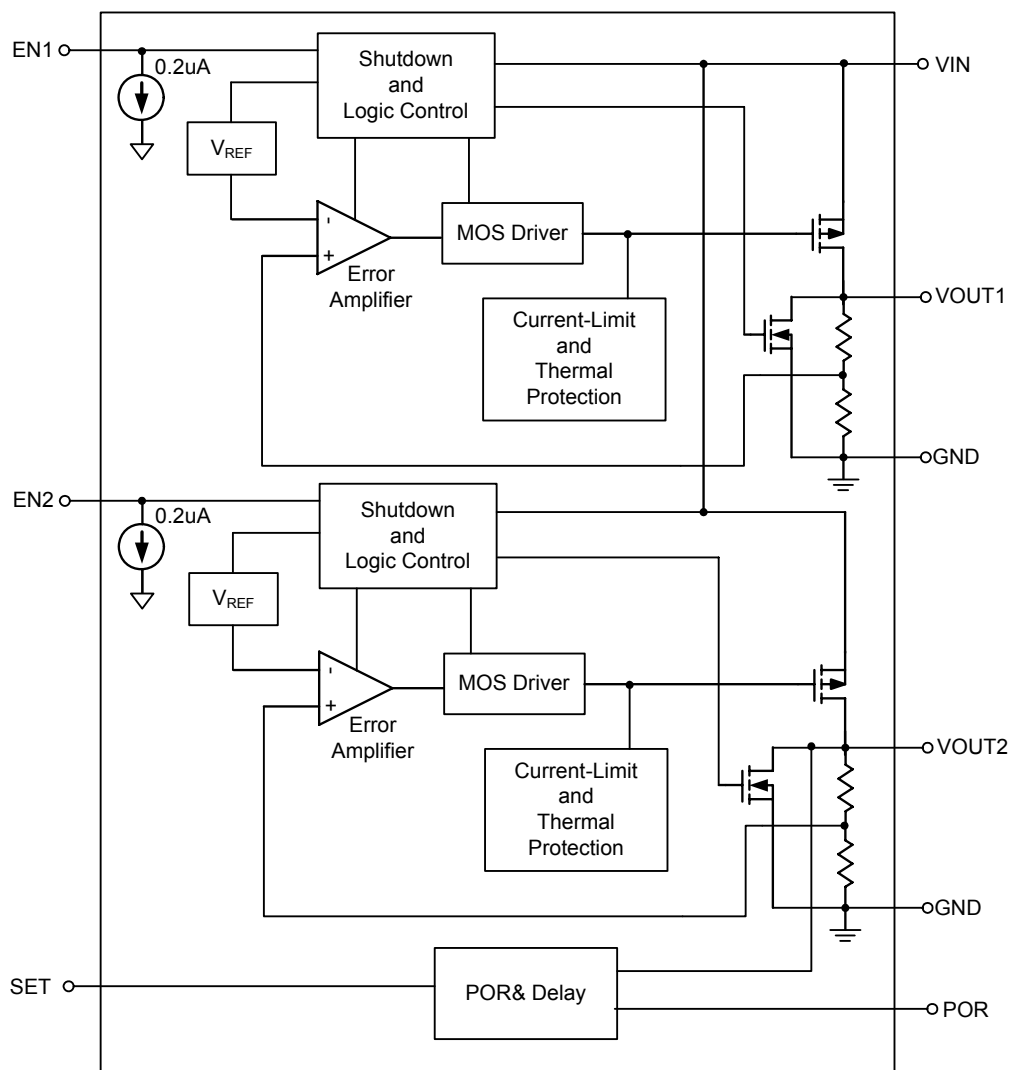
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Supply Input.
2	EN1	Chip Enable1 (Active High).
3	EN2	Chip Enable2 (Active High).
4	SET	Delay Set Input. Connect external capacitor to GND to set the internal delay.
5	GND	Common Ground.
6	POR	Power-On Reset Output : Open-drain output. Active low indicates an output under-voltage condition on regulator 2.
7	VOUT2	Channel 2 Output Voltage.
8	VOUT1	Channel 1 Output Voltage.
Exposed Pad (9)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Available Voltage Version

Code	C	F	W	G	D	Y	H	E	J	K	T
Voltage	1.2	1.5	1.6	1.8	1.85	1.9	2	2.1	2.5	2.6	2.65
Code	L	M	N	V	P	Q	R	S	--	--	--
Voltage	2.7	2.8	2.85	2.9	3	3.1	3.2	3.3	--	--	--

Function Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage	6V
Other I/O Pin Voltages	6V
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$	
WDFN-8L 2x2	0.606W
Package Thermal Resistance (Note 4)	
WDFN-8L 2x2, θ_{JA}	165°C/W
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility (Note 2)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

Recommended Operating Conditions (Note 3)

Supply Input Voltage	2.5V to 5.5V
Enable Input Voltage	0V to 5.5V
Operation Junction Temperature Range	-40°C to 125°C
Operation Ambient Temperature Range	0°C to 85°C

Electrical Characteristics

(VIN = VOUT + 1V, VEN = VIN, CIN = COUT = 1μF, TA = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage	VIN	VIN = 2.5V to 5.5V	2.5	--	5.5	V
Dropout Voltage (Note 5)	VDROP	IOUT = 150mA	--	120	--	mV
		IOUT = 300mA	--	240	--	mV
Output voltage range	VOUT		1.2	--	3.6	V
VOUT Accuracy	ΔV	IOUT = 1mA	-2	--	+2	%
Line Regulation	ΔVLINE	VIN = (VOUT + 0.3V) to 5.5V or VIN > 2.5V, whichever is larger	--	--	0.2	%/V
Load Regulation	ΔVLOAD	1mA < IOUT < 300mA	--	--	0.6	%
Current Limit		RLOAD = 1Ω	330	450	700	mA
Quiescent Current	IQ	VEN > 1.5V	--	58	80	μA
Shutdown Current	IQ_SD	VEN < 0.4V	--	--	1	μA
EN Threshold	VIH	VIN = 2.5V to 5.5V, Power On	1.5	--	--	V
	VIL	VIN = 2.5V to 5.5V, Shutdown	--	--	0.4	
Output Voltage TC			--	100	--	ppm/°C
Thermal Shutdown	TSD		--	170	--	°C
Thermal Shutdown Hysteresis	ΔTSD		--	40	--	°C

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PSRR $I_{LOAD} = 10mA$	PSRR	f =100Hz	--	65	--	dB
		f =1kHz	--	60	--	dB
		f =10kHz	--	50	--	dB
PSRR $I_{LOAD} = 150mA$	PSRR	f =100Hz	--	65	--	dB
		f =1kHz	--	50	--	dB
		f =10kHz	--	50	--	dB
Power Good						
Reset Threshold	V_{THL}	Low Threshold, % of nominal V_{OUT2} (Flag On)	90	--	--	%
	V_{THH}	High Threshold, % of nominal V_{OUT2} (Flag Off)	--	--	96	%
POR Output Logic Low Voltage	V_{OL}	$I_{LOW} = 250\mu A$	--	0.02	0.1	V
POR Leakage Current	I_{POR}	Flag Off	-1	0.01	1	μA
Set pin Current Source		$V_{SET} = 0$	0.60	1.25	1.70	μA
Set pin Threshold		POR = high	--	1.4	--	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

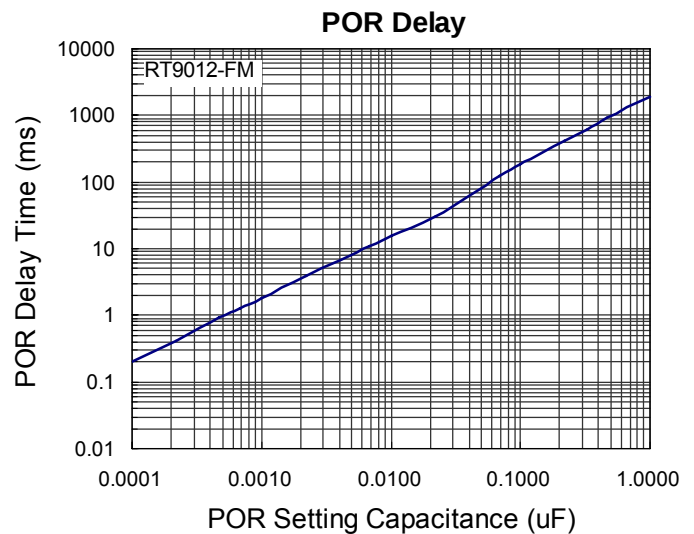
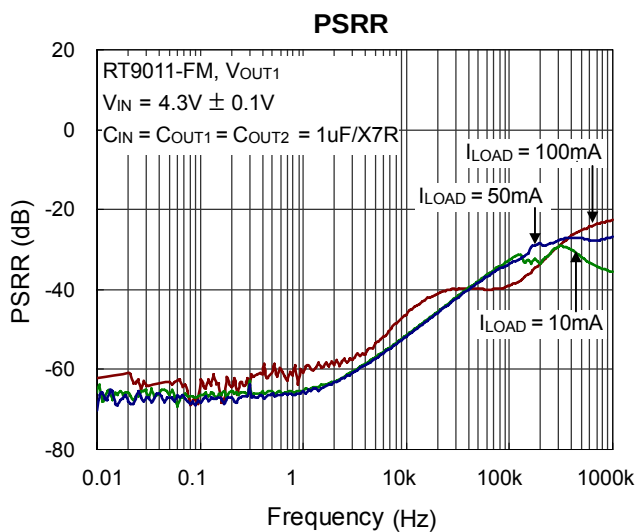
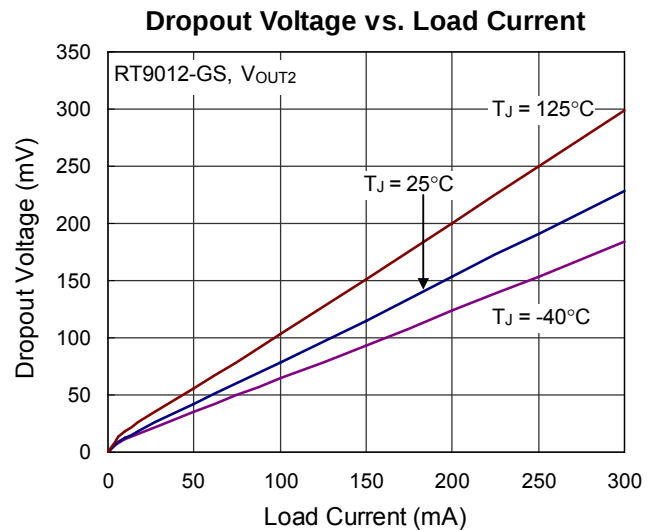
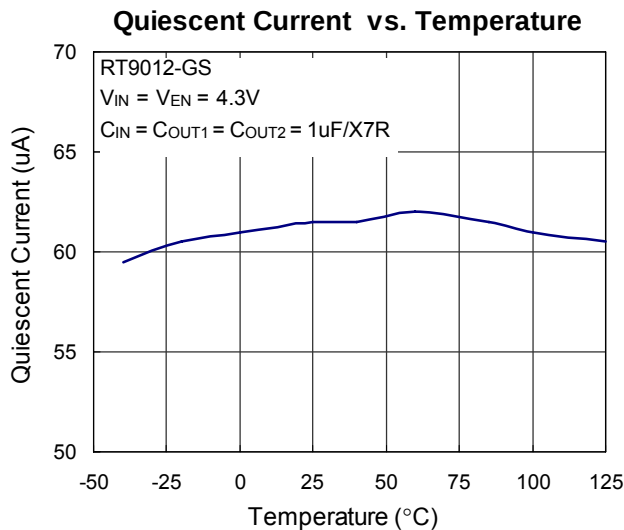
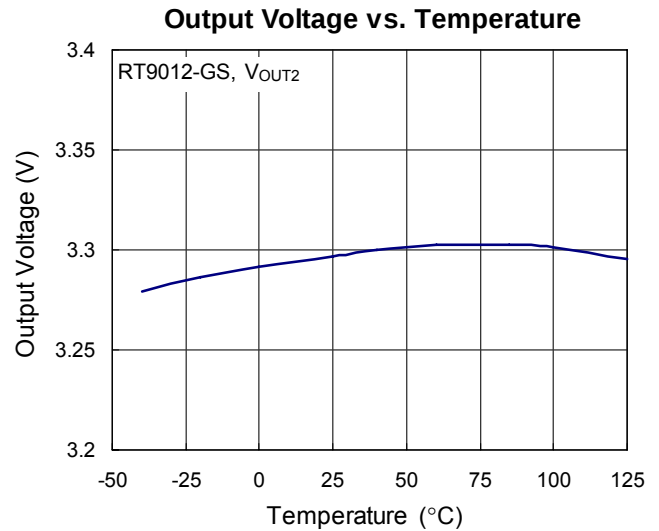
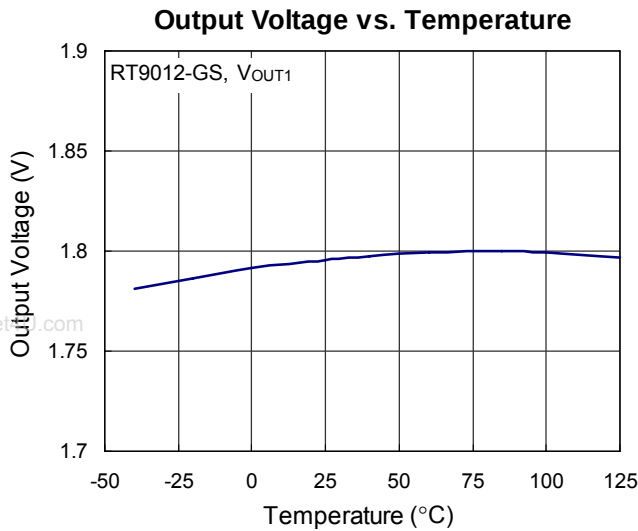
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

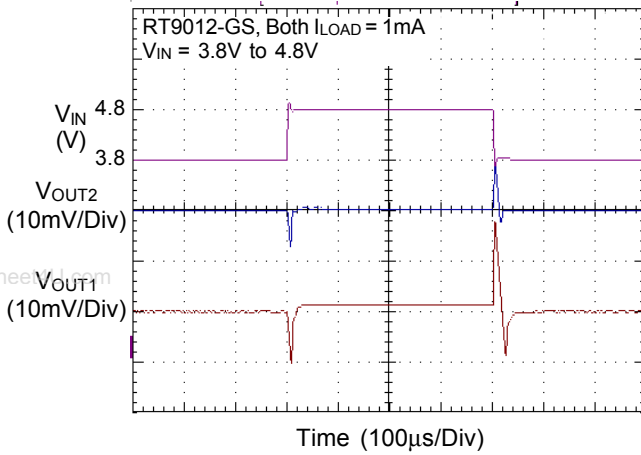
Note 4. θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 5. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)} - 100mV$.

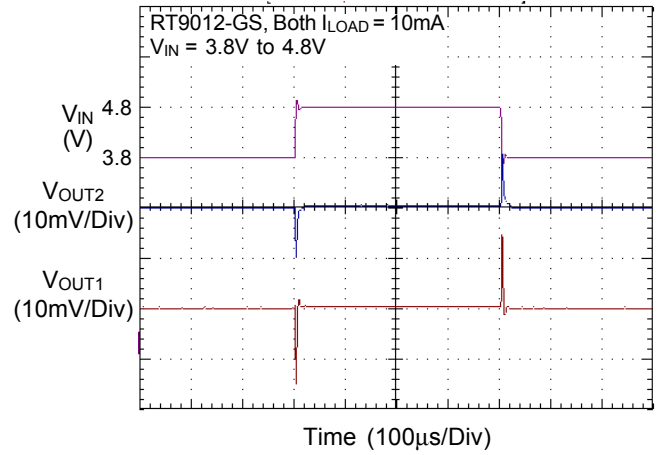
Typical Operating Characteristics



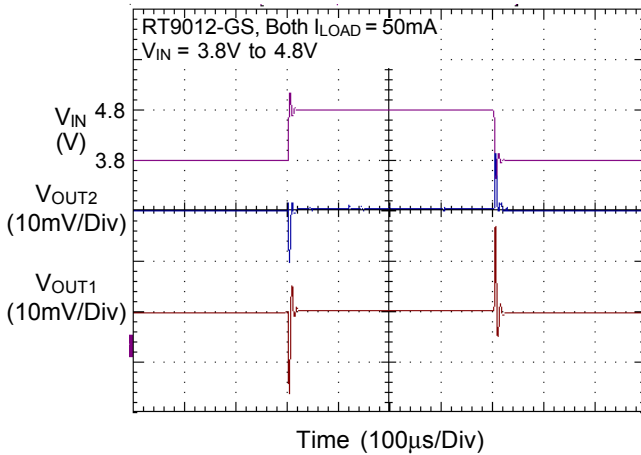
Line Transient Response



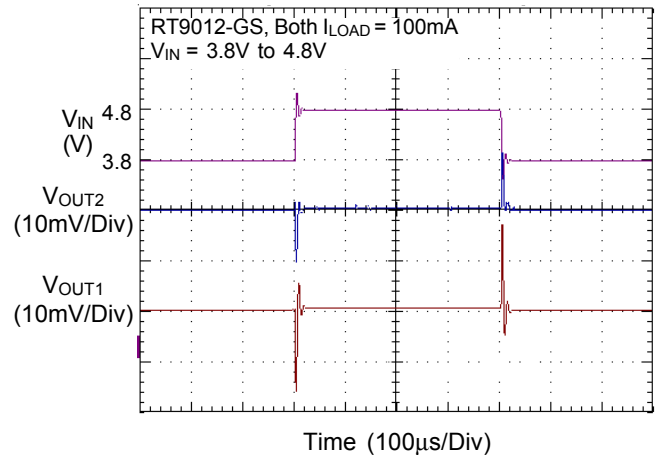
Line Transient Response



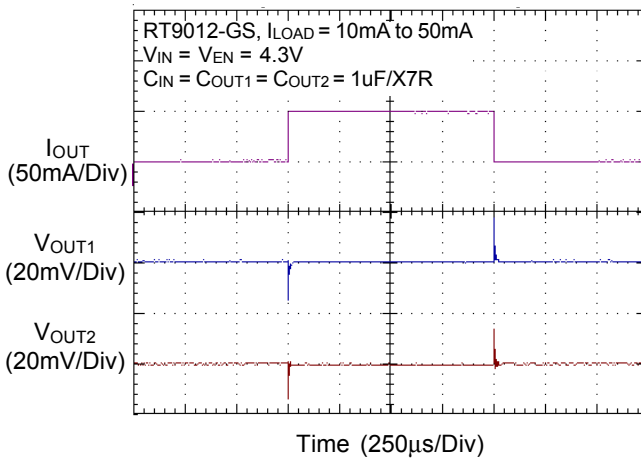
Line Transient Response



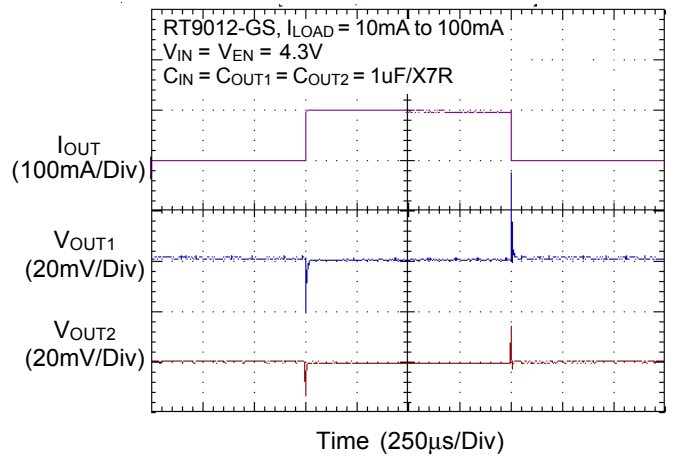
Line Transient Response



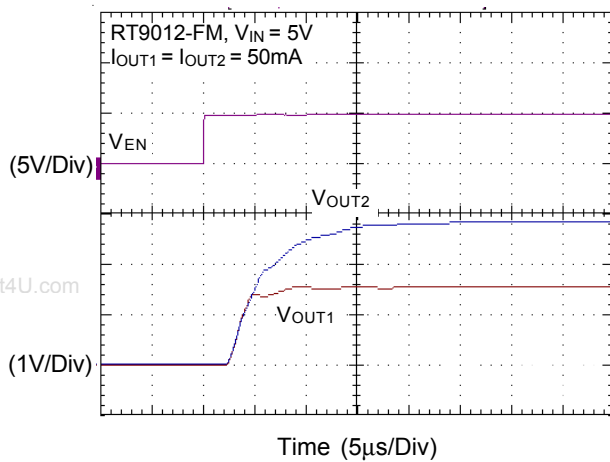
Load Transient Response



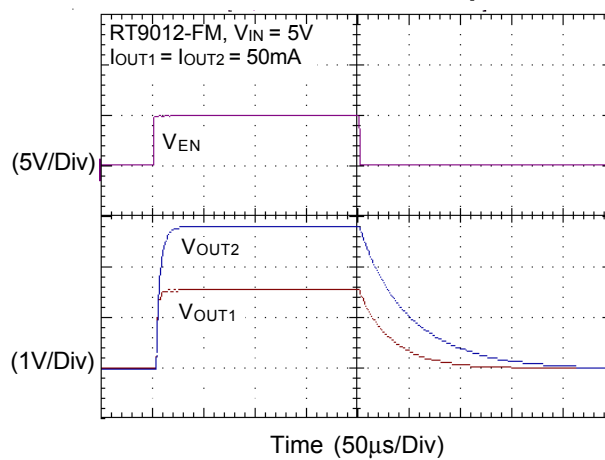
Load Transient Response



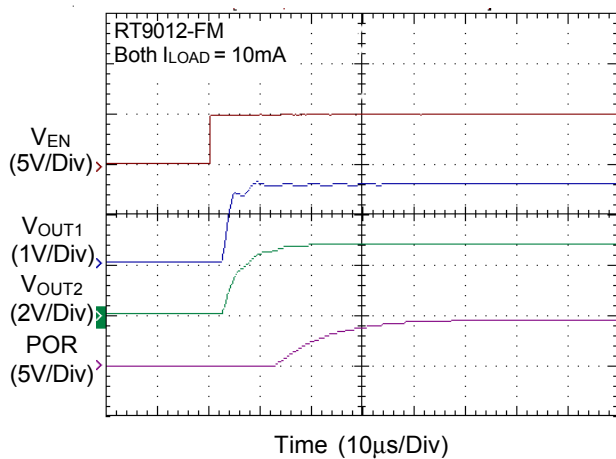
Start Up



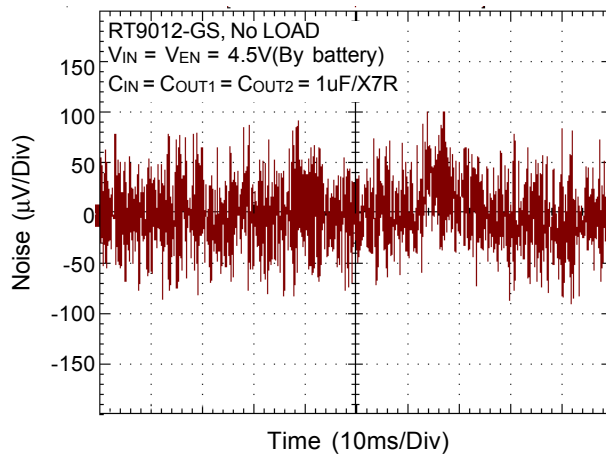
EN Pin Shutdown Response



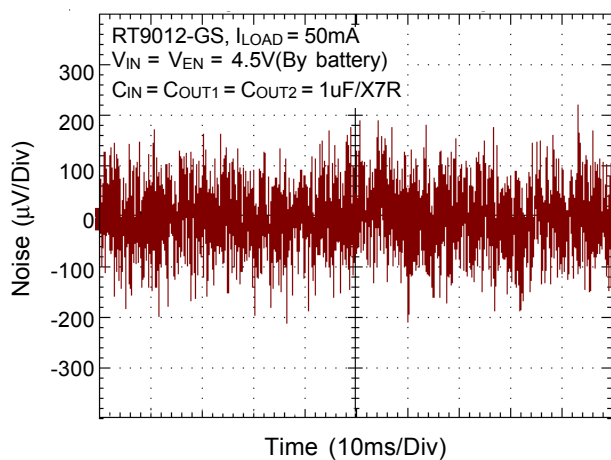
Power-On



Noise



Noise



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9012 must be carefully selected for regulator stability and performance. Using a capacitor whose value is $> 1\mu\text{F}$ on the RT9012 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9012 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ with ESR is $> 20\text{m}\Omega$ on the RT9012 output ensures stability. The RT9012 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9012 and returned to a clean analog ground.

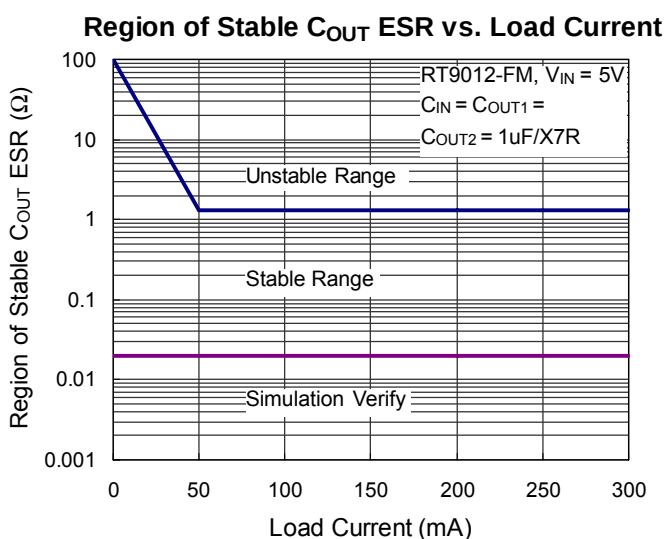


Figure 1. Stable Cout ESR Range

Thermal Considerations

Thermal protection limits power dissipation in RT9012. When the operation junction temperature exceeds 170°C , the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 40°C . RT9012 lowers its OTP trip level from 170°C to 110°C when output short circuit occurs ($V_{OUT} < 0.4\text{V}$) as shown in Figure 2. It limits IC case temperature under 100°C and provides maximum safety to customer while output short circuit occurring.

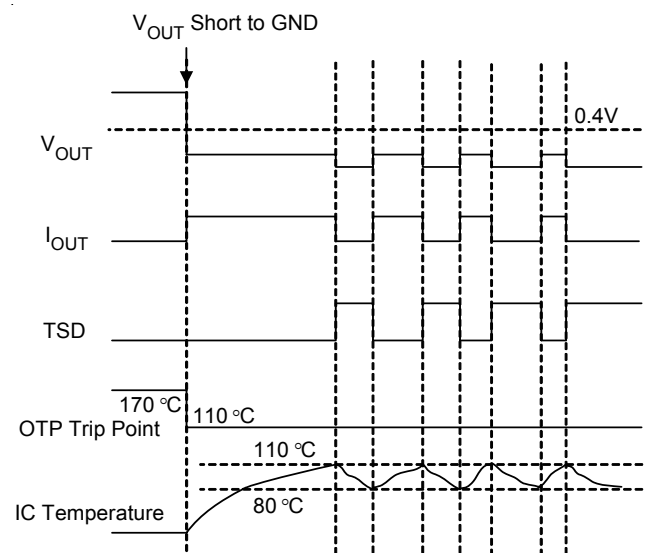


Figure 2. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C . The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9012, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the operated ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for WDFN-8L 2x2 package is 108°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A = 25^{\circ}\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^{\circ}\text{C} - 25^{\circ}\text{C}) / 108 = 0.926\text{W for WDFN-8L 2x2 packages}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT9012 packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

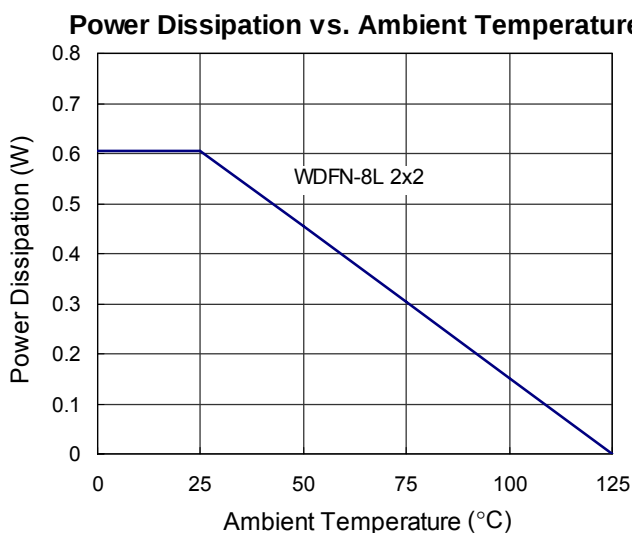
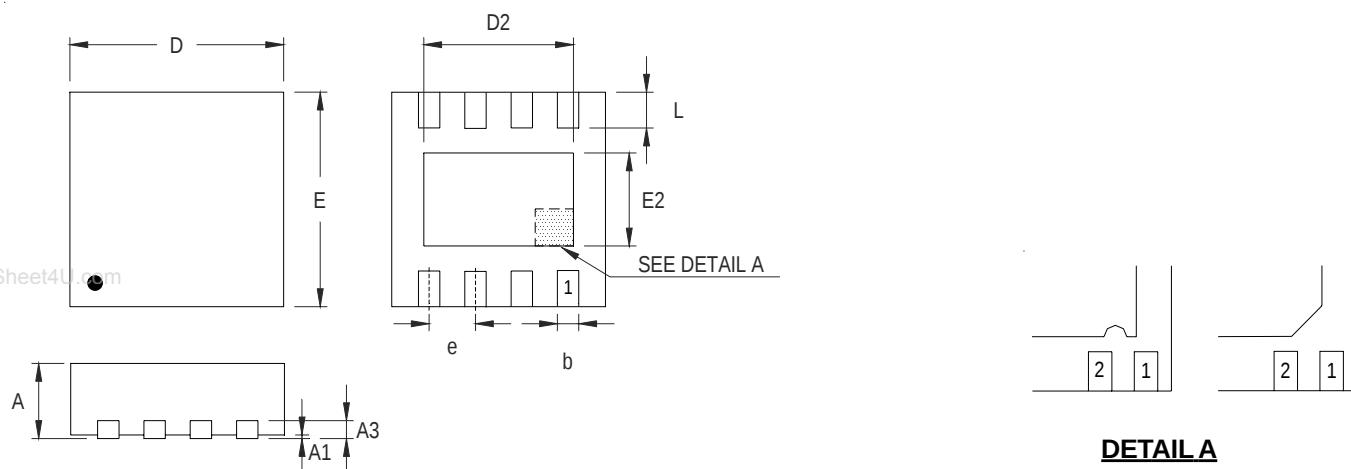


Figure 3. Derating Curves for RT9012 Packages

Outline Dimension



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

Richtek Technology Corporation

Headquarter

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)

8F, No. 137, Lane 235, Paochiao Road, Hsintien City

Taipei County, Taiwan, R.O.C.

Tel: (8862)89191466 Fax: (8862)89191465

Email: marketing@richtek.com