mosaic

Mosaic
Semiconductor
Inc.

16,777,216 bit CMOS FLASH Memory Module

Features

Fast Access Times of 150/200/250 ns.

JEDEC Ceramic Surface Mount 68 'J' Footprint

User Configurable as 32 / 16 / 8 bit wide.

Operating Power   880 / 473 / 270 mW (max.)
Standby Power 400 µW (typical).

Single High Voltage for Erase/Write : V_{PP}=12.0V±5%.

Automatic Write Verification with $\overline{DATA}$ Polling, with a byte write time of 10µs (typical).

Block Erase Capability - Block Size = 16K bytes; up to 128 blocks can be erased simultaneously.

Flash Electrical Erase of Module, 1 second (typical) and Automatic Chip/Block Erase with Status Polling.

10^4 Erase/Write Cycle Endurance minimum.

May be processed to MIL-STD-883, non-compliant.

Block Diagram
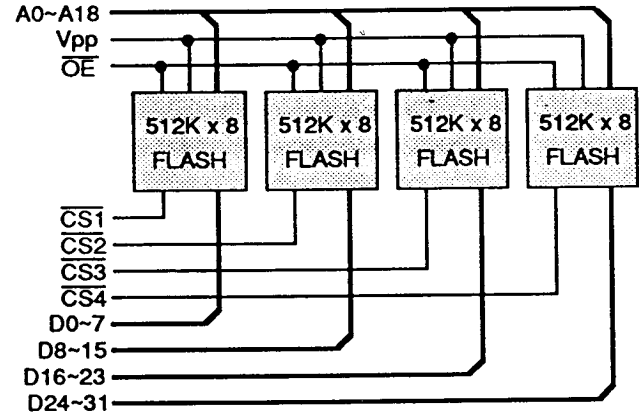
Pin Definition see also page 15.
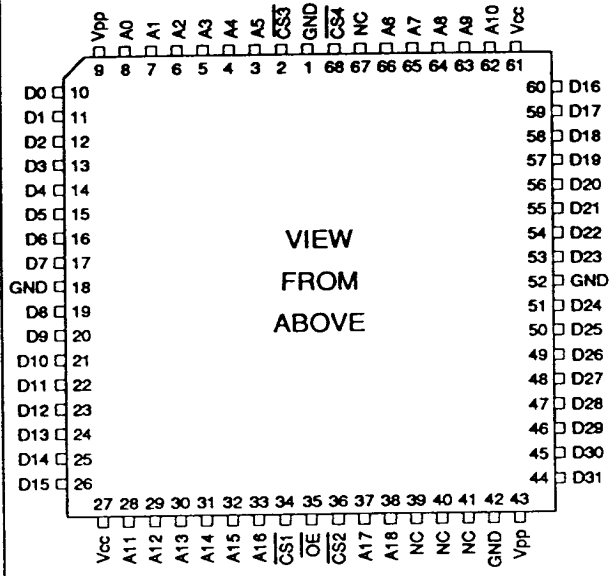
Pin Functions

A0-A18	Address Inputs
D0-D31	Data Input/Output
$\overline{CS1\text{-}4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{PP}	Write/Erase Input Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).

22.86±0.127
(0.900±0.005)
square

5.08 max
(0.200)

1.27 (0.050)
BSC

COPLANARITY ±0.06

/
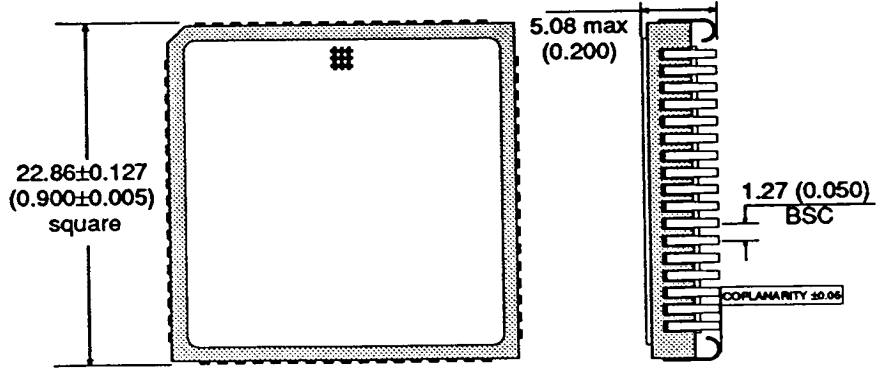
GENERAL DESCRIPTION

The PUMA 67F16000 is a 16,777,216 bit CMOS FLASH Memory which is configurable as 8, 16 or 32 bit wide output using CS1-4, allowing flexibility in a wide range of applications.

FLASH memory combines the functionality of EPROM with on-board electrical Write/Erasure. The PUMA 67F16000 utilizes devices which use a Command Register to manage these functions, allowing fixed power supply during Write/Erase and maximum EPROM compatibilty. During Write cycles, the command register internally latches address and data needed for the Write and Erase operations, thus simplifying the external control circuitry.

Programming and Erasure are both controlled by fast High Reliabilty Algorithms which are applied by the user. Alternatively, to simplify device operation, Auto-Verify Program and AutoErase are performed on-chip by the application of correct command codes to the PUMA 67F16000. The end of an automatic sequence is indicated by either Status Polling or $\overline{DATA}$ Polling on bits D7,15,23 and 31 depending on the operation being performed.

A new feature of this module is the capability of erasing blocks of 16K bytes (16,384 bytes), and between 1 and 128 blocks can be erased simultaneously. Note that Block Erasure can be either controlled externally or performed automatically as in Chip Erasure.

FLASH technology reliably stores data even after 10,000 Write/Erase cycles and utilises a single program supply of 12V±5%. Additionally, the interactive program algorithm allows a typical room temperature program time of less than 6 seconds for the entire module (in 32 bit mode). The typical module erasure time is less than 1 second.

Absolute Maximum Ratings [1]

Temperature Under Bias	T_{OPR}	-55 to +125 °C
Storage Temperature	T_{STG}	-65 to +150 °C
Voltage on Any Pin with respect to GND [2]	$V_{IN,OUT}$	-0.6 to +7.0 V
Voltage on A9 pin with respect to GND [2]	V_{ID}	-0.6 to 13.5 V
Voltage on V_{PP} pin with respect to GND	V_{PP}	-0.6 to +14.0 V
V_{CC} Supply Voltage [2]	V_{CC}	-0.6 to +7.0 V

Notes :(1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_{IN}, V_{OUT}, V_{ID} minimum = -2.0V for pulse width of less than 20 ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Programming Voltage Read	V_{PPL}	V_{CC}-1.0	-	V_{CC}	V
Write/Erase/Verify	V_{PPH}	11.4	12.0	12.6	V
Identifier Voltage	V_{ID}	11.4	12.0	12.6	V
Input High Voltage TTL	V_{IH}	2.2	-	V_{CC}+1.0	V
CMOS	V_{IHC}	V_{CC} -0.3	-	V_{CC}+0.3	V
Input Low Voltage TTL	V_{IL}	-0.3	-	0.8	V
CMOS	V_{ILC}	-0.3	-	0.3	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (-I suffix)
	T_{AI}	-55	-	125	°C (-M,-MB suffix)

Capacitance (T_A=25°C,f=1MHz)

Parameter		Symbol	Test Condition	typ	max	Unit
Input Capacitance	$\overline{CS1~4}$	C_{IN1}	V_{IN}=0V	-	16	pF
	Other pins	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	-	22	pF

Note : These parameters are calculated, not measured.

DC Electrical Characteristics (T_A=-55°C to +125°C,V_{CC}=5V ± 10%)

Parameter		Symbol	Test Condition	min	typ[2]	max	Unit
I/P Leakage Current Address, $\overline{OE}$		I_{LI1}	V_{IN}=0V to V_{CC},V_{PP}=V_{PPL} or V_{PPH}	-	-	±8	μA
	$\overline{CS1~4}$	I_{LI2}	As above	-	-	±2	μA
Output Leakage Current	32 bit	I_{LO}	V_{OUT}=0V to V_{CC}, V_{PP}=V_{PPL} or V_{PPH}, 8 bit	-	-	±2	μA
V_{PP} Current		I_{PP1}	V_{PP}=5.5V	-	-	100	μA
		I_{PP2}	V_{PP}=12.6V	-	-	100	μA
V_{CC} Read Current	32 bit	I_{CCR132}	$\overline{CS}^{(1)}$=V_{IL}, $\overline{OE}$=V_{IH}, I_{OUT}=0mA, f=1.00 MHz	-	-	160	mA
	16 bit	I_{CCR116}	As above	-	-	86	mA
	8 bit	I_{CCR18}	As above	-	-	49	mA
	32 bit	I_{CCR832}	$\overline{CS}^{(1)}$=V_{IL}, $\overline{OE}$=V_{IH}, I_{OUT}=0mA, f=6.67 MHz	-	-	400	mA
	16 bit	I_{CCR816}	As above	-	-	206	mA
	8 bit	I_{CCR88}	As above	-	-	109	mA
V_{CC} Write/Erase Current	32 bit	I_{CCE32}	$\overline{CS}^{(1)}$=V_{IL},V_{PP}=V_{PPH},Write/Erase in progress	-	-	160	mA
	16 bit	I_{CCE16}	As above	-	-	86	mA
	8 bit.	I_{CCE8}	As above	-	-	49	mA
V_{CC} Verify Current	32 bit	I_{CCA32}	$\overline{CS}$=$V_{IL}^{(1)}$,V_{PP}=V_{PPH}, Verify in progress	-	-	80	mA
	16 bit	I_{CCA16}	As above	-	-	46	mA
	8 bit	I_{CCA8}	As above	-	-	29	mA
V_{PP} Write/Erase Current	32 bit	I_{PPE32}	$\overline{CS}^{(1)}$=V_{IL},V_{PP}=V_{PPH}, Write/Erase in progress	-	-	240	mA
	16 bit	I_{PPE16}	As above	-	-	120	mA
	8 bit	I_{PPE8}	As above	-	-	60	mA
V_{PP} Verify Current	32 bit	I_{PPA32}	$\overline{CS}^{(1)}$=V_{IL},V_{PP}=V_{PPH}, Verify in progress	-	-	60	mA
	16 bit	I_{PPA16}	As above	-	-	30	mA
	8 bit	I_{PPA8}	As above	-	-	15	mA
Standby Supply Current	TTL	I_{SB1}	V_{CC}=V_{CC} max, $\overline{CS}^{(1)}$=V_{IH}	-	-	12	mA
	CMOS	I_{SB2}	V_{CC}=V_{CC} max, $\overline{CS}^{(1)}$=V_{IHC}	-	0.08	2	mA
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	-	0.45	V
Output High Voltage		V_{OH}	I_{OH}=-400μA.	2.4	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1-4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Typical figures are measured at 25°C and nominal V_{CC}

(3) Maximum active current is the sum of I_{CC} and I_{PP}.

(4) **CAUTION**: the PUMA 67F16000 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

AC Read Characteristics $(T_A = -55°C$ to $+125°C, V_{CC} = 5V \pm 10\%, V_{PP} = V_{CC})$

Parameter	Symbol	-15		-20		-25		Unit
		min	max	min	max	min	max	
Address Access Time	t_{ACC}	-	150	-	200	-	250	ns
Chip Select Access Time	t_{CE}	-	150	-	200	-	250	ns
Output Enable Access Time	t_{OE}	-	70	-	80	-	90	ns
Output Disable to Output in High Z [1]	t_{DF}	0	35	0	40	0	50	ns
Output Hold Time	t_{OH}	5	-	5	-	5	-	ns

Notes: (1) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is not 100% tested.

Read Cycle Timing Waveform
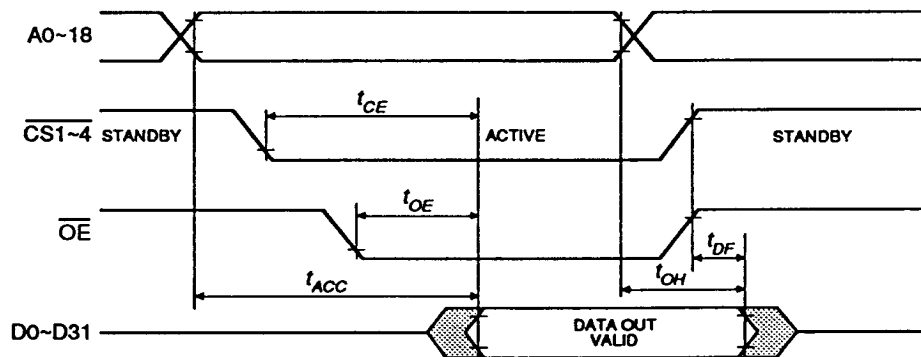
AC Write/Erase/Program Characteristics (T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, V_{PP} = 12V±5%)

| Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
V_{PP} Setup Time	t_{VPS}	100	-	100	-	100	-	ns
Output Enable Setup Time	t_{OES}	100	-	100	-	100	-	ns
Chip Select Pulse Width High	t_{CEH}	20	-	20	-	20	-	ns
Chip Select Pulse Width	t_{CEP}	50	-	50	-	50	-	ns
Address Setup Time	t_{AS}	50	-	50	-	50	-	ns
Address Hold Time	t_{AH}	10	-	10	-	10	-	ns
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns
Data Hold Time	t_{DH}	10	-	10	-	10	-	ns
Chip Select Setup before Status Polling	t_{CESP}	100	-	100	-	100	-	ns
Chip Select Setup Time	t_{CES}	0	-	0	-	0	-	ns
Chip Select Setup before Command Write	t_{CESC}	100	-	100	-	100	-	ns
Chip Select Setup before Verfiy	t_{CESV}	6	-	6	-	6	-	µs
V_{PP} Hold Time	t_{VPH}	100	-	100	-	100	-	ns
Output Disable Time [3]	t_{DF}	35	-	40	-	45	-	ns
Status Polling Access Time	t_{SPA}	-	150	-	200	-	250	ns
Verify Access Time	t_{VA}	-	150	-	200	-	250	ns
Auto Chip Erase Time	t_{AETC}	0.5	30	0.5	30	0.5	30	s
Auto Block Erase Time	t_{AETB}	0.5	30	0.5	30	0.5	30	s
Auto Verify Programming Time	t_{AVT}	10	400	10	400	10	400	µs
Standby Time before Programming	t_{PPW}	10	-	10	-	10	-	µs
Standby Time in Erase	t_{ET}	9.5	-	9.5	-	9.5	-	ms
Block Address Load Cycle	t_{BALC}	70	300	70	300	70	300	ns
Block Address Load Time	t_{BAL}	1	-	1	-	1	-	µs

Notes (1) $\overline{CS1-4}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from V_{PPL} to V_{PPH} or from V_{PPH} to V_{PPL}.

(2) Refer to Read Operation when V_{PP}=V_{PPL}.

(3) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is not 100% tested.

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input rise and fall times: ≤ 10ns.
* Input and Output timing reference levels: 0.8V and 2.0V
* Output load : see diagram.
* Module is tested in 32 bit operation using Auto modes only.
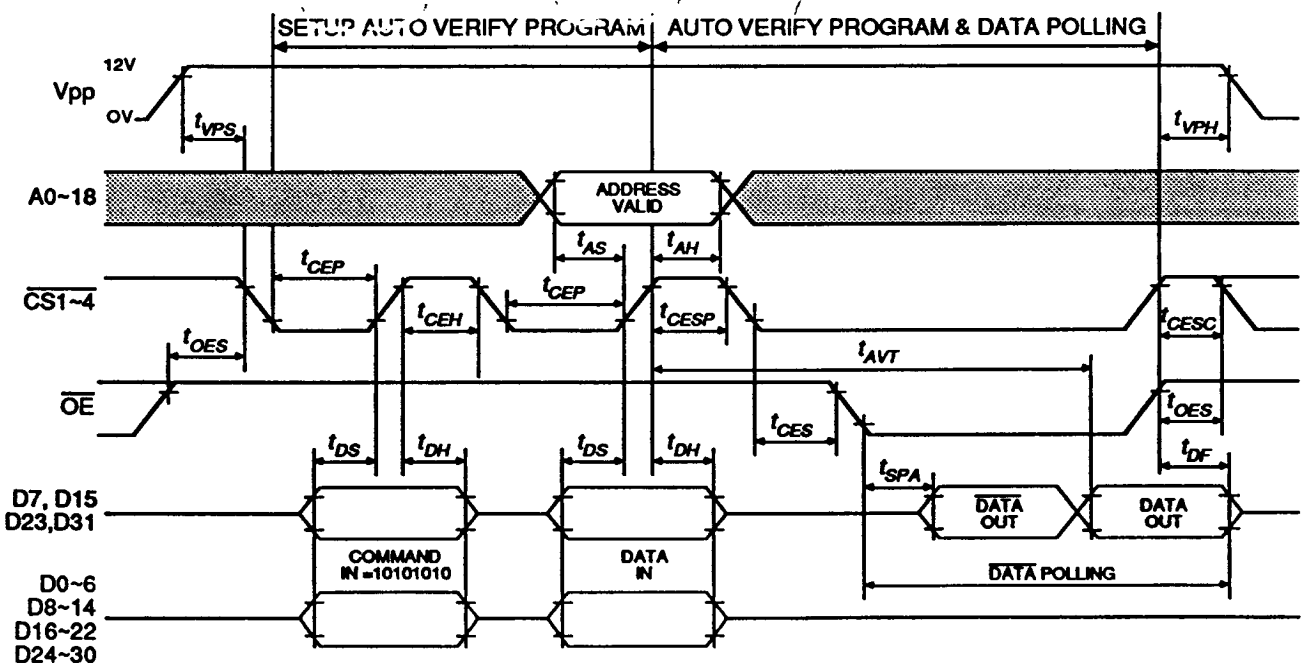
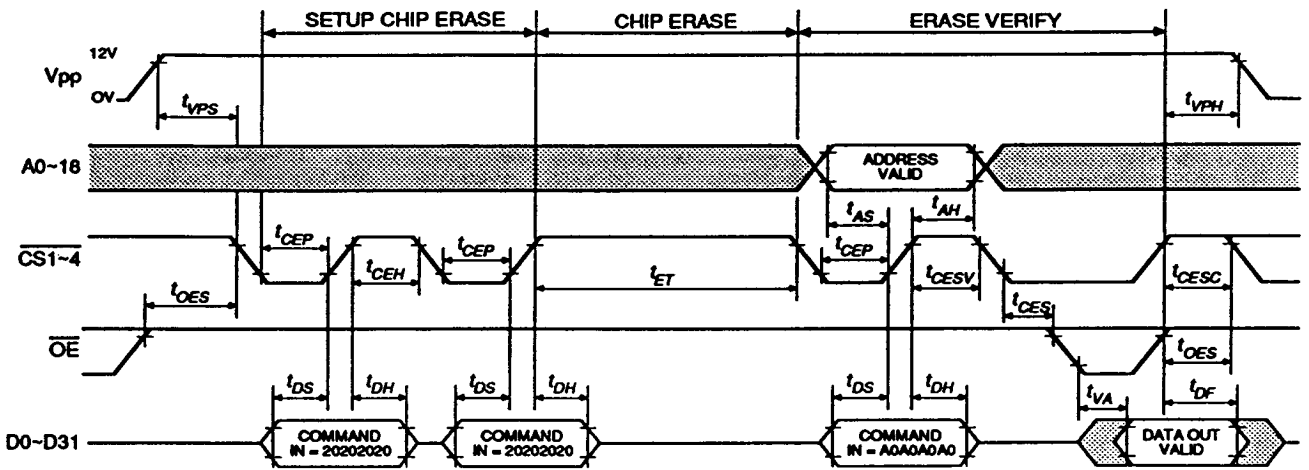## Output Load
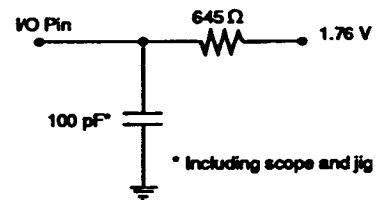
Programming Timing Waveform
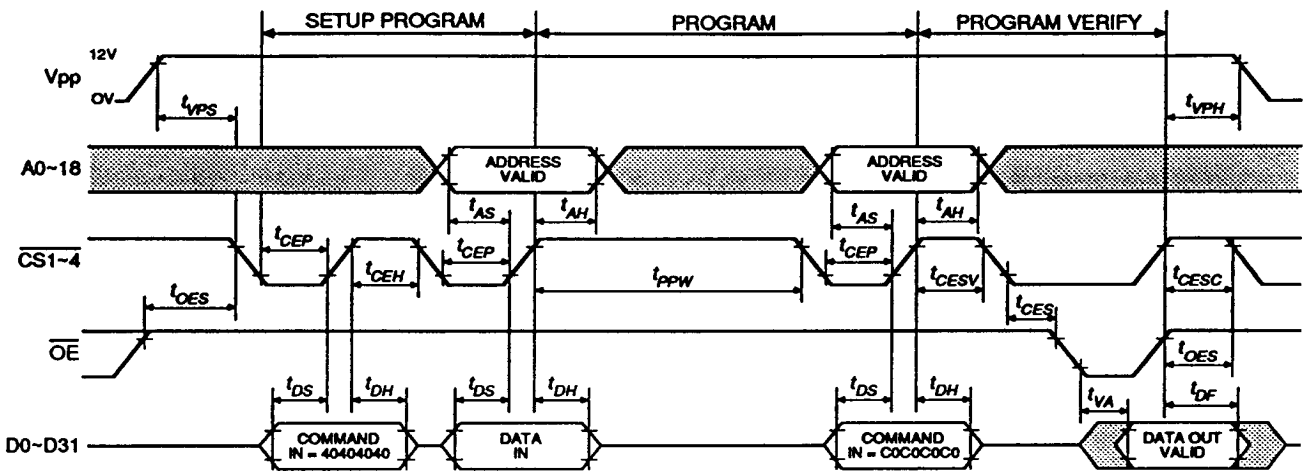
AutoVerify Programming Timing Waveform

$\overline{DATA}$ Polling allows the status of the FLASH memory to be determined. While the AutoVerify algorithm is in operation, external control is not required because the algorithm operations are executed automatically by internal control circuits. Programming completion is indicated by $\overline{DATA}$ polling on D7/D15/D23/D31 de- pending which byte is selected. While a device is busy, the inverse of the programmed data is output on the above bits, and after verification the true data appears. All of the other data bits remain in the high impedance state. The $\overline{DATA}$ Polling feature is only active during the AutoVerify Programming Mode.

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Chip Erase Timing Waveform

Automatic Chip Erase Timing Waveform

Status Polling allows the status of the FLASH memory to be determined. While the automatic Chip Erase algorithm is in operation, external control is not required because the algorithm operations are executed automatically by internal control circuits. Chip Erasure completion is indicated by Status Polling on D7/D15/D23/D31 depending which byte is selected. While a device is busy, the above bits are placed at V_{IL}, and on completion they are placed at V_{IH}. All of the other data bits remain in the high impedance state. The Status Polling feature is only active during the AutoErase Mode.

7
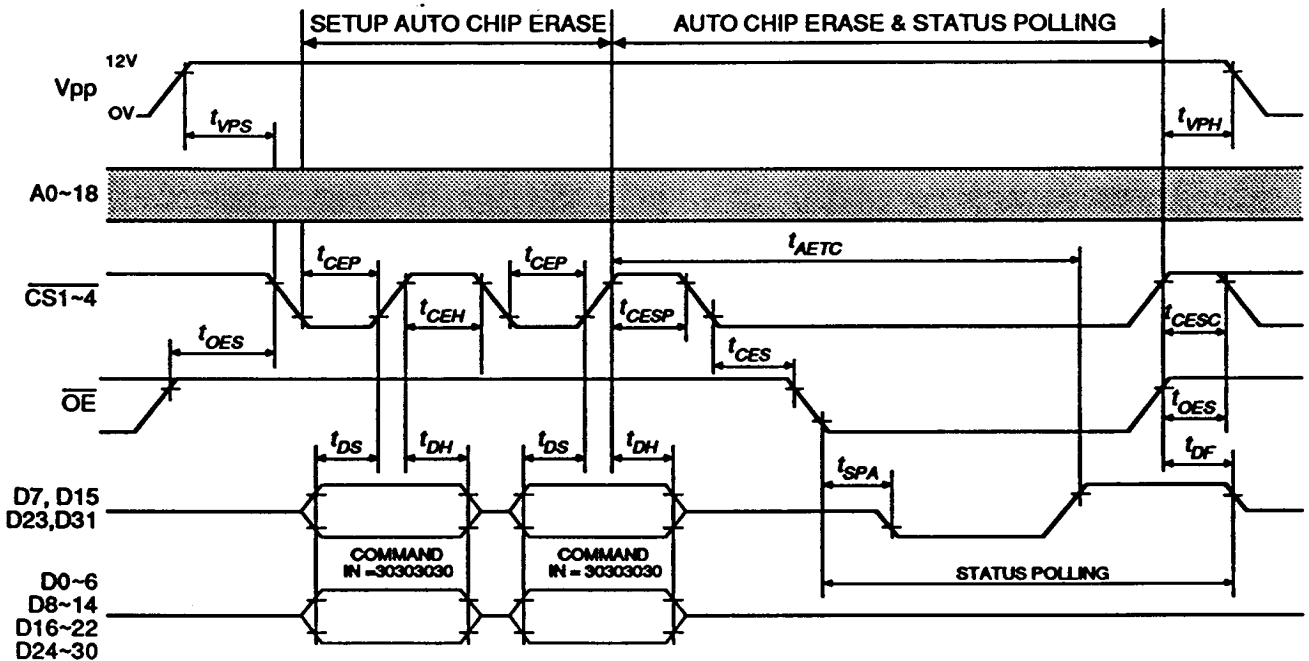
Block Erase Timing Waveform
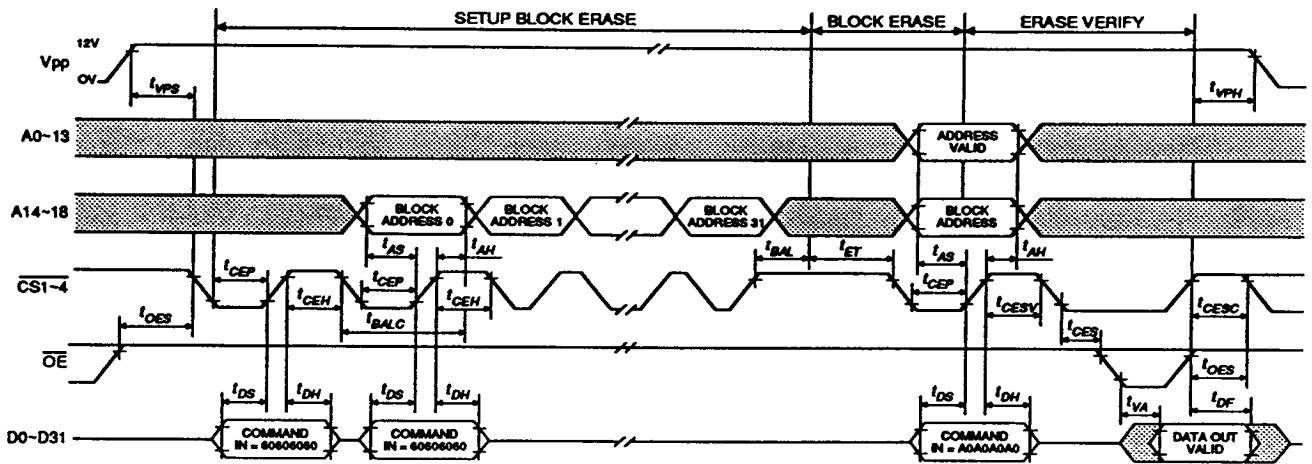
Automatic Block Erase Timing Waveform

Any Block or Blocks of 16K byte of data as indicated by A14~A18 can be Erased separately. While the Automatic Block Erase algorithm is in operation, external control is not required because the algorithm operations are executed automatically by internal control circuits. Block Erasure completion is indicated by Status Polling on D7/D15/D23/D31 depending which byte is selected. While a device is busy, the above bits are placed at V_{IL}, and on completion they are placed at V_{IH}. All of the other data bits remain in the high impedance state. The Status Polling feature is only active during the AutoErase Mode.

8

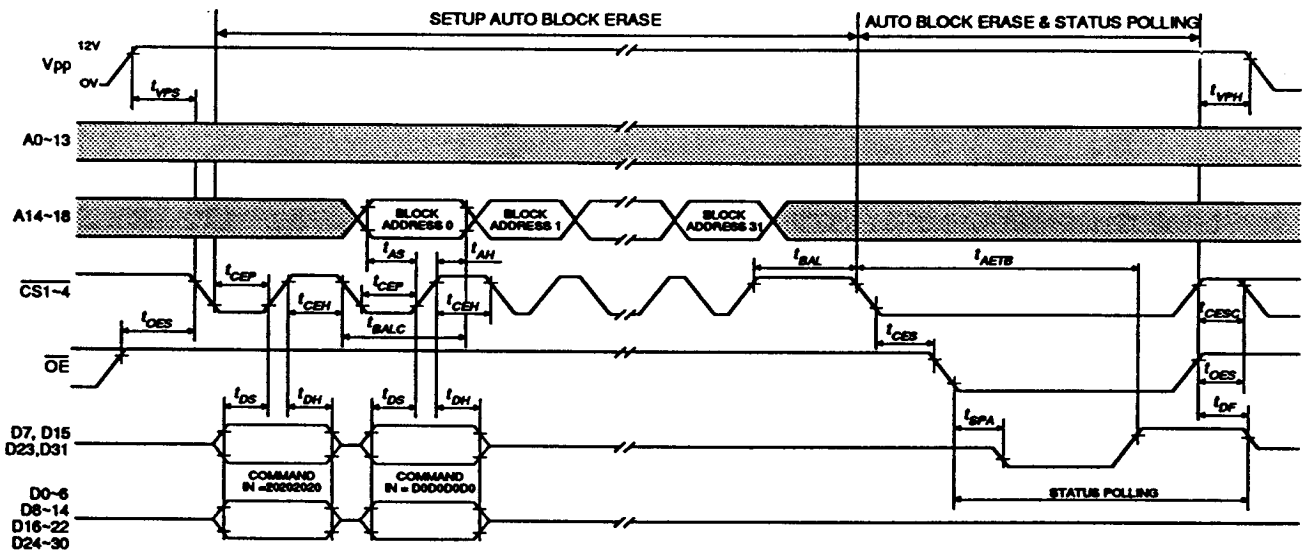## GENERAL DESCRIPTION

FLASH memory combines the functionality of EPROM with on board electrical Write/Erasure. The PUMA 67F16000 utilises a Command Register to manage these functions, allowing fixed power supply during Write Erase and maximum EPROM compatibility.

When normal TTL/CMOS logic levels are applied to the V_{PP} pin, the module displays normal EPROM Read, Standby and Output Disable. However, when high voltage (V_{PPH}) is applied to V_{PP} the Write /Erase options are available as well as the Read.

BUS OPERATIONS

Read Two control functions are provided, both of which must be logically active to obtain data at the outputs. Chip Select selects the module and controls the power, while Output Enable gates data from the output pins - see the Read Cycle Waveform for details.

Write Module Write/Erasure are accessed via the command register while V_{PP} is at V_{PPH}. Note that the register itself does not occupy an addressable memory location, but is simply a latch used to store the command and address/data information required to execute the command.

With Chip Select at V_{IL} and Output Enable at V_{IH} the command register is accessed; the command is latched on the rising edge of Chip select and the

address and data is latched on the second rising edge of Chip Select. The four most significant bits of each register (D7~D4) encode the command function while the other bits (D3~D0) must be zero. The exception to this is the Reset command when data FF_H is written to the register.

Output Disable When Output Enable is at V_{IH} the output pins are placed in a high impedance state and output from the module is disabled.

Standby If Chip Select is held at V_{IH} the power consumption of the PUMA 67F16000 is substantially reduced because most of the on-board circuitry is disabled. The outputs are placed in a high impedance state (independent of Output Enable).

If the PUMA 67F16000 module is deselected and placed in Standby mode during Write/Erase and Verify cycles, the module will continue to draw normal active current until the operation is terminated.

Identifier If a voltage $V_{ID} = 12V\pm0.5V$ is placed on address A9 while the PUMA 67F16000 is in the Read Only mode, both manufacturer and device identifiers can be output to aid user operation. While in this state, making A0 = V_{IL} outputs the manufacturer code of 07_H and A0 = V_{IH} outputs the device code of 80_H. This feature can also be accessed by the Command Register as described in the next section.

PUMA 67F16000 Operating Modes

OPERATION		Vpp	A0	A9	$\overline{CS}$	$\overline{OE}$	D0 - D7
READ ONLY	Read	V_{PPL}	A0	A9	V_{IL}	V_{IL}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	High Z
	Standby	V_{PPL}	X	X	V_{IH}	X	High Z
	Manufacturer Identifier[1]	V_{PPL}	V_{IL}	$V_{ID}^{(2)}$	V_{IL}	V_{IL}	Data = 07H
	Device Identifier[1]	V_{PPL}	V_{IH}	$V_{ID}^{(2)}$	V_{IL}	V_{IL}	Data = 80H
COMMAND PROGRAM	Read[3] [5]	V_{PPH}	A0	A9	V_{IL}	V_{IL}	Data Out
	Standby	V_{PPH}	X	X	V_{IH}	X	High Z
	Write [4]	V_{PPH}	A0	A9	V_{IL}	V_{IH}	Data In

Notes (1) Device Identifier codes can be output in command programming mode. Refer to the Command Definition Table.

(2) $11.5V \leq V_{ID} \leq 12.5V$

(3) Read operations with $V_{PP}=V_{PPH}$ may access array data or identifier codes.

(4) Refer to Command Definition table for valid Data In during a Write operation. Data is Programmed, Erased or Verified after mode setting by command inputs.

(5) Status of Automatic Chip/Block Erase and AutoVerify Program can be verified in this mode. Status and $\overline{DATA}$ polling output appears on D7, with D0-D6 in the high impedance state.

(6) X can be V_{IL} or V_{IH}.

COMMAND DEFINITIONS

With the V_{PP} pin at a low voltage the Command Register contents default to 00_H, enabling Read-only operations. A high voltage on V_{PP} enables Read/Write modes with device operation selected by writing data into the Register - see the Command Definition table for details.

Read While V_{PP} is high the memory contents can be Read by first writing 00_H into the Command Register and thereafter obeying the timings shown on the Read Cycle Waveform. This mode remains enabled until the Command Register contents are altered.

On power up the Register contents will be 00_H, ensuring that the memory contents are not changed during the V_{PP}/V_{CC} power transition. If the V_{PP} pin is hard wired to a high voltage the memory will power up enabled for Read until the Register contents are altered.

PUMA 67F16000 Command Definitions

COMMAND	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Type [1]	Addr [2]	Data [3]	Type [1]	Addr [2]	Data [3]
Read Memory [4]	1	Write	X	00_H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90_H	Read	IA	ID
Set-up Chip Erase/Chip Erase [5]	2	Write	X	20_H	Write	X	20_H
Set-up Block Erase/Block Erase [8]	2	Write	X	60_H	Write	BA	60_H
Erase Verify [5]	2	Write	EVA	$A0_H$	Read	X	EVD
Set-up Auto Chip Erase/Auto Chip Erase [6]	2	Write	X	30_H	Write	X	30_H
Set-up Auto Block Erase/Auto Block Erase [9]	2	Write	X	20_H	Write	BA	$D0_H$
Set-up Program/Program [7]	2	Write	X	40_H	Write	PA	PD
Program Verify [7]	2	Write	PVA	$C0_H$	Read	X	PVD
Set-up Auto Verify/Auto Verify [10]	2	Write	X	10_H	Write	PA	PD
Reset	1/2	Write	X	FF_H	Write [11]	X [11]	FF_H [11]

Notes (1) See Operating Modes Table.

(2) IA = Identifier address. 00000_H for Manufacturers code and 00001_H for device code.
EVA = Address of memory location to be read during Erase Verify.
PA = Address of memory location to be programmed.
PVA = Address of memory location to be verified after programming.
RA = Address of memory location to be Read.
BA = Address of memory location to be Block Erased.
Addresses are latched on the rising edge of Chip Select pulse.

(3) ID = Data read from location IA during device identification. (Manufacturer = 07_H, Device = 80_H)
EVD = Data read from location EA during Erase Verify.
PD = Data to be programmed at location PA. Data is latched on the rising edge of Chip Select.
PVD = Data to be read from location PA during Program Verify. PA is latched on the Program command.

(4) Command latch default value when applying 12.0V to V_{PP} is 00_H. Device is in Read mode after V_{PP} is set to 12.0V.

(5) All data in the chip is erased. Erasure occurs according to the Fast High Reliability Erase Flowchart

(6) All data in the chip is erased. The data is erased automatically by the internal logic circuitry, with external verification not required. Termination of erasure must be verified by Status Polling after AutoErase begins.

(7) Data is programmed according to the Fast High Reliability Programming Flowchart.

(8) The Block data as indicated by BA is erased. Data is erased according to the Fast High Reliability Block Erase Flowchart.

(9) Block data as indicated by BA is erased. The data is erased automatically by the internal logic circuitry, with external verification not required. Termination of erasure must be verified by Status Polling after AutoErase begins.

(10) One byte of data is programmed. The data is programmed automatically by the internal logic circuitry, with external verification not required. Termination of erasure must be verified by DATA Polling after AutoVerify begins.

(11) The Reset command must be written twice to exit from the Setup Program mode or the AutoVerify mode. All other modes may be exited by issuing this command once.

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Intelligent Identifier In order to use the correct programming and erase algorithms on PROM devices, these parts usually have built in codes to identify manufacturer and specific device. However, to access these codes address line A9 normally has to be placed at a high voltage, which is not considered good practice and leads to complications in PCB design.

The PUMA 67F16000 allows the identifiers to be accessed through the Command Register without placing a high voltage on A9. Writing 90_H into the Registers starts this process with a subsequent Read from 00000_H retrieving the manufacturer codes of 07_H and a Read from 00001_H giving the device codes 80_H. To terminate this sequence another valid command must be written to the Register.

Setup Program/Program Setup program is a command only operation which prepares the memories for byte programming, initiated by writing 40_H into the command register.

Once Setup Program has been performed, the next Chip Select rising edge causes data and address to be latched. Internal programming begins on this rising edge and is terminated with the next falling edge of Chip Select.

Program-Verify This module is programmed byte by byte, which can occur sequentially or at random, but the byte just written must be verified.

Writing $C0_H$ to the command registers begins this operation, which also terminates the programming operation. The last byte written will be verified; no new address information is required as the previous address is latched. A Read Cycle can now be performed in order to compare the data just written with the byte contents. This process is shown by the Programming Algorithm.

Setup AutoVerify Program/AutoVerify Program Setup AutoVerify Program is a command only operation which prepares the memories for automatic byte programming, initiated by writing 10_H into the command register.

Once Setup AutoVerify Program has been performed, the next Chip Select rising edge causes data and address to be latched. Data is programmed automatically, beginning on this edge, and the termination of this mode must be verified by DATA Polling as shown on the AutoVerify Programming Algorithm.

Setup Chip Erase/Erase Setup erase is a command only operation which prepares the memory for electrical erasure of all contents, initiated by writing 20_H to the Command Registers.

In order to start erasure 20_H must again be written to the registers; this two-step sequence ensures that accidental erasure will not occur. Additionally, if the V_{PP} pin is not at a high voltage the memory contents are protected against erasure.

Setup Block Erase/Block Erase Each of the devices used on the PUMA 67F16000 contains 512 Kbytes of memory, which is divided into 32 blocks of 16 Kbytes. Any one of these blocks may be erased individually, and more than one block simultaneously. Each block is addressed using A14~A18, with the other address lines being Don't Care, and after the block address load time ($t_{BAL} = 1\mu s$) has been exceeded the loading of the blocks to be erased is deemed to have finished.

In order to initiate this process, 60_H is written to the command registers, and to start Block Erase, 60_H must again be written to the registers, after which the blocks to be erased may be loaded. This two-step sequence ensures that accidental erasure will not occur. Additionally, if the V_{PP} pin is not at a high voltage the memory contents are protected against erasure.

Erase-Verify The Chip Erase command erases all the contents of the memory and the Block Erase command erases the contents of one or more blocks, but in either case after these operations all bytes erased must be verified. This is done by writing $A0_H$ to the Command Register, with the address of the byte to be verified supplied as it is latched on the rising edge of the Chip Select. Reading FF_H from the addressed bytes indicates that they are erased.

If the data read is not FF_H another Chip Erase or Block Erase operation must be performed. Verification can then continue from the address of the last verified byte, and once all bytes have been verified the erase procedure is complete. These processes are shown by the Chip Erase and Block Erase algorithms.

The verify operation is halted by writing another valid command into the command register.

Auto Chip Erase The Chip Erase and Chip Erase Verify processes can be performed automatically by writing 30_H into the Command register, followed by a second write of 30_H to initiate the AutoErase. Once initiated all of the locations in the PUMA 67F16000 will be set to FF_H automatically, without the need to verify each byte. Typically the whole device will be erased in 1 second, with the end of erasure being indicated by Status Polling.

Status Polling allows the status of the FLASH memory to be determined. If the PUMA 67F16000 is set to the Status Polling mode during the Chip Erase Cycle, D7

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(D15, D23, D31) is lowered to V_{OL} to indicate that the PUMA 67F16000 is performing an Chip Erase operation. When the Chip Erase has terminated, D7 (D15, D23, D31) is set to V_{IH}.

Auto Block Erase As in Auto Chip Erase, any block or blocks of memory can be automatically erased, with a block being addressed by A14~A18. The other address lines are Don't Care, and after the block address load time (t_{BAL} = 1µs) has been exceeded the loading of the blocks to be erased is deemed to have finished. Once initiated all of the locations in the selected blocks will be set to FF_H automatically, without the need to verify each byte. Typically any number of blocks will be erased in 1 second, with the end of erasure being indicated by Status Polling.

In order to initiate this process, 20_H is written to the command registers, and to start Auto Block Erase, $D0_H$ must be written to the registers, after which the selected blocks are automatically erased. This two-step sequence ensures that accidental erasure will not occur. Additionally, if the V_{PP} pin is not at a high voltage the memory contents are protected against erasure.

Reset This command will safely abort either the Erase or Program operations after the Setup commands. Two consecutive writes of FF_H are required to exit from the Setup Program or AutoVerify Program states, while only one is needed to exit from all of the other modes. Memory contents will not be altered, and a valid command must then be written to place the device in the desired state.

ALGORITHM NOTES

These algorithms **MUST BE FOLLOWED** to ensure correct and reliable device operation and are shown as flowcharts on the following pages.

Fast Programming Algorithm This programming algorithm uses pulses of 10µs duration in order to improve programming time. Each operation is followed by byte verification in order to check when the specified byte has been successfully programmed. The algorithm allows up to 20 pulses per byte, even though most bytes will verify on the first or second pulse. Both the Write and Verify sequences take place with V_{PP} = V_{PPH}. See the Programming Algorithm for a full description.

Fast Chip Erase Algorithm The Fast Chip Erase algorithm uses a closed loop flow similar to that of the Programming Algorithm to reliably and quickly erase all memory contents.

Uniform and reliable erasure is guaranteed by first writing 00_H to all memory locations. This can be accomplished using the Fast Programming algorithm. Erase

execution then proceeds with an initial Erase operation, after which Erase Verification (data = FF_H) begins at 00_H. This continues through the devices until the last address is reached or any data other than FF_H is found. With each subsequent Erase operation a greater number of bytes will verify to the erased state.

The erase time may be minimised by storing the address of the last byte verified; after the next Erase operation verification can begin at this address, circumventing the need to re-verify previously erased locations. Erasure occurs typically in 1 second.

Fast Block Erase Algorithm This algorithm is similar to the Chip Erase one, except any addressed block or blocks of 16 Kbyte can be erased. The bytes in each block must then be verified as before.

Timing Delays Four timing delays are associated with the Program and Erase algorithms described:

(1) When V_{PP} first turns on the capacitors on the V_{PP} line cause an RC ramp, the rise time of which is proportional to the number of devices being erased and the capacitance per device. V_{PP} must reach its final value 100ns before any commands are executed.

(2) The second timing delay is the erase time pulse width of 10ms, which should be timed by a microprocessor routine. This operation must be terminated by writing the Erase/Verify Command; if this command is not issued the memory cells may be driven into depletion.

(3) Each programming operation lasts 10µs, and since the algorithm is interactive each byte is verified after a Write pulse; the program operation must be terminated at the conclusion of the timing routine.

(4) In order to improve memory cell operation, an internally generated margin voltage is applied to the addressed cell during Write/Erase Verify. It is during this 6µs delay that the internal circuitry is changing voltage levels between the Erase/Write level and those used for Verify and Read operations. Any attempt to Read the device(s) during this period will result in possible false data appearing on the outputs.

Parallel Erase If the PUMA 67F16000 is used in 32 /16 bit mode then 2/4 devices will be accessed at the same time. This reduces the Erase time, but because individual devices will erase at different rates care must be taken that each is verified separately. When a Chip or Block is completely erased and verified a masking code should be used to prevent further erasure e.g. writing the Read Command to the appropriate device. Other devices will continue to Erase until verified.

FAST PROGRAMMING ALGORITHM

This algorithm **MUST BE FOLLOWED** to ensure proper and reliable operation, and is shown for a single device only.

FAST CHIP ERASE ALGORITHM

This algorithm **MUST BE FOLLOWED** to ensure proper and reliable operation, and is shown for a single device only.

FAST PROGRAMMING ALGORITHM flowchart:

START PROGRAM → APPLY V_{PPH} → ADDRESS = 0 → $n = 0$ → $n = n + 1$ → WRITE SET-UP PROGRAM COMMAND → WRITE PROGRAM COMMAND → TIME OUT 10 μs → WRITE PROGRAM VERIFY COMMAND → TIME OUT 6 μs → VERIFY DATA

VERIFY DATA — NO → IS $n = 20$? — NO → (back to WRITE SET-UP PROGRAM COMMAND); IS $n = 20$? — YES → APPLY V_{PPL} → ERROR

VERIFY DATA — YES → LAST ADDRESS ? — NO → INCREMENT ADDRESS → (back to $n = 0$); LAST ADDRESS ? — YES → APPLY V_{PPL} → END

FAST CHIP ERASE ALGORITHM flowchart:

START ERASE → PROGRAM ALL BITS TO "0" → APPLY V_{PPH} → $n = 0$ → $n = n + 1$ → WRITE SET-UP CHIP ERASE COMMAND → WRITE CHIP ERASE COMMAND → TIME OUT 10 ms → ADDRESS = 0 → WRITE ERASE VERIFY COMMAND → TIME OUT 6 μs → VERIFY DATA

VERIFY DATA — NO → IS $n = 3000$? — NO → (back to $n = n + 1$); IS $n = 3000$? — YES → APPLY V_{PPL} → ERROR

VERIFY DATA — YES → LAST ADDRESS ? — NO → INCREMENT ADDRESS → (back to WRITE ERASE VERIFY COMMAND); LAST ADDRESS ? — YES → APPLY V_{PPL} → END

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FAST BLOCK ERASE ALGORITHM
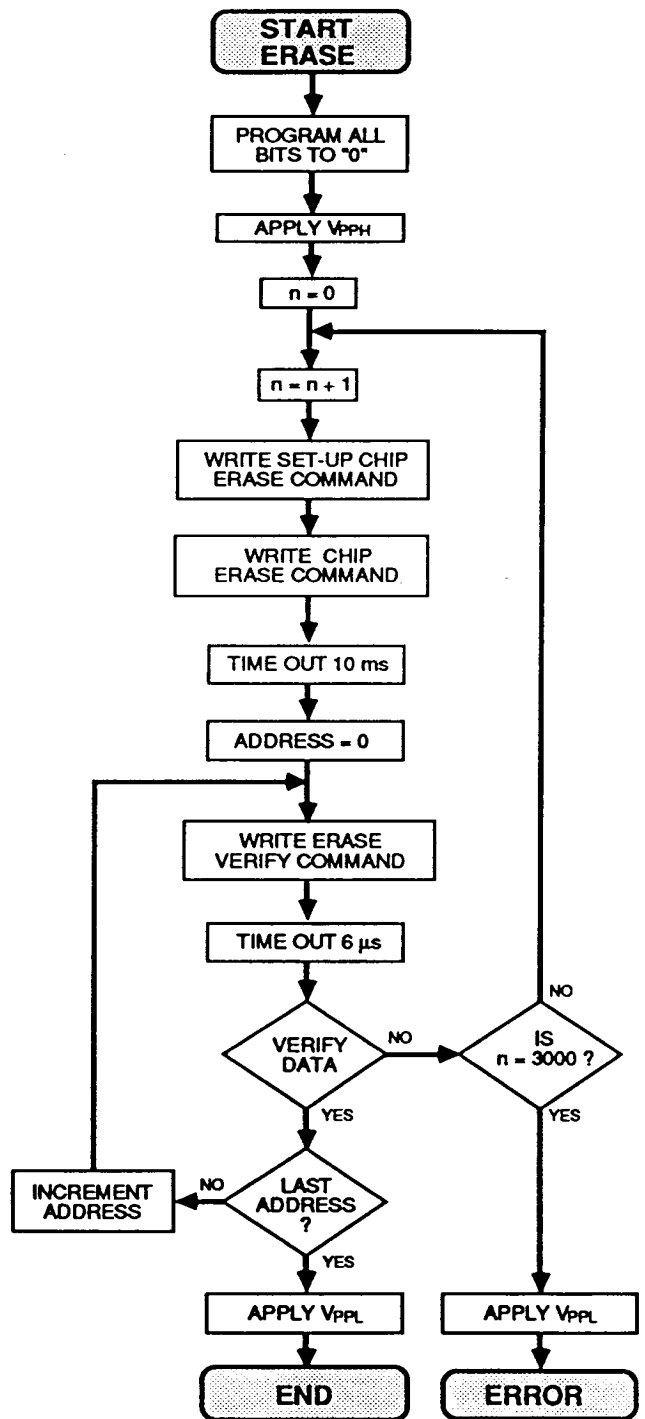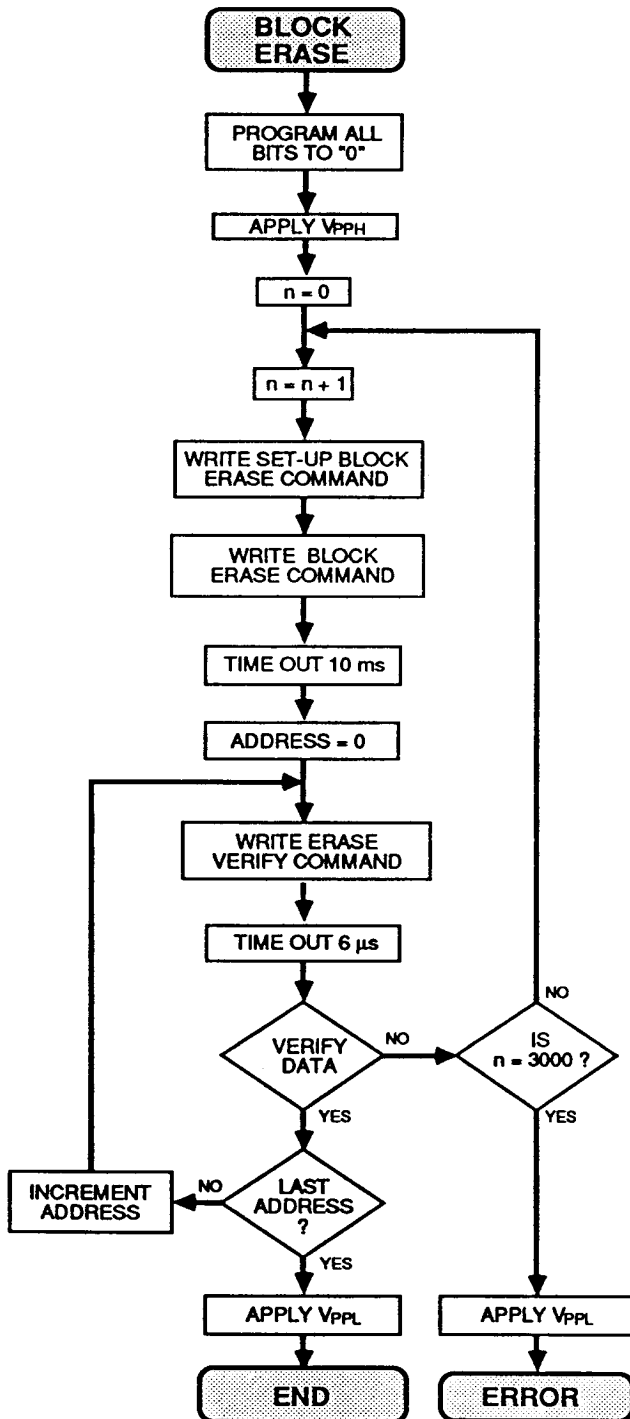
This algorithm **MUST BE FOLLOWED** to ensure proper and reliable operation, and is shown for a single device only.

```
                    BLOCK
                    ERASE
                      |
                      v
              PROGRAM ALL
              BITS TO "0"
                      |
                      v
               APPLY VPPH
                      |
                      v
                   n = 0
                      |
                      v  <--------------+
                  n = n + 1             |
                      |                 |
                      v                 |
             WRITE SET-UP BLOCK         |
             ERASE COMMAND              |
                      |                 |
                      v                 |
               WRITE BLOCK              |
               ERASE COMMAND            |
                      |                 |
                      v                 |
              TIME OUT 10 ms            |
                      |                 |
                      v                 |
               ADDRESS = 0              |
                      |                 |
    +---------------->|                 |
    |                 v                 |
    |          WRITE ERASE              |
    |          VERIFY COMMAND           |
    |                 |                 |
    |                 v                 |
    |           TIME OUT 6 µs           |
    |                 |                 |
    |                 v          NO     |
    |           / VERIFY \  NO  / IS  \ |
    |          <  DATA    >--->< n =   >+
    |           \       /      \ 3000?/
    |             | YES          | YES
    |             v              |
    | NO    / LAST    \          |
 INCREMENT< ADDRESS   >          |
 ADDRESS   \   ?     /           |
    ^         | YES              |
    |         v                  v
    |    APPLY VPPL         APPLY VPPL
    |         |                  |
    |         v                  v
    |        END               ERROR
```

DESIGN CONSIDERATIONS

Two Line Control Two Read signals are provided for output control to accommodate large memory arrays, giving the lowest possible memory power dissipation and ensuring bus contention does not occur.

Supply Decoupling Flash memory power-switching characteristics require careful decoupling. Three supply current issues have to be considered - Standby, Active and transient current peaks caused by rising and falling edges of Chip Select.

Two line control and correct decoupling capacitor selection will help to suppress these transient voltage peaks. Each PUMA 67F16000 device should have a $0.1\mu F$ ceramic capacitor between V_{cc} and GND and between V_{pp} and GND. These high frequency, low inductance capacitors should be placed as close as possible to the PUMA 67F16000.

Additionally, it is recommended that a $4.7\mu F$ electrolytic capacitor should be placed between V_{cc} and GND every eight PUMA 67F16000 devices. This capacitor will smooth out voltage dips in the supply caused by PCB track inductance and will supply charge to the on-board capacitors as needed.
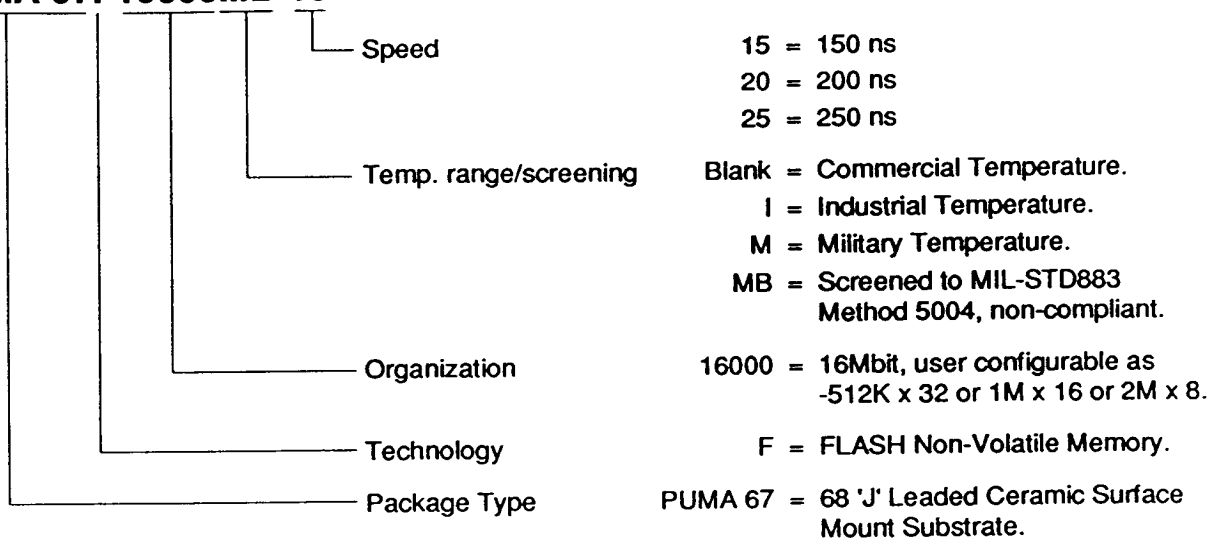
V_{pp} Trace Because Flash memories are designed to be programmed in situ, the PCB designer must be made aware of the V_{pp} supply trace. This should be made similar to the V_{cc} bus as the V_{pp} pin supplies the memory cell current for Programming and Erase.

Power Up/Down FLASH memories are protected against accidental Erasure or Programming during power transitions. At power up, these devices do not care which supply, V_{pp} or V_{cc} is active first; power supply sequencing is not required.

System designers must guard against active writes for supply voltages above V_{cc} (min) when V_{pp} is active. Since Chip Select must be low and Output Enable must be high for a Command Register access, placing Chip select high or Output Enable low will inhibit writes. Additionally, the two step command sequence required to activate writes provides further protection.

Ordering Information

PUMA 67F16000MB-15

Speed   15 = 150 ns
20 = 200 ns
25 = 250 ns

Temp. range/screening   Blank = Commercial Temperature.
I = Industrial Temperature.
M = Military Temperature.
MB = Screened to MIL-STD883
Method 5004, non-compliant.

Organization   16000 = 16Mbit, user configurable as
-512K x 32 or 1M x 16 or 2M x 8.

Technology   F = FLASH Non-Volatile Memory.

Package Type   PUMA 67 = 68 'J' Leaded Ceramic Surface
Mount Substrate.

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7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
271 6058

032038