T-46-23-12

P4C164/P4C164L
ULTRA HIGH SPEED 8K x 8 STATIC CMOS RAMS (SCRAMS)

2

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 15/17/20/25/30/35 ns (Commercial)
  - 20/25/30/35/45 ns (Military)
- Low Power Operation (Commercial/Military)
  - 690 mW Active – 15,17
  - 605/715 mW Active – 20
  - 495/575 mW Active – 25, 30, 35, 45
  - 116/127 mW Standby (TTL Input)
  - 1.1 mW Standby (CMOS Input) P4C164L
- Output Enable and Dual Chip Enable Control Functions
- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply, 10 µA Typical Current
- Common Data I/O
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE II Technology™
- Standard Pinout (JEDEC Approved)
  - 28-Pin 300 mil DIP, SOJ
  - 28-Pin 600 mil ceramic DIP
  - 28-Pin 350 x 550 mil LCC

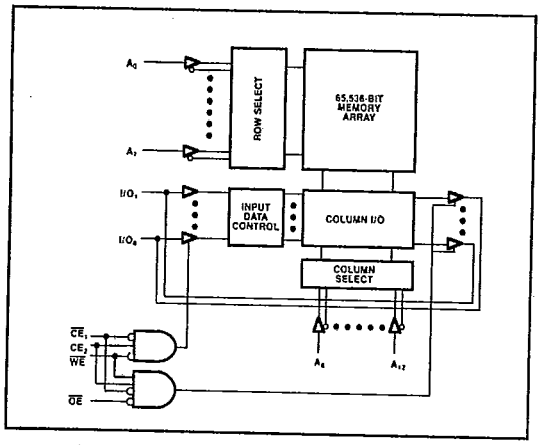
DESCRIPTION

The P4C164 and P4C164L are 65,536-bit ultra high-speed static RAMs organized as 8K x 8. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained with supply voltages down to 2.0V. Current drain is typically 10 µA from a 2.0V supply.

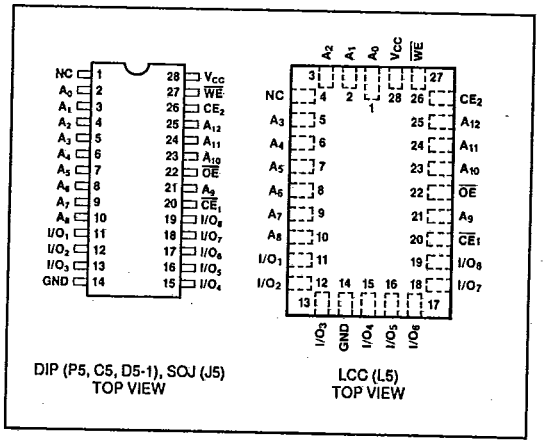
Access times as fast as 15 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low 690 mW active, 116 mW standby. In full standby mode with CMOS inputs, power consumption is only 1.1 mW for the P4C164L. The P4C164 and P4C164L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies. The P4C164 and P4C164L are manufactured with PACE II Technology™.

The P4C164 and P4C164L are available in 28-pin 300 mil DIP and SOJ, 28-pin 600 mil ceramic DIP, and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P5, C5, D5-1), SOJ (J5)
TOP VIEW

LCC (L5)
TOP VIEW

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

1519 Tbl 01

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1519 Tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Military	–55 to +125°C	0V	5.0V ± 10%

1519 Tbl 03

Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

1519 Tbl 04

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C164		P4C164L		Unit
				Min	Max	Min	Max	
V_{IH}	Input High Voltage			2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage			–0.5[3]	0.8	–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC}–0.2	V_{CC}+0.5	V_{CC}–0.2	V_{CC}+0.5	V
V_{LC}	CMOS Input Low Voltage			–0.5[3]	0.2	–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.2		–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +10 mA, V_{CC} = Min. I_{OL} = +8 mA, V_{CC} = Min.			0.5 0.4		0.5 0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.			0.2		0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.		2.4		2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = –100 µA, V_{CC} = Min.		V_{CC}–0.2		V_{CC}–0.2		V
I_{LI}	Input Leakage Current	V_{CC} = Max. V_{IN} = GND to V_{CC}	Mil. Com'l.	–10 –5	+10 +5	–5 –2	+5 +2	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Mil. Com'l.	–10 –5	+10 +5	–5 –2	+5 +2	µA

1519 Tbl 05

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF

1519 Tbl 06

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

1519 Tbl 07

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

T-46-23-12

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C164 Min	P4C164 Max	P4C164L Min	P4C164L Max	Unit
I_{CC}	Dynamic Operating Current – 15, 17	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	n/a	—	n/a	mA
			Com'l.	—	125	—	n/a	
I_{CC}	Dynamic Operating Current – 20	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	130	—	130	mA
			Com'l.	—	110	—	110	
I_{CC}	Dynamic Operating Current – 25, 30, 35, 45	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	105	—	105	mA
			Com'l.	—	90	—	90	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, V_{CC} = Max., f = Max., Outputs Open	Mil.	—	23	—	23	mA
			Com'l.	—	21	—	21	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1 \geq V_{HC}$ or $CE_2 \leq V_{LC}$, V_{CC} = Max., f = 0, Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil.	—	18	—	1	mA
			Com'l.	—	17	—	0.2	

n/a = Not Applicable

1519 Tbl 08

DATA RETENTION CHARACTERISTICS (P4C164L Only)

Symbol	Parameter	Test Condition	Min	Typ.* V_{CC}= 2.0V	Typ.* V_{CC}= 3.0V	Max V_{CC}= 2.0V	Max V_{CC}= 3.0V	Unit
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	Mil.		10	15	200	300	µA
		Com'l.		10	15	60	90	µA
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

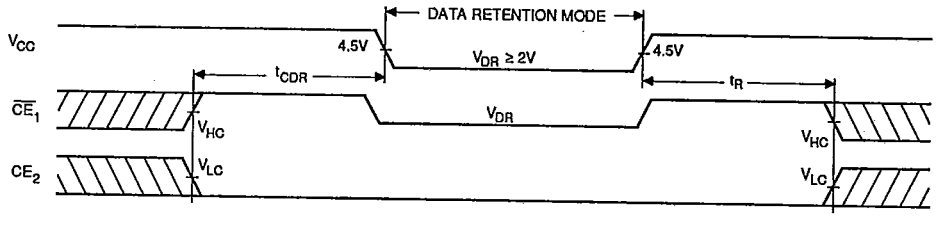
*T_A = +25°C

§t_{RC} = Read Cycle Time

†This parameter is guaranteed but not tested.

1519 Tbl 09

DATA RETENTION WAVEFORM



1519 01

T-46-23-12

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

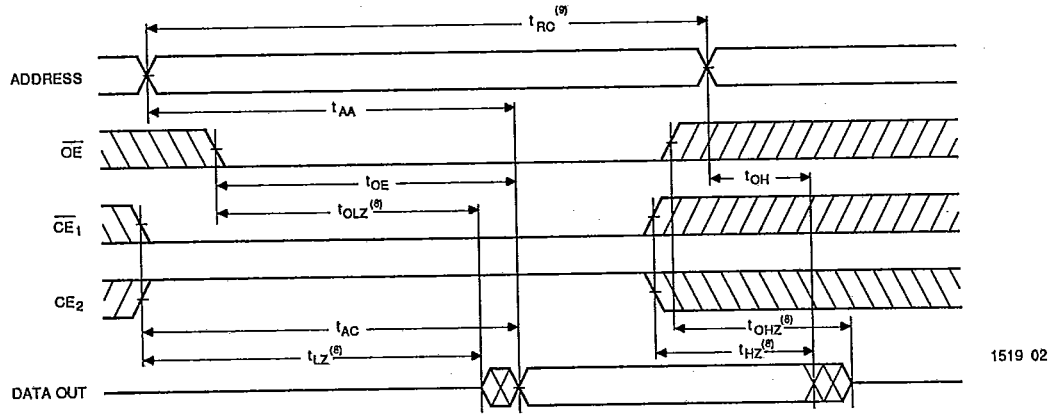
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-15*		-17		-20		-25		-30		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		17		20		25		30		35		45		ns
t_{AA}	Address Access Time		15		17		20		25		30		35		45	ns
t_{AC}	Chip Enable Access Time		15		17		20		25		30		35		45	ns
t_{OH}	Output Hold from Address Change	2		2		2		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		8		8		8		10		13		15		20	ns
t_{OE}	Output Enable Low to Data Valid		9		10		10		13		15		18		20	ns
t_{OLZ}	Output Enable Low to Low Z	2		2		2		3		3		3		3		ns
t_{OHZ}	Output Enable High to High Z		9		9		9		12		14		15		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		15		17		20		20		20		20		25	ns

1519 Tbl 10

*V_{CC} = 5V ± 5% for -15

READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED) [5]

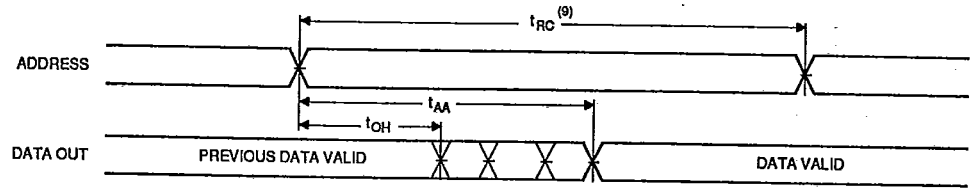


1519 02

Notes:
5. $\overline{WE}$ is high for READ cycle.
6. $\overline{CE_1}$ is low, CE_2 is high and $\overline{OE}$ is low for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE_1}$ transition low and CE_2 transition high.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

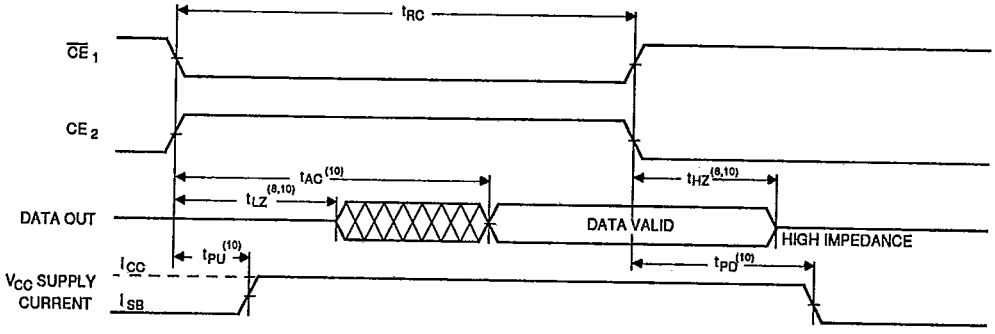
T-46-23-12

READ CYCLE NO. 2 (ADDRESS CONTROLLED) [5,6]



1519 03

READ CYCLE NO. 3 ($\overline{CE}_1$, CE_2 CONTROLLED) [5,7,10]



1519 04

Notes:

9. READ Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

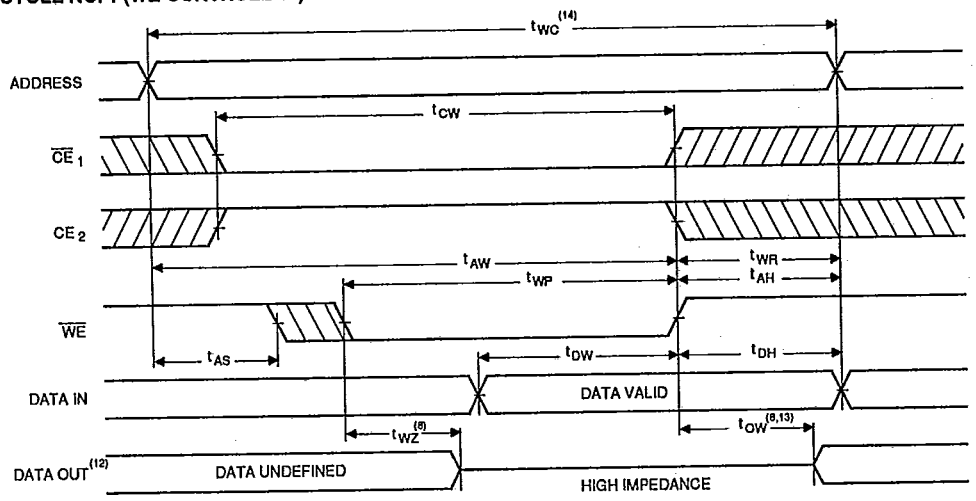
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-15*		-17		-20		-25		-30		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		17		20		25		30		35		45		ns
t_{CW}	Chip Enable Time to End of Write	12		13		15		18		22		25		33		ns
t_{AW}	Address Valid to End of Write	12		13		15		18		22		25		33		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	12		13		15		18		20		20		25		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		0		ns
t_{WR}	Write Recovery Time	0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	9		10		11		13		15		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		7		8		10		12		14		18	ns
t_{OW}	Output Active from End of Write	3		3		3		3		5		5		5		ns

*V_{CC} = 5V ± 5% for -15

1519 Tbl 11

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) [11]



1519 05

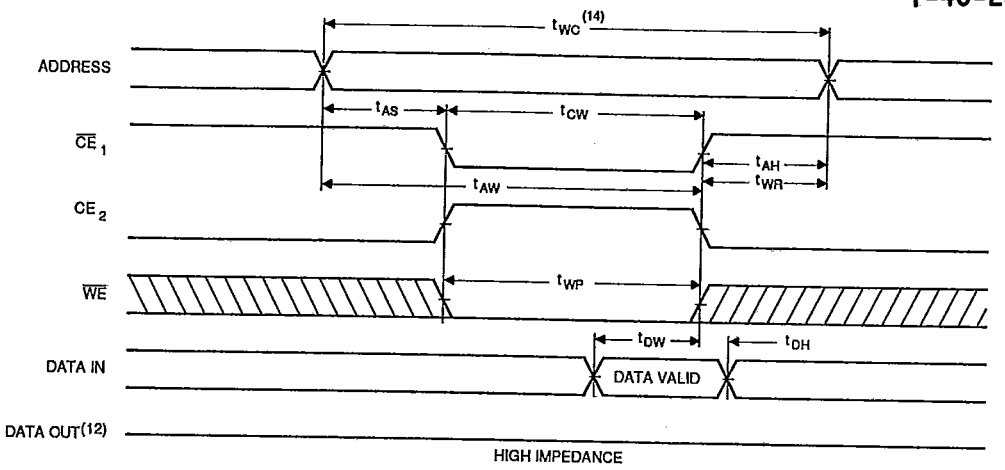
Notes:

11. $\overline{CE}_1$ and $\overline{WE}$ must be low, and CE_2 high for WRITE cycle.
12. $\overline{OE}$ is low for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE}_1$ goes high, or CE_2 goes low, simultaneously with $\overline{WE}$ high, the output remains in a low impedance state
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

T-46-23-12

2

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (11)



1519 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

1519 Tbl 12

TRUTH TABLE

Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

1519 Tbl 13

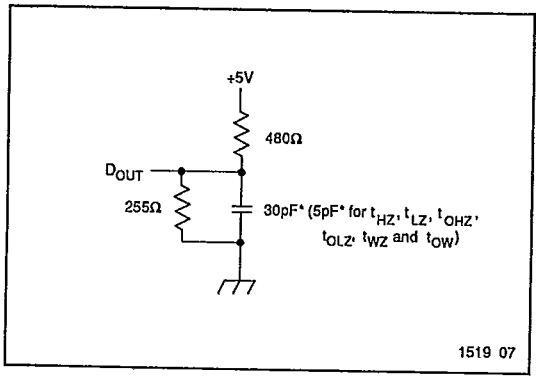


Figure 1. Output Load

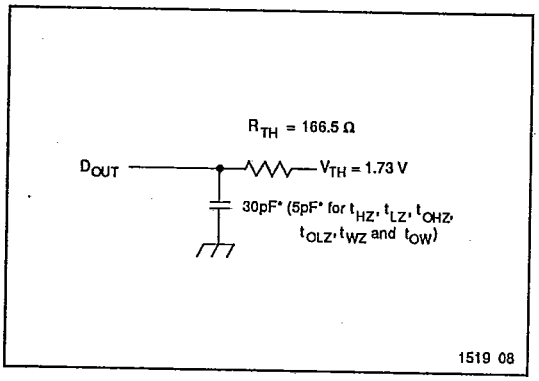


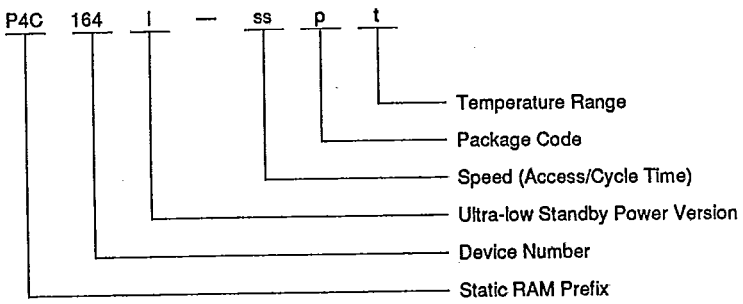
Figure 2. Thevenin Equivalent

* Including scope and test fixture.

Note:
Due to the ultra-high speed of the P4C164/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{cc} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{cc} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION

The following part numbering scheme is used for



l = Ultra-low standby power designator L, if needed.
ss = Speed (access/cycle time in ns), e.g., 25, 35
p = Package code, i.e., P, J, C, DW, L.
t = Temperature range, i.e., C, M, MB.

1519 09

PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide standard
DW	CERDIP, 600 mil wide
L	Leadless Chip Carrier (ceramic)

1519 Tbl 14

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C – +70°C.
M	Military Temperature Range, –55°C – +125°C.
MB	Mil. Temp. with MIL-STD-883C Class B compliance

1519 Tbl 15

SELECTION GUIDE

The P4C164 is available in the following temperature, speed and package options. The P4C164L is only available with access times of 20ns and slower for commercial temperatures, 25ns and slower for military temperatures.

Temp. Range	Package \ Speed	15	17	20	25	30	35	45
Com'l	Plastic DIP	-15PC	-17PC	-20PC	-25PC	-30PC	-35PC	N/A
	Plastic SOJ	-15JC	-17JC	-20JC	-25JC	-30JC	-35JC	N/A
	Sidebrazed DIP	-15CC	-17CC	-20CC	-25CC	-30CC	-35CC	N/A
	LCC	-15LC	-17LC	-20LC	-25LC	-30LC	-35LC	N/A
Mil. Temp.	Sidebrazed DIP	N/A	N/A	-20CM	-25CM	-30CM	-35CM	-45CM
	CERDIP (600 mil)	N/A	N/A	-20DWM	-25DWM	-30DWM	-35DWM	-45DWM
	LCC	N/A	N/A	-20LM	-25LM	-30LM	-35LM	-45LM
Military Proc'd*	Sidebrazed DIP	N/A	N/A	-20CMB	-25CMB	-30CMB	-35CMB	-45CMB
	CERDIP (600 mil)	N/A	N/A	-20DWMB	-25DWMB	-30DWMB	-35DWMB	-45DWMB
	LCC	N/A	N/A	-20LMB	-25LMB	-30LMB	-35LMB	-45LMB

1519 Tbl 16

* Military temperature range with MIL-STD-883 Revision C, Class B processing.
N/A = Not available

TECHDOC 1519