

DRAM MODULE

1, 2, 4 MEG x 32

4, 8, 16 MEGABYTE, 5V,
BURST EDO

FEATURES

- 72-pin, single-in-line memory module (SIMM)
- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- High-performance CMOS silicon-gate process
- Single +5V \pm 5% power supply
- All inputs and outputs are TTL-compatible
- Refresh modes: CAS-BEFORE-RAS (CBR) or RAS ONLY
- 1,024-cycle refresh (10 row-, 10 column-addresses) [MT2D(T)132 B]
- 2,048-cycle refresh (11 row-, 10 column-addresses) (MT4D232 B)
- 2,048-cycle refresh (11 row-, 11 column-addresses) (MT8D432 B)
- Four-cycle Extended Data-Out (EDO) burst accesses

OPTIONS

- Timing
52ns access; 15ns cycle -52
60ns access; 16.6ns cycle -60
- Components
SOJ D
TSOP (1 Meg x 32 only) DT
- Packages
72-pin SIMM M
72-pin SIMM (gold) G

MARKING

KEY TIMING PARAMETERS

SPEED	^t RAC	^t PC	^t CAC	^t COH	^t DS	^t DH
-52	52ns	15ns	10ns	3ns	0ns	5ns
-60	60ns	16.6ns	11ns	3ns	0ns	5ns

PART NUMBERS

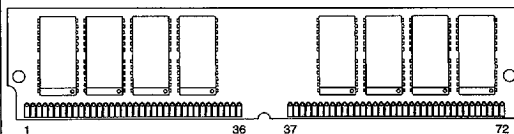
PART NUMBER	DESCRIPTION
MT2D132G-xx B	1 Meg x 32 Burst EDO, Gold, SOJ
MT2DT132G-xx B	1 Meg x 32 Burst EDO, Gold, TSOP
MT4D232G-xx B	2 Meg x 32 Burst EDO, Gold, SOJ
MT8D432G-xx B	4 Meg x 32 Burst EDO, Gold, SOJ
MT2D132M-xx B	1 Meg x 32 Burst EDO, Tin/Lead, SOJ
MT2DT132M-xx B	1 Meg x 32 Burst EDO, Tin/Lead, TSOP
MT4D232M-xx B	2 Meg x 32 Burst EDO, Tin/Lead, SOJ
MT8D432M-xx B	4 Meg x 32 Burst EDO, Tin/Lead, SOJ

xx = speed

PIN ASSIGNMENT (Front View)

72-Pin SIMM

- (DD-11) 1 Meg x 32 TSOP version
- (DD-9) 1 Meg x 32 SOJ version
- (DD-8) 2 Meg x 32
- (DD-3) 4 Meg x 32 (shown)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAST	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT2D(T)132 B, MT4D232 B and MT8D432 B are randomly accessed 4MB, 8MB and 16MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20/21/22 address bits, which are entered 10/11 bits (A0-A10) at RAS time and 10/11 bits (A0-A10) at CAS time.

These SIMMs are burst access DRAM modules in which all READ and WRITE cycles occur in bursts of four. The bursts wrap around on a 4-half-byte boundary. This means only the two least significant bits of the CAS address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with WE LOW), with address A0 set to either HIGH or LOW. A0 LOW will

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GENERAL DESCRIPTION (continued)

program the module to execute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information (0010 000x) where x=A0 is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a RAS-ONLY or CBR REFRESH cycle to exit this programming mode.

A READ or WRITE cycle is selected with the WE input during the first CAS LOW pulse of the burst. During the burst cycle the WE input must remain constant for the burst to continue. Transition of the WE input during a burst causes the burst to terminate and place the outputs in a High-Z state. After a terminated burst, the next falling edge of CAS will start a new burst access at the address present on the external address bus.

During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. WE must be LOW prior to CAS going LOW. This places the input/output pins in the High-Z state allowing the data-in (D) to be driven on the bus. WE must remain LOW during the burst operation for it to complete. WE going HIGH after WCH from CAS LOW and before WCS of the next CAS LOW terminates the burst operation and places the DQ pins in the High-Z state.

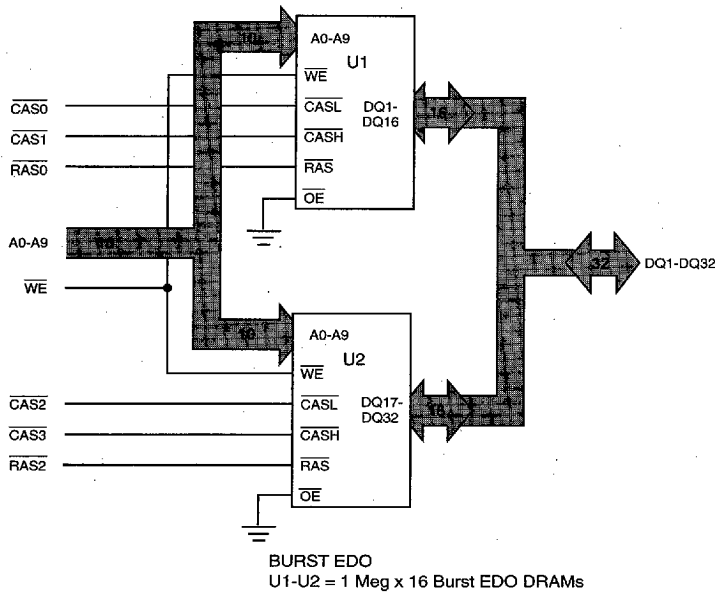
During a READ cycle WE must be HIGH prior to CAS going LOW. WE must remain HIGH during the burst operation for the burst to complete. WE going LOW after WCH from CAS LOW and before WCS of the next CAS LOW terminates the burst operation and places the DQ pins in the High-Z state.

Returning RAS and CAS HIGH terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next access during the RAS HIGH time.

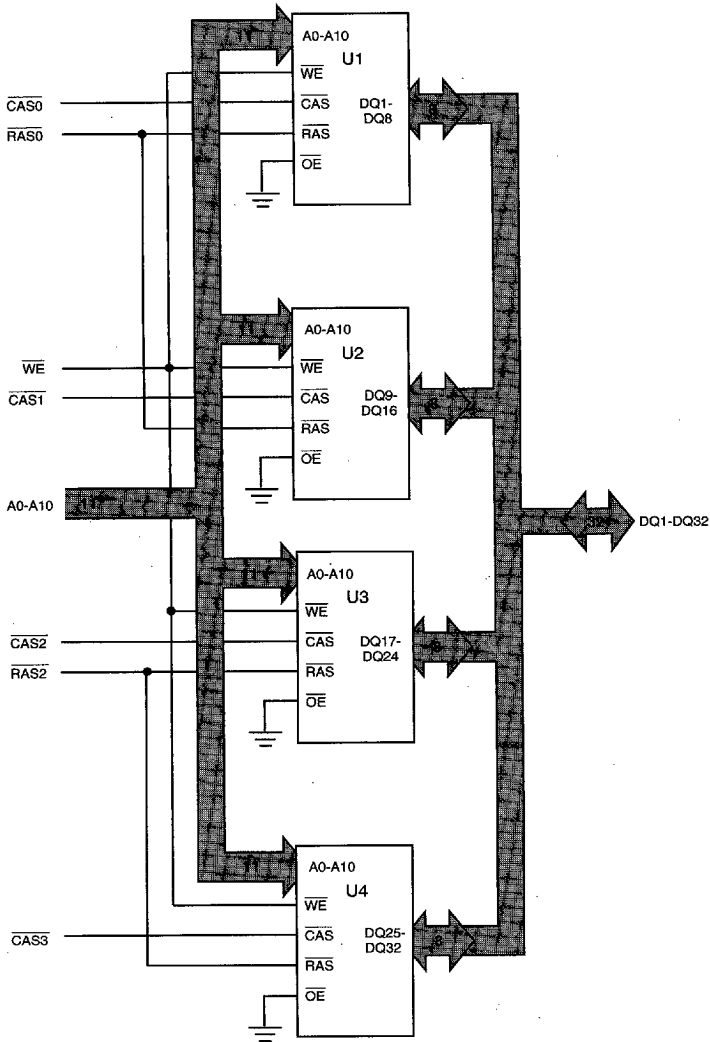
WORD AND BYTE WRITES

WORD WRITES on the x16 Burst EDO DRAM based module [MT2D(T)132] require CAS0 with CAS1 and CAS2 with CAS3 skew considerations that are not required on modules employing x4 and x8 Burst EDO DRAMs. BYTE WRITES on the x16 based MT2D(T)132 require special considerations when bursts are attempted. Refer to the MT4LC1M16H5 1 Meg x 16 Burst EDO DRAM data sheet for information on CAS to CAS skew requirements during WORD WRITE cycles and bursting BYTE WRITES.

**FUNCTIONAL BLOCK DIAGRAM
MT2(T)D132 B (4MB)**



**FUNCTIONAL BLOCK DIAGRAM
MT4D232 B (8MB)**

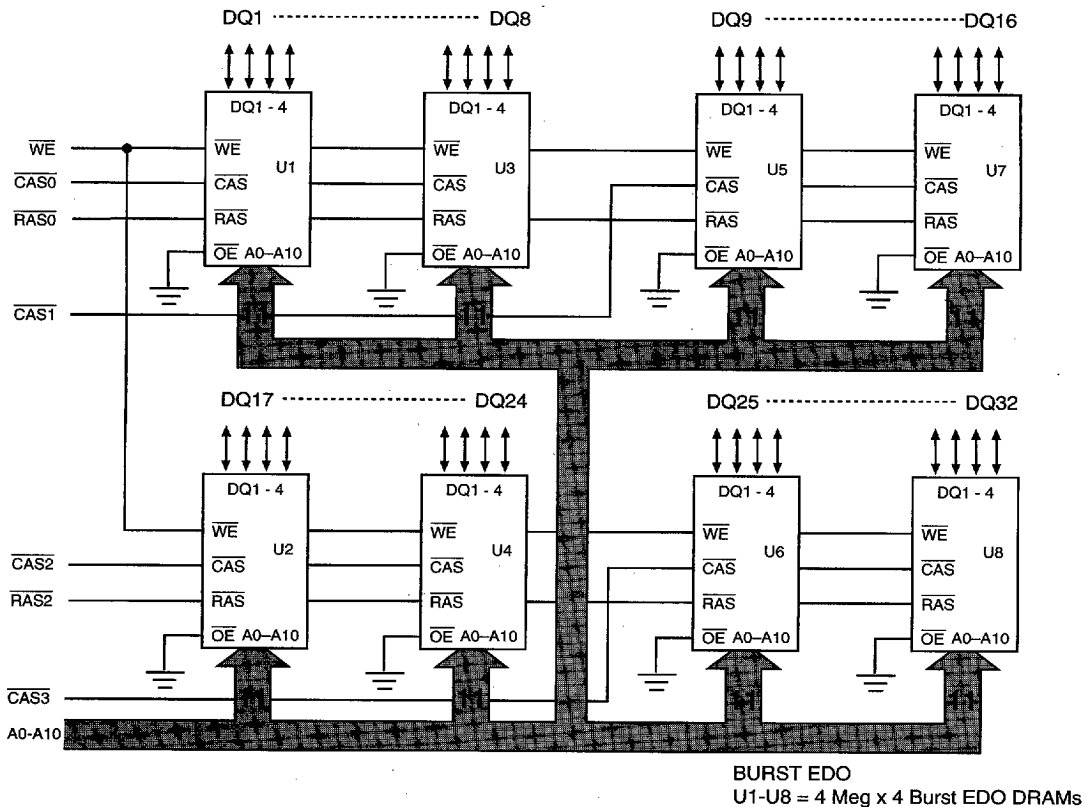


**BURST EDO
U1-U4 = 2 Meg x 8 Burst EDO DRAMs**

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**FUNCTIONAL BLOCK DIAGRAM
MT8D432 B (16MB)**

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EDO BURST MODE TRUTH TABLE

PRESENT STATE	RESULTING STATE	R \overline{AS}	C \overline{AS}	W \overline{E}	O \overline{E}	ADDRESSES		DATA
						Row	Column	DQ1-32
Any	Idle	L→H	H	X	X	X	X	High-Z
Idle	Row Open	H→L	H	X	X	ROW	X	High-Z
Idle	CBR REFRESH	H→L	L	H	X	X	X	High-Z
Row Open	R \overline{AS} -ONLY REFRESH	L	H	X	X	ROW	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	COL	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	COL	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H→L	L	L	X	A0 ¹	X	High-Z
PROGRAM	EXIT PROGRAM MODE using CBR REFRESH	H→L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE using R \overline{AS} -ONLY REFRESH	L	H	X	X	ROW	X	High-Z

NOTE: 1. A WCBR cycle determines the burst sequence. A0=LOW sets the burst sequence to linear, A0=HIGH set the burst sequence to interleave. A8 through A10 are "don't cares." A7-A0 should contain the sequence (0010 000x where x=A0) to ensure future compatability. A refresh cycle (R \overline{AS} ONLY or CBR) must follow the WCBR cycle to exit the programming mode.

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INTERLEAVE BURST SEQUENCE TABLE

OPERATION	ADDRESSES USED		
	A10 - A2	A1	A0
First access, register external CAS address	A10 - A2	A1	A0
Second access, (first burst address)	registered A10 - A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A10 - A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A10 - A2	registered $\overline{A1}$	registered $\overline{A0}$

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X00	X..X11	X..X10
X..X10	X..X11	X..X00	X..X01
X..X11	X..X10	X..X01	X..X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

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CAPACITANCE

PARAMETER	SYMBOL	MAX			UNITS	NOTES
		4MB	8MB	16MB		
Input Capacitance: A0-A10	Ci1	16	26	46	pF	3
Input Capacitance: WE	Ci2	16	26	46	pF	3
Input Capacitance: RAS0, RAS2	Ci3	10	16	28	pF	3
Input Capacitance: CAS0 - CAS3	Ci4	8	8	12	pF	3
Input/Output Capacitance: DQ1-DQ32	Cio	10	10	10	pF	3

PRESENCE-DETECT - MT2(T)D132 B (4MB)

SYMBOL	PIN #	-52	-60
PRD1	67	Vss	Vss
PRD2	68	Vss	Vss
PRD3	69	Vss	NC
PRD4	70	Vss	NC

PRESENCE-DETECT - MT4D232 B (8MB)

SYMBOL	PIN #	-52	-60
PRD1	67	NC	NC
PRD2	68	NC	NC
PRD3	69	Vss	NC
PRD4	70	Vss	NC

PRESENCE-DETECT - MT8D432 B (16MB)

SYMBOL	PIN #	-52	-60
PRD1	67	Vss	Vss
PRD2	68	NC	NC
PRD3	69	Vss	NC
PRD4	70	Vss	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss -1V to +7V
 Voltage on Inputs, NC or I/O pins
 Relative to Vss -1V to +5.5V
 Operating Temperature, T_A (ambient) 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 4.8W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (Vcc = +5V ±5%)

PARAMETER/CONDITION	SYM	SIZE	MIN	MAX	UNITS	NOTES	
Supply Voltage	Vcc	ALL	4.75	5.25	V		
Input High (Logic 1) Voltage, all inputs	V _{IH}	ALL	2.4	5.25	V	2	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	ALL	-1.0	0.8	V	2	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V (All other pins not under test = 0V)	CAS0-CAS3	I _{I1}	4MB	-2	2	μA	
		8MB	-2	2	μA		
		16MB	-4	4	μA		
	A0-A10, \overline{WE} , $\overline{RAS0}$, $\overline{RAS2}$	I _{I2}	4MB	-4	4	μA	18
8MB		-8	8	μA			
		16MB	-16	16	μA		
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	DQ1-DQ32	I _{OZ}	ALL	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA) Output Low Voltage (I _{OUT} = 4.2mA)		V _{OH}	ALL	2.4		V	
		V _{OL}	ALL		0.4	V	

PARAMETER/CONDITION	SYM	SIZE	MAX		UNITS	NOTES
			-52	-60		
STANDBY CURRENT: (TTL) (RAS = CAS = V _{IH})	I _{CC1}	4MB 8MB 16MB	14 18 26	14 18 26	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc - 0.2V)	I _{CC2}	4MB 8MB 16MB	11 12 14	11 12 14	mA	
OPERATING CURRENT: Closed Row Burst READ/WRITE Average power supply current; (PC = t _{PC} [MIN]; 50% duty cycle on RAS; open row, four-cycle burst, close row)	I _{CC3}	4MB 8MB 16MB	320 440 880	300 400 800	mA	4, 5
OPERATING CURRENT: Open Row Burst READ/WRITE Average power supply current (alternating four-cycle burst followed by four cycles of inactivity; PC = t _{PC} [MIN])	I _{CC4}	4MB 8MB 16MB	180 280 520	170 260 480	mA	4, 5
REFRESH CURRENT: RAS ONLY Average power supply current (address cycling; RAS cycling CAS = V _{IH} ; RAS = t _{RAS} [MIN]; RP = t _{RP} [MIN])	I _{CC5}	4MB 8MB 16MB	380 560 1,040	320 520 960	mA	4, 5
REFRESH CURRENT: CBR Average power supply current (RAS, CAS cycling; RAS = t _{RAS} [MIN]; RP = t _{RP} [MIN])	I _{CC6}	4MB 8MB 16MB	340 560 1,040	300 520 960	mA	5, 6

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

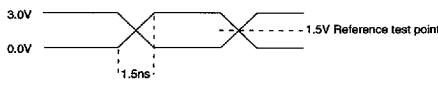
(Notes: 7, 8, 9, 10, 13) (Vcc = +5V ±5%)

AC CHARACTERISTICS PARAMETER	SYM	-52		-60		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Access time from CAS	tAA		25		28.2	ns	11
Column-address setup time	tASC	1.5		1.5		ns	
Row-address setup time	tASR	1.5		1.5		ns	
Burst terminate hold time	tBTH	3		3		ns	
Output disable from burst terminate	tBTHZ	7	13	7	13	ns	14
Access time from CAS	tCAC		10		11	ns	
Column-address hold time	tCAH	8.5		8.5		ns	
CAS pulse width	tCAS	5	10,000	5	10,000	ns	
CAS0 and CAS1 or CAS2 and CAS3 Coincident HIGH time	tCCH	5		5		ns	15
CAS hold time (CBR or WCBR)	tCHR	15		15		ns	6
CAS to output in Low-Z	tCLZ	3		3		ns	
Data Hold time from CAS LOW	tCOH	3		3		ns	
CAS precharge time	tCP	5		5		ns	
CAS precharge time (CBR or WCBR)	tCPN	10		10		ns	
CAS to RAS precharge time	tCRP	10		10		ns	
CAS LOW to RAS HIGH (WRITE only)	tCRW	15		16.6		ns	
Skew between CAS0 and CAS1 or CAS2 and CAS3 (WRITE only)	tCSK		2		2	ns	16
CAS setup time (CBR or WCBR)	tCSR	10		10		ns	6
Data-in hold time	tDH	5		5		ns	
Data-in setup time	tDS	0		0		ns	17
Output buffer turn-off delay	tOFF	4	13	4	13	ns	
Burst EDO cycle time	tPC	15		16.6		ns	
Access time from RAS	tRAC		52		60	ns	
Row-address hold time	tRAH	8.5		8.5		ns	
RAS pulse width	tRAS	52	125,000	60	125,000	ns	
Random Read or Write cycle time	tRC	90				ns	
RAS to CAS delay time	tRCD1	20		20		ns	
RAS to CAS delay time	tRCD2	40		45		ns	
Read command hold time	tRCH	5		5		ns	
Read command setup time	tRCS	3		4		ns	
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (2,048 cycles)	tREF		32		32	ms	
RAS precharge time	tRP	30		40		ns	
RAS to CAS precharge time	tRPC	5		5		ns	
RAS hold time	tRSH	0		0		ns	
Transition time (rise or fall)	tT	1.5	50	1.5	50	ns	
Burst Terminate pulse width	tTP	6		6		ns	12
Write command hold time	tWCH	5		5		ns	
WE command setup time	tWCS	3		4		ns	
Output Disable from WE LOW	tWHZ	4	10	4	10	ns	14
WE hold time (CBR or WCBR)	tWRH	10		10		ns	
WE setup time (CBR or WCBR)	tWRP	10		10		ns	

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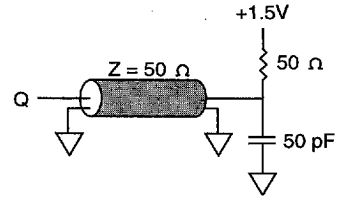
Input timing waveform:



Output timing waveform:



**Figure 1
TIMING SPECIFICATIONS**



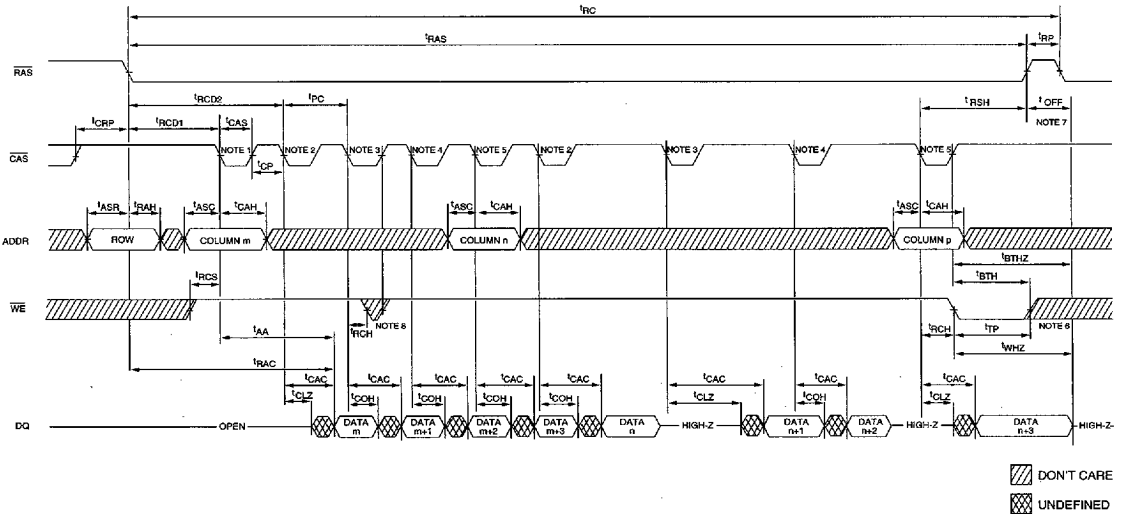
**Figure 2
AC TIMING OUTPUT LOAD EQUIVALENT**

NOTES

1. All voltages referenced to V_{ss}.
2. Input Power-up: V_{IH} ≤ +5.5V and V_{CC} ≤ +5.5V for t ≤ 200ms
3. This parameter is sampled. V_{CC} = 5V ±5%; f = 1 MHz.
4. Address transitions once per burst access.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum t_{PC} and 50 percent duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100μs after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with WE HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded. A WCBR cycle must be executed to initialize the burst type, interleave or linear followed by a $\overline{\text{RAS}}$ ONLY or CBR REFRESH cycle.
8. AC characteristics assume t_T = 1.5ns.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when AC specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. t_{AA} is a calculated specification which is the sum of t_{PC} and t_{CAC}.
12. Applies only during burst termination operation.
13. AC output loading is specified with C_L = 50pF as in Figure 2. Transition is measured at the 1.5V reference level.
14. The DQs will continue to drive data out until both t_{BTHZ} (MIN) and t_{WHZ} (MIN) have been satisfied and will reach the High-Z state once t_{BTHZ} (MAX) and t_{WHZ} (MAX) have both been satisfied.
15. $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$, etc. HIGH pulse widths must be concurrently HIGH for at least this limit [MT2D(T)132 B version only].
16. The skew between $\overline{\text{CAS0}}$ and $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ and $\overline{\text{CAS3}}$ is required for WRITE cycles and is required only on the MT2D(T)132 B SIMM since it utilizes 1 Meg x 16 Burst EDO DRAMs.
17. Valid data-in is referenced from when a valid logic level (V_{IH}, V_{IL}) is achieved.
18. $\overline{\text{RAS0}}$ and $\overline{\text{RAS2}}$ will be half of the values shown.

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BURST EDO READ CYCLE



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- NOTE:**
1. Latch column address; start READ cycle.
 2. Output data 1; increment burst counter.
 3. Output data 2; increment burst counter.
 4. Output data 3; increment burst counter.
 5. Output data 4; latch column address; start READ cycle.
 6. WE transitioning LOW will terminate the burst and reset the burst counter provided tTP and tBTH are satisfied. The DQs will continue to drive data out until tBTHZ (MIN) and tWHZ (MIN) have both been

- satisfied and will reach the High-Z state once tBTHZ (MAX) and tWHZ (MAX) have both been satisfied.
7. The combination of RAS and CAS HIGH close the row and place the DQs in the High-Z state. tOFF is measured from the last signal (RAS or CAS) that transitions HIGH.
8. WE transitioning LOW and returning HIGH prior to CAS going HIGH will not terminate the burst.

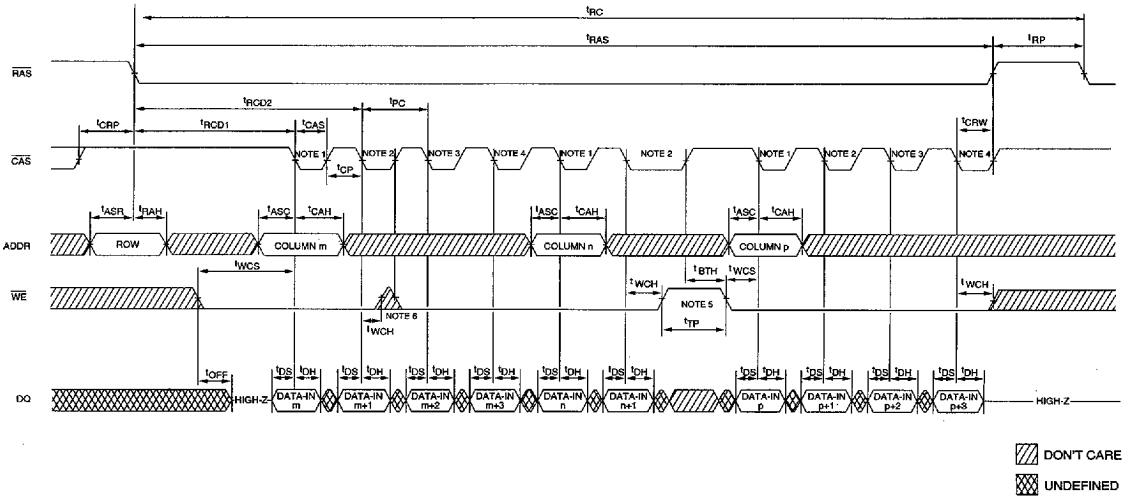
TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		28.2	ns
tASC	1.5		1.5		ns
tASR	1.5		1.5		ns
tBTH	3		3		ns
tBTHZ	7	13	7	13	ns
tCAC		10		11	ns
tCAH	8.5		8.5		ns
tCAS	5	10,000	5	10,000	ns
tCLZ	3		3		ns
tCOH	3		3		ns
tCP	5		5		ns
tCRP	10		10		ns
tOFF	4	10	4	10	ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
tPC	15		16.6		ns
tRAC		52		60	ns
tRAH	8.5		8.5		ns
tRAS	52	125,000	60	125,000	ns
tRC	90		110		ns
tRCD1	20		20		ns
tRCD2	40		45		ns
tRCH	5		5		ns
tRCS	3		4		ns
tRP	30		40		ns
tRSH	0		0		ns
tTP	6		6		ns
tWHZ	4	10	4	10	ns

BURST EDO WRITE CYCLE

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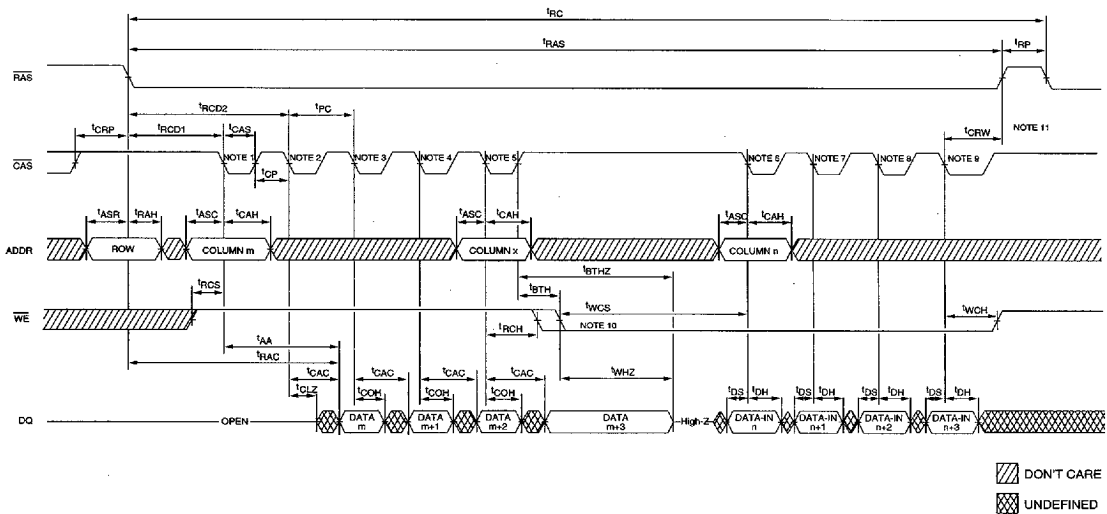
- NOTE:**
1. Latch column address; start burst WRITE cycle; write data 1.
 2. Increment burst counter; write data 2.
 3. Increment burst counter; write data 3.
 4. Increment burst counter; write data 4.
 5. WE transitioning HIGH will terminate the burst and reset the burst counter provided t_{TP} and t_{BTH} are satisfied.
 6. WE transitioning HIGH and returning LOW prior to \overline{CAS} going HIGH will not terminate the burst.

TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t_{ASC}	1.5		1.5		ns
t_{ASR}	1.5		1.5		ns
t_{BTH}	3		3		ns
t_{CAH}	8.5		8.5		ns
t_{CAS}	5	10,000	5	10,000	ns
t_{CP}	5		5		ns
t_{CRP}	10		10		ns
t_{CRW}	15		16.6		ns
t_{DH}	5		5		ns
t_{DS}	0		0		ns
t_{OFF}	4	13	4	13	ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t_{PC}	15		16.6		ns
t_{RAH}	8.5		8.5		ns
t_{RAS}	52	125,000	60	125,000	ns
t_{RC}	90		110		ns
t_{RCD1}	20		20		ns
t_{RCD2}	40		45		ns
t_{RP}	30		40		ns
t_{TP}	6		6		ns
t_{WCH}	5		5		ns
t_{WCS}	3		4		ns

BURST EDO READ/WRITE CYCLE



▨ DON'T CARE
▩ UNDEFINED

NOTE:

1. Latch column address; start burst READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start burst READ cycle.
6. Latch column address; start burst WRITE cycle; write data 1.
7. Increment burst counter; write data 2.
8. Increment burst counter; write data 3.
9. Increment burst counter; write data 4.
10. \overline{WE} transitioning LOW will terminate the burst and reset the burst counter provided t_{TP} and t_{BTH} are satisfied. t_{TP} is met by the READ burst being terminated by a WRITE burst. The DQs will continue to drive data out until t_{BTHZ} (MIN) and t_{WHZ} (MIN) have both been satisfied and will reach the High-Z state once t_{BTHZ} (MAX) and t_{WHZ} (MAX) have both been satisfied.
11. The combination of \overline{RAS} and \overline{CAS} HIGH close the row and place the DQ pins in the High-Z state.

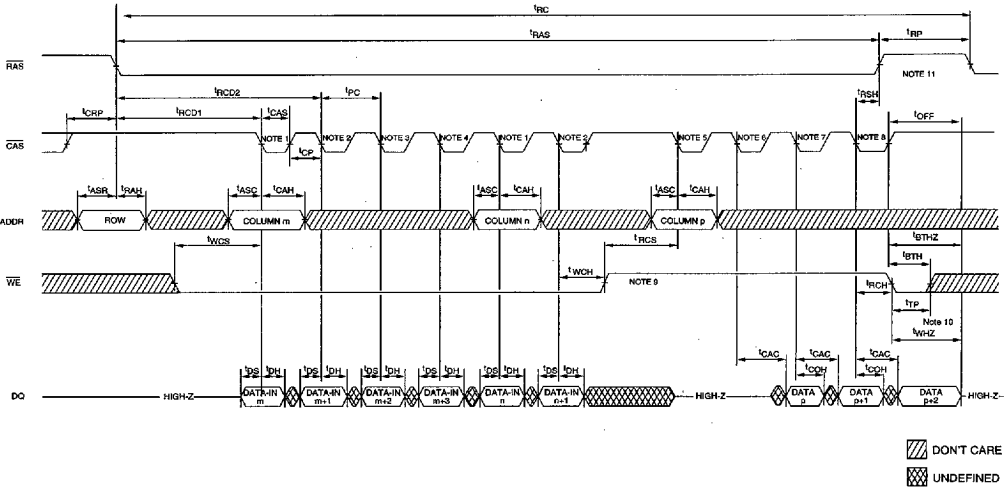
TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		28.2	ns
t_{ASC}	1.5		1.5		ns
t_{ASR}	1.5		1.5		ns
t_{BTH}	3		3		ns
t_{BTHZ}	7	13	7	13	ns
t_{CAC}		10		11	ns
t_{CAH}	8.5		8.5		ns
t_{CAS}	5	10,000	5	10,000	ns
t_{CLZ}	3		3		ns
t_{COH}	3		3		ns
t_{CP}	5		5		ns
t_{CRP}	10		10		ns
t_{CRW}	15		16.6		ns
t_{DH}	5		5		ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t_{DS}	0		0		ns
t_{PC}	15		16.6		ns
t_{RAC}		52		60	ns
t_{RAH}	8.5		8.5		ns
t_{RAS}	52	125,000	60	125,000	ns
t_{RC}	90		110		ns
t_{RCD1}	20		20		ns
t_{RCD2}	40		45		ns
t_{RCH}	5		5		ns
t_{RCS}	3		4		ns
t_{RP}	30		40		ns
t_{WCH}	5		5		ns
t_{WCS}	3		4		ns
t_{WHZ}	4	10	4	10	ns

BURST EDO WRITE/READ CYCLE

**NEW
DRAM SIMM**



▨ DONT CARE
▩ UNDEFINED

NOTE:

1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. Latch column address; start burst READ cycle.
6. Output data 1; increment column address.
7. Output data 2; increment column address.
8. Output data 3; increment column address.
9. WE transitioning HIGH will terminate the burst and reset the burst counter. The tBTH time is not required as it is satisfied by tRCS; tTP is met by the WRITE burst being terminated by a READ burst.

10. WE transitioning LOW will terminate the burst and reset the burst counter provided tTP and tBTH are satisfied. The DQs will continue to drive data out until tBTHZ (MIN) and WHZ (MIN) have both been satisfied and will reach the High-Z state once tBTHZ (MAX) and tWHZ (MAX) have both been satisfied.
11. The combination of RAS and CAS HIGH close the row and place the DQ pins in the High-Z state. tOFF is measured from the last signal (RAS or CAS) that transitions HIGH.

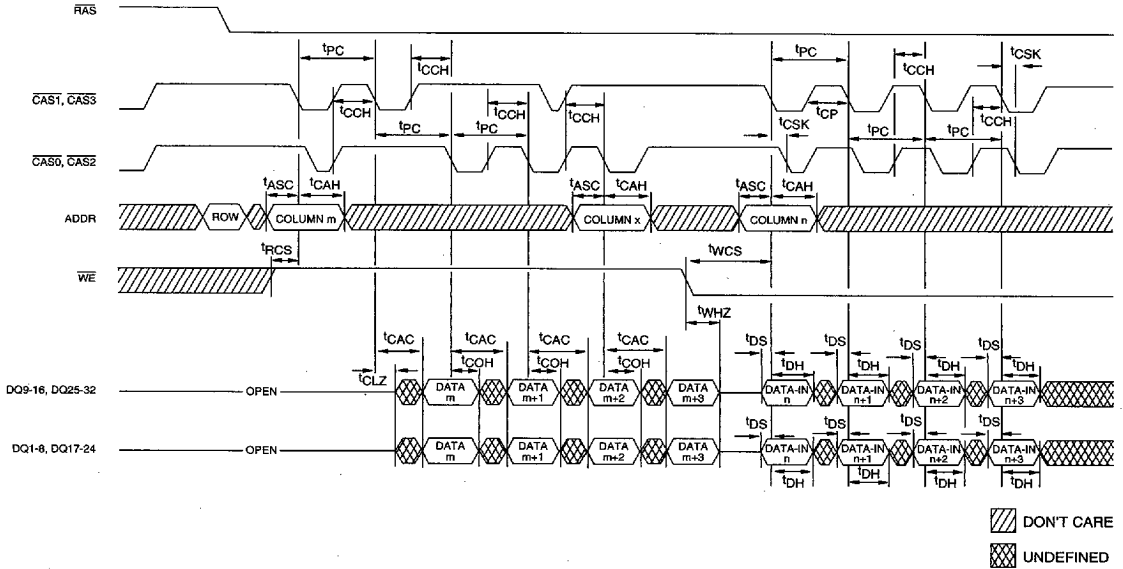
TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
tASC	1.5		1.5		ns
tASR	1.5		1.5		ns
tBTH	3		3		ns
tBTHZ	7	13	7	13	ns
tCAC		10		11	ns
tCAH	8.5		8.5		ns
tCAS	5	10,000	5	10,000	ns
tCOH	3		3		ns
tCP	5		5		ns
tCRP	10		10		ns
tDH	5		5		ns
tDS	0		0		ns
tOFF	4	10	4	10	ns
tPC	15		16.6		ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
tRAH	8.5		8.5		ns
tRAS	52	125,000	60	125,000	ns
tRC	90		110		ns
tRCD1	20		20		ns
tRCD2	40		45		ns
tRCH	5		5		ns
tRCS	3		4		ns
tRP	30		40		ns
tRSH	0		0		ns
tTP	6		6		ns
tWCH	5		5		ns
tWCS	3		4		ns
tWHZ	4	10	4	10	ns

■ 6111549 0013617 T2T ■

**BURST EDO
READ/WORD-WRITE CYCLE**



**NEW
DRAM SIMM**

NOTE: 1. The CAS to CAS skew requirements apply to CAS0 with CAS1 and CAS2 with CAS3 on the MT2D(T)132 B only.

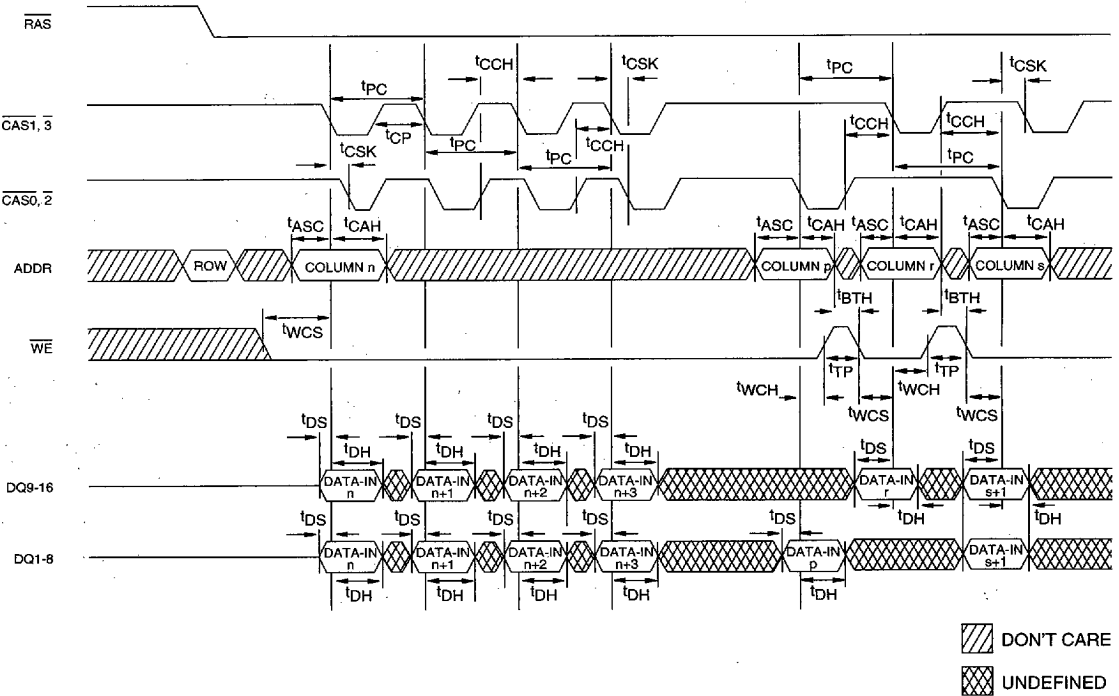
TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t _{ASC}	1.5		1.5		ns
t _{CAC}		10		11	ns
t _{CAH}	8.5		8.5		ns
t _{CCH}	5		5		ns
t _{CLZ}	3		3		ns
t _{COH}	3		3		ns
t _{CP}	5		5		ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t _{CSK}		2		2	ns
t _{DH}	5		5		ns
t _{DS}	0		0		ns
t _{PC}	15		16.6		ns
t _{RCS}	3		4		ns
t _{WCS}	3		4		ns
t _{WHZ}	4	10	4	10	ns

BURST EDO
WORD-WRITE/BYTE-WRITE CYCLE

NEW DRAM SIMM



▨ DON'T CARE
▩ UNDEFINED

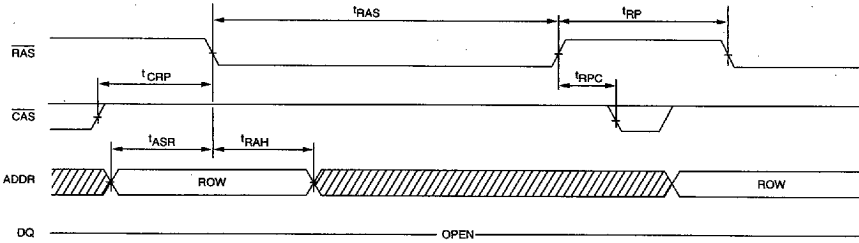
NOTE: 1. Applies to MT2D(T)132 B module only.

TIMING PARAMETERS

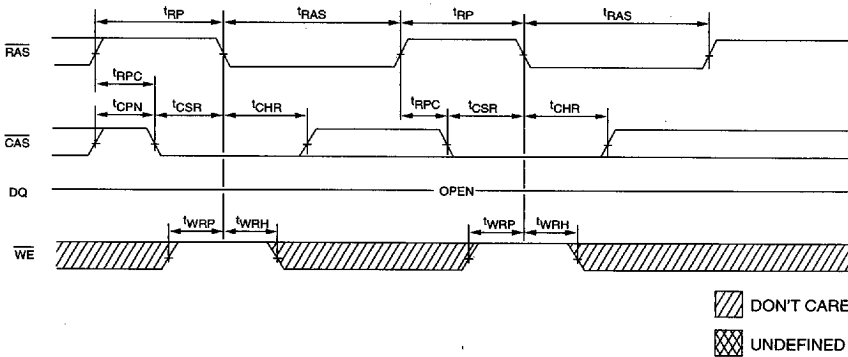
SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
^t ASC	1.5		1.5		ns
^t BTH	3		3		ns
^t CAH	8.5		8.5		ns
^t CCH	5		5		ns
^t CP	5		5		ns
^t CSK		2		2	ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
^t DH	5		5		ns
^t DS	0		0		ns
^t PC	15		16.6		ns
^t TP	6		6		ns
^t WCH	5		5		ns
^t WCS	3		4		ns

RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE



NOTE: 1. CBR REFRESH is recommended for all new designs to ensure compatibility with future generation DRAMs. Micron and JEDEC recommend CBR REFRESH as the preferred method of refresh for the 64 Meg DRAM generation and beyond.

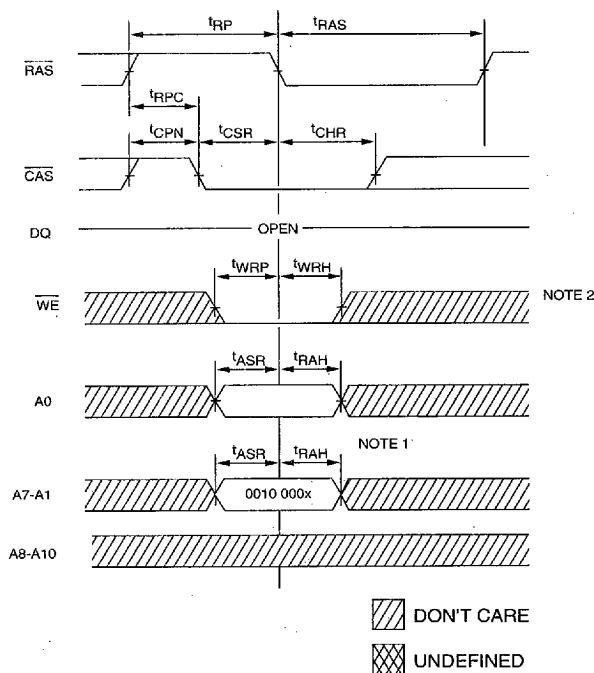
TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	1.5		1.5		ns
t _{CHR}	15		15		ns
t _{CPN}	10		10		ns
t _{CRP}	10		10		ns
t _{CSR}	10		10		ns
t _{RAH}	8.5		8.5		ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t _{RAS}	52	125,000	60	125,000	ns
t _{RP}	30		40		ns
t _{RPC}	5		5		ns
t _{WRH}	10		10		ns
t _{WRP}	10		10		ns

NEW DRAM SIMM

WCBR PROGRAM CYCLE



- NOTE:**
1. A0 LOW sets the burst sequence to linear bursts. A0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are "don't cares." Addresses A7-A0 should contain the state of (0010 000x where x=A0) to ensure future compatibility. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
 2. A RAS-ONLY or CBR REFRESH cycle must be executed after the WCBR cycle to exit the programming mode.

TIMING PARAMETERS

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t_{ASR}	1.5		1.5		ns
t_{CHR}	15		15		ns
t_{CPN}	10		10		ns
t_{CSR}	10		10		ns
t_{RAH}	8.5		8.5		ns

SYM	-52		-60		UNITS
	MIN	MAX	MIN	MAX	
t_{RAS}	52	125,000	60	125,000	ns
t_{RP}	30		40		ns
t_{RPC}	5		5		ns
t_{WRH}	10		10		ns
t_{WRP}	10		10		ns