FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10142-4E

MEMORY

CMOS 4 M × 1 BIT FAST PAGE MODE DRAM

MB814100A-60/-70/-80

CMOS 4,194,304 × 1 bit Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB814100A is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a ×1 configuration. The MB814100A features a ”fast page” mode of operation whereby high-speed random access of up to 2,048-bits of data within the same row can be selected. The MB814100A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814100A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814100A is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100A are not critical and all inputs are TTL compatible.

■ PRODUCT LINE & FEATURES

Parameter		MB814100A-60	MB814100A-70	MB814100A-80
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.	80 ns max.
$\overline{CAS}$ Access Time		15 ns max.	20 ns max.	20 ns max.
Address Access Time		30 ns max.	35 ns max.	40 ns max.
Randam Cycle Time		110 ns min.	125 ns min.	140 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.	45 ns min.
Low Power Dissipation	Operating current	605 mW max.	550 mW max.	495 mW max.
	Standby current	11 mW max. (TTL level) / 5.5 mW max. (CMOS level)		

- 4,194,304 words ×1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output areTTL compatible
- 1024 refresh cycles every16.4 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

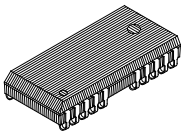
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

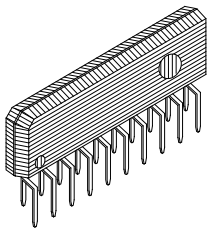
Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	–1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	–1 to +7	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

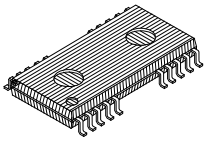
■ PACKAGE



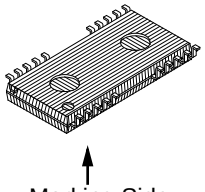
LCC-26P-M04



ZIP-20P-M02



(Normal Bend)
FPT-26P-M01

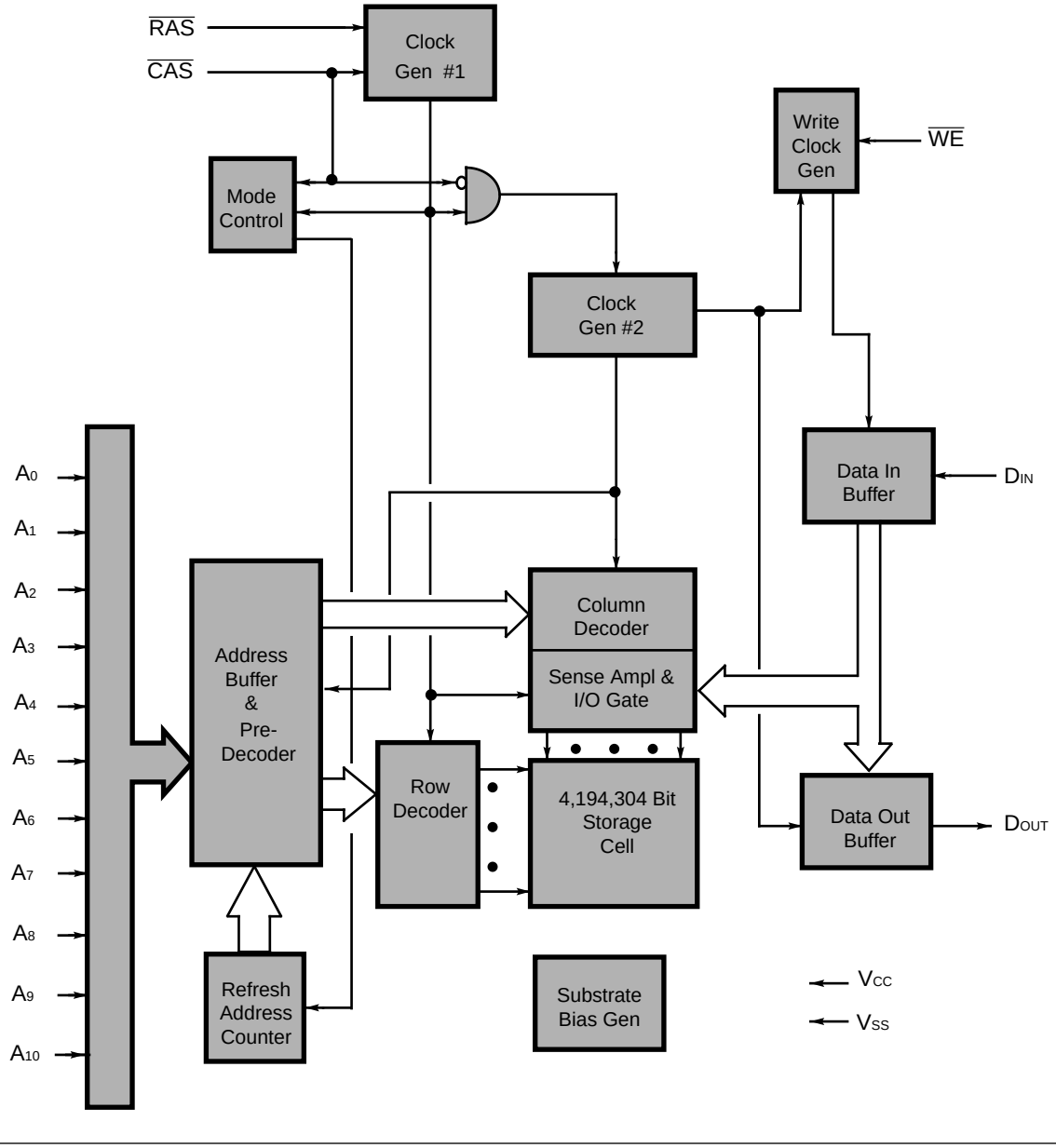


(Reverse Bend)
FPT-26P-M02

Package and Ordering Information

– 26-pin plastic (300 mil) SOJ, order as MB814100A-xxPJN
– 20-pin plastic ZIP, order as MB814100A-xxPZ
– 26-pin plastic (300 mil) TSOP, with normal bend leads, order as MB814100A-xxPFTN
– 26-pin plastic (300 mil) TSOP, with reverse bend leads, order as MB814100A-xxPFTN

Fig. 1 - MB814100A DYNAMIC RAM - BLOCK DIAGRAM



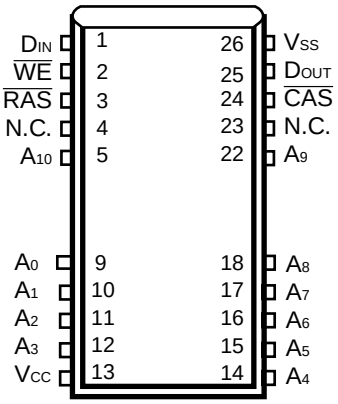
■ CAPACITANCE

(TA=25°C, F=1 MHZ)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_{10}, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	7	pF
Input Capacitance, D_{OUT}	C_{OUT}	—	7	pF

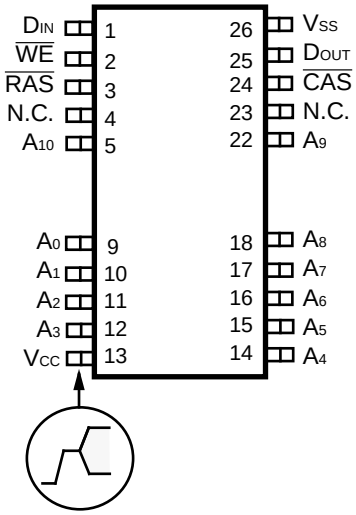
■ PIN ASSIGNMENT AND DESCRIPTION

26-Pin SOJ:
(Top View)

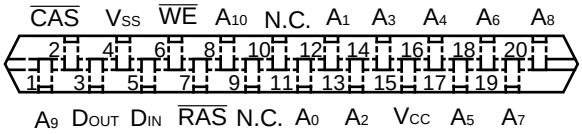


26-Pin FPT:
(Top View)

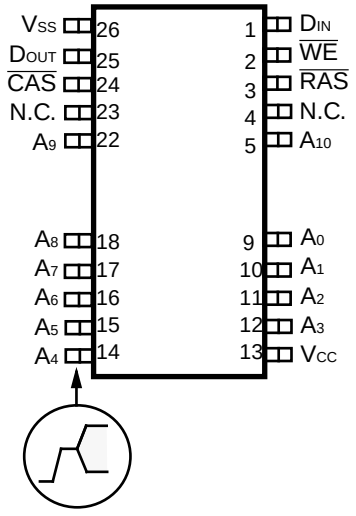
<Normal Bend : FPT-26P-M01>



20-Pin ZIP:
(Top View)



<Reverse Bend : FPT-26P-M02>



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row Address Strobe.
N.C.	No Connection.
A_0 to A_{10}	Address Inputs.
V_{CC}	+5 volt Power Supply.
$\overline{CAS}$	Column Address Strobe.
V_{SS}	Circuit Ground.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V_{IL}	–2.0	—	0.8	V	

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty-two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A_0-A_{10}) are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 5. First, eleven row address bits are applied on pins A_0-through-A_{10} and latched with the row address strobe ($\overline{RAS}$) then, eleven column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min.)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways--an early write cycle and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- **t_{RAC} :** from the falling edge of $\overline{RAS}$ when t_{RCD} (max.) is satisfied.
- **t_{CAC} :** from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max.).
- **t_{AA} :** from column address input when t_{RAD} is greater than t_{RAD} (max.).

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 2,048-bits can be accessed and, when multiple MB 814100s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready-modify-write cycles are permitted.

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) **Note 3**

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Output High Voltage	1	V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output Low Voltage	1	V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	
Input Leakage Current (Any input)		$I_{I(L)}$	0 V≤V_{IN}≤5.5 V; 4.5 V≤V_{CC}≤5.5 V; V_{SS} =0 V; All other pins not under test = 0 V	–10	—	10	µA
Output Leakage Current		$I_{O(L)}$	0 V≤V_{OUT}≤5.5 V; Data out disabled	–10	—	10	
Operating current (Average Power Supply Current) 2	MB814100A-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min.	—	—	110	mA
	MB814100A-70					100	
	MB814100A-80					90	
Standby Current (Power Supply Current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} -0.2 V			1.0	
Refresh Current #1 (Average Power Supply Current) 2	MB814100A-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min.	—	—	110	mA
	MB814100A-70					100	
	MB814100A-80					90	
Fast Page Mode Current 2	MB814100A-60	I_{CC4}	$\overline{RAS}$ =V_{IL}, $\overline{CAS}$ cycling; t_{RC} = min.	—	—	55	mA
	MB814100A-70					50	
	MB814100A-80					45	
Refresh Current #2 (Average Power Supply Current) 2	MB814100A-60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min.	—	—	90	mA
	MB814100A-70					80	
	MB814100A-80					70	

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100A-60		MB814100A-70		MB814100A-80		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	140	—	ns
3	Read-Modify-WriteCycle Time		t_{RWC}	130	—	150	—	165	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	—	80	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	20	—	20	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	ns
10	Transition Time		t_T	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	50	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	20	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	5	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	20	50	20	60	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	20	—	20	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	80	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	10	—	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	15	40	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	40	—	ns
25	Column Address to $\overline{CAS}$ Lead time		t_{CAL}	30	—	35	—	40	—	ns
26	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns

■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100A-60		MB814100A-70		MB814100A-80		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
28	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
29	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	ns
31	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	12	—	ns
32	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	20	—	ns
33	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	18	—	20	—	ns
34	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
35	DIN Hold Time		t_{DH}	10	—	10	—	12	—	ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	60	—	70	—	80	—	ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	15	—	20	—	20	—	ns
38	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	30	—	35	—	40	—	ns
39	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	12	—	ns
42	$\overline{WE}$ Set Up Time from $\overline{RAS}$	18	t_{WSR}	0	—	0	—	0	—	ns
43	$\overline{WE}$ Hold Time from $\overline{RAS}$	18	t_{WHR}	10	—	10	—	10	—	ns
51	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	45	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	60	—	68	—	70	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	35	—	40	—	40	ns
54	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns
55	Fast Page Mode $\overline{RAS}$ Pulse width		t_{RASP}	—	200000	—	200000	—	200000	ns
56	Fast Page Mode $\overline{RAS}$ Hold Time from CAS Precharge		t_{RHCP}	35	—	40	—	40	—	ns
57	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	35	—	40	—	40	—	ns

Notes:
1. Referenced to V_{SS}
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during one Page Cycle.
3. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min.) and V_{IL} (max.).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$(max.), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max.) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min.) = t_{RAH} (min.)+ $2t_T$ + t_{ASC} (min.).
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD} , t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.), $t_{RWD} \geq t_{RWD}$ (min.), and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read modify-write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin , and write operation can be exected by satisfying t_{RWL} , t_{CWL}, t_{CAL} and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max.).
17. Assumes that $\overline{CAS}$-before- $\overline{RAS}$ refresh.
18. Assumes that Test mode function.

Fig. 2 - t_{RAC} vs. t_{RCD}

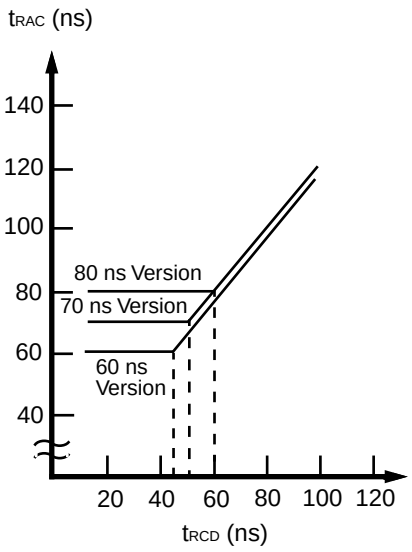


Fig. 3 - t_{RAC} vs. t_{RAD}

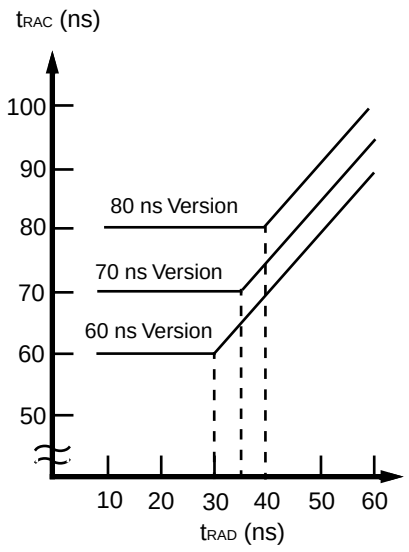
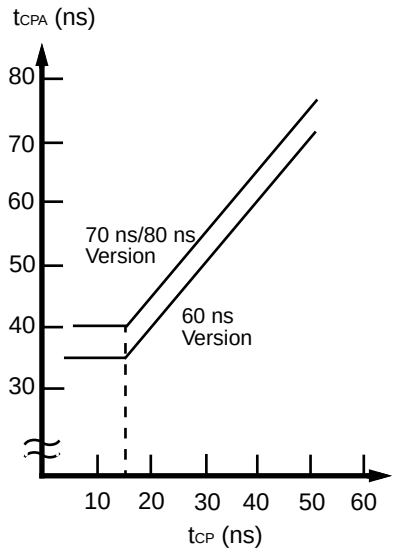


Fig. 4 - t_{CPA} vs. t_{CP}



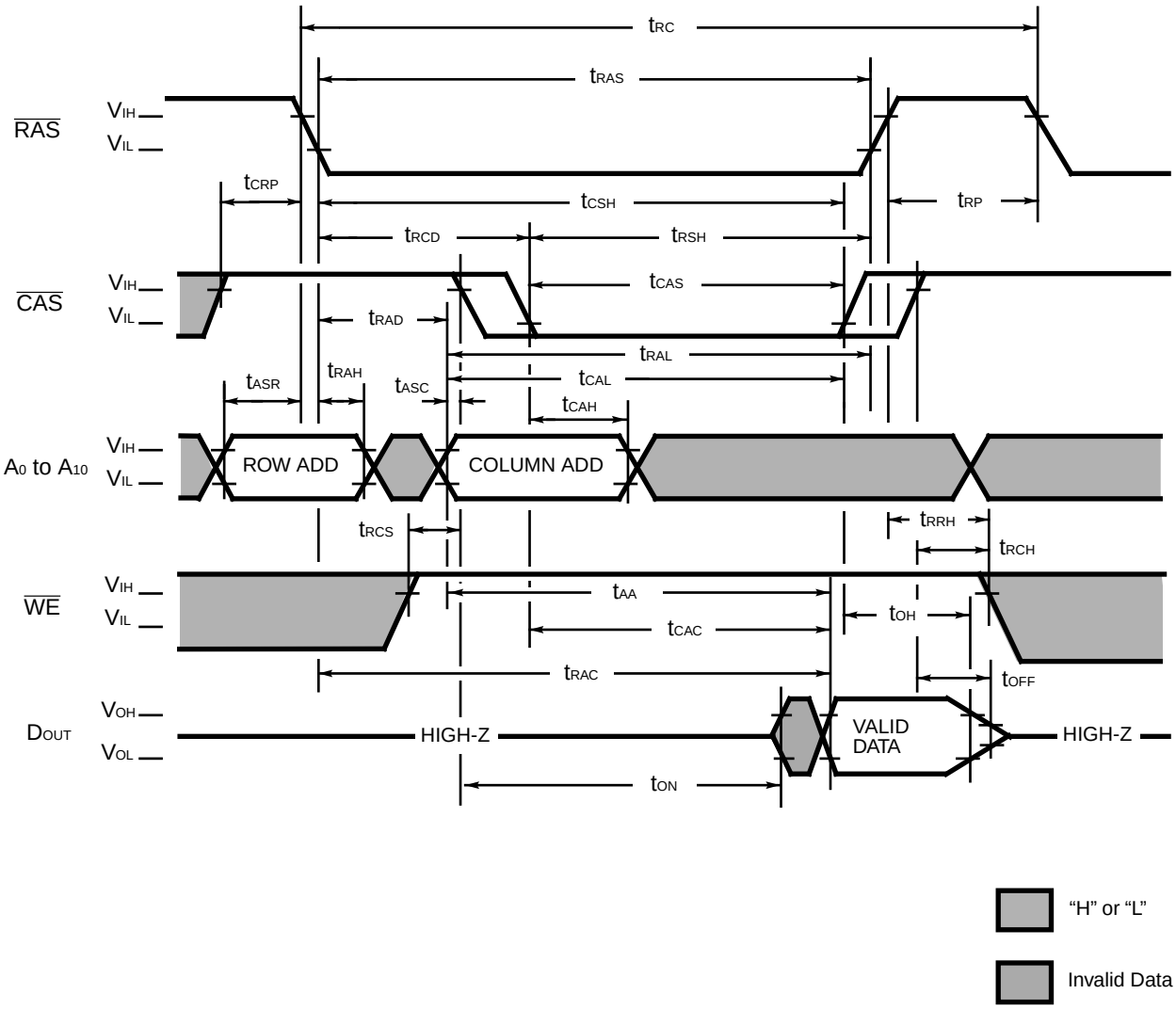
■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}$ (min.)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}$ (min.)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}$ (min.)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.)
Hidden Refresh Cycle	H→L	L	H	—	—	—	Valid	Yes	Previous data is kept
Test mode set cycle (CBR)	L	L	L	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.) $t_{WSR} \geq t_{WSR}$ (min.)
Test mode set cycle (Hidden)	H→L	L	L	—	—	—	Valid	Yes	$_{CSR} \geq t_{CSR}$ (min.) $t_{WSR} \geq t_{WSR}$ (min.)

Note : X : “H” or “L”

*1: It is impossible in Fast Page Mode.

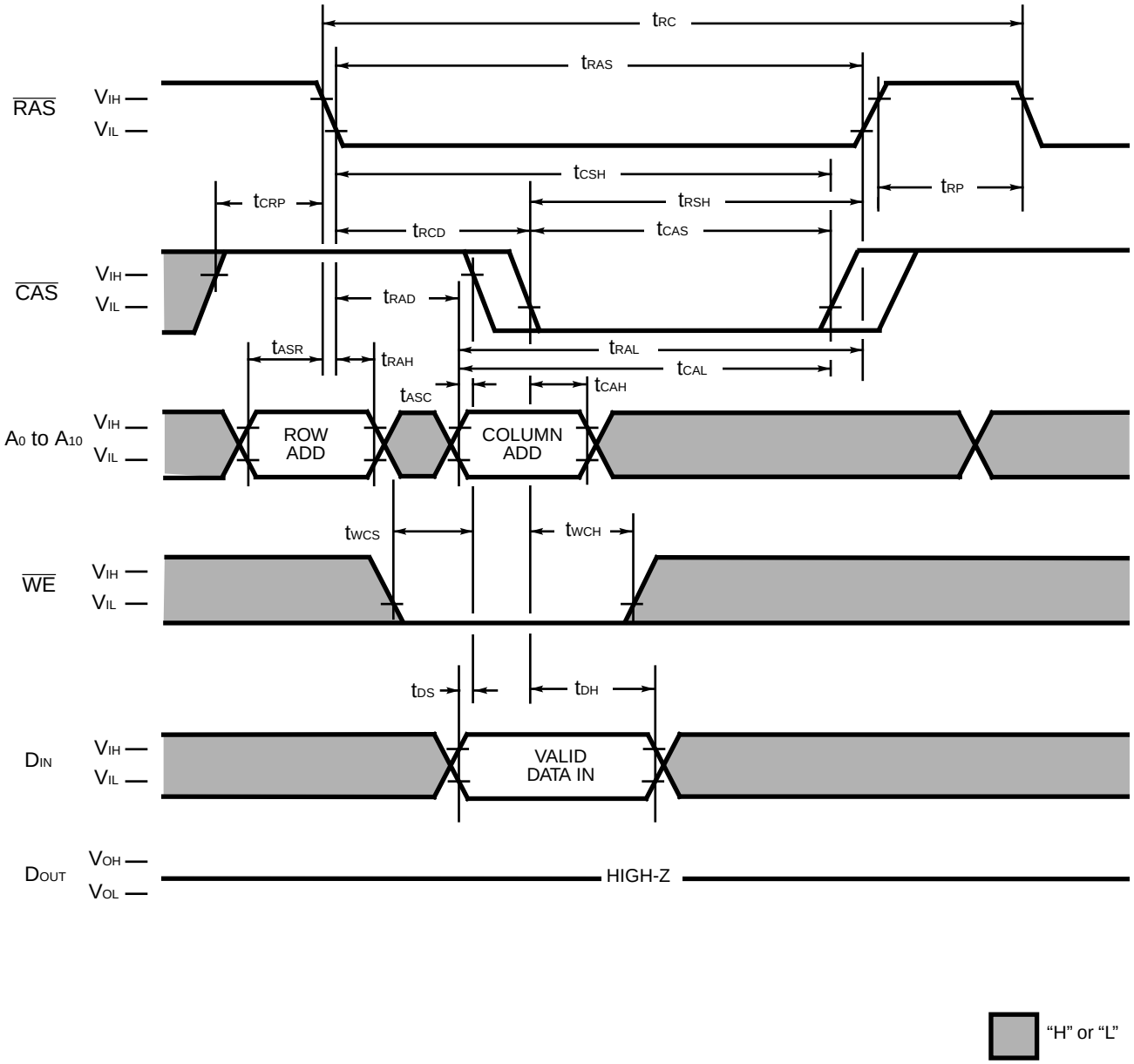
Fig. 5 - READ CYCLE



DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H" , the data becomes invalid after t_{OH} is satisfied. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), or Column address input (t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{AA}.

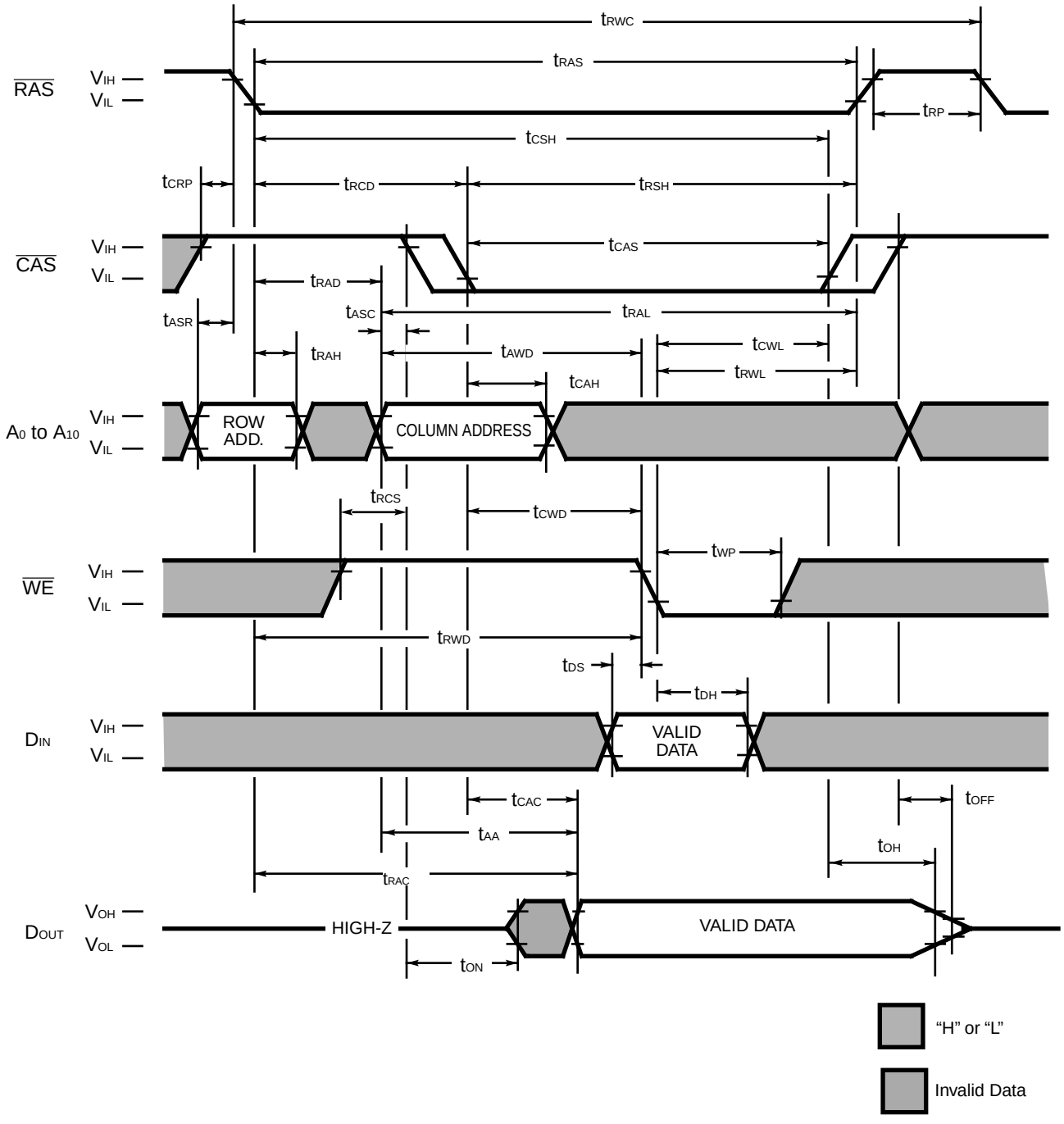
Fig. 6 - WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and D_{IN} pins. The data on D_{IN} pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, t_{RWL} and t_{RAL} must be satisfied with the specifications.

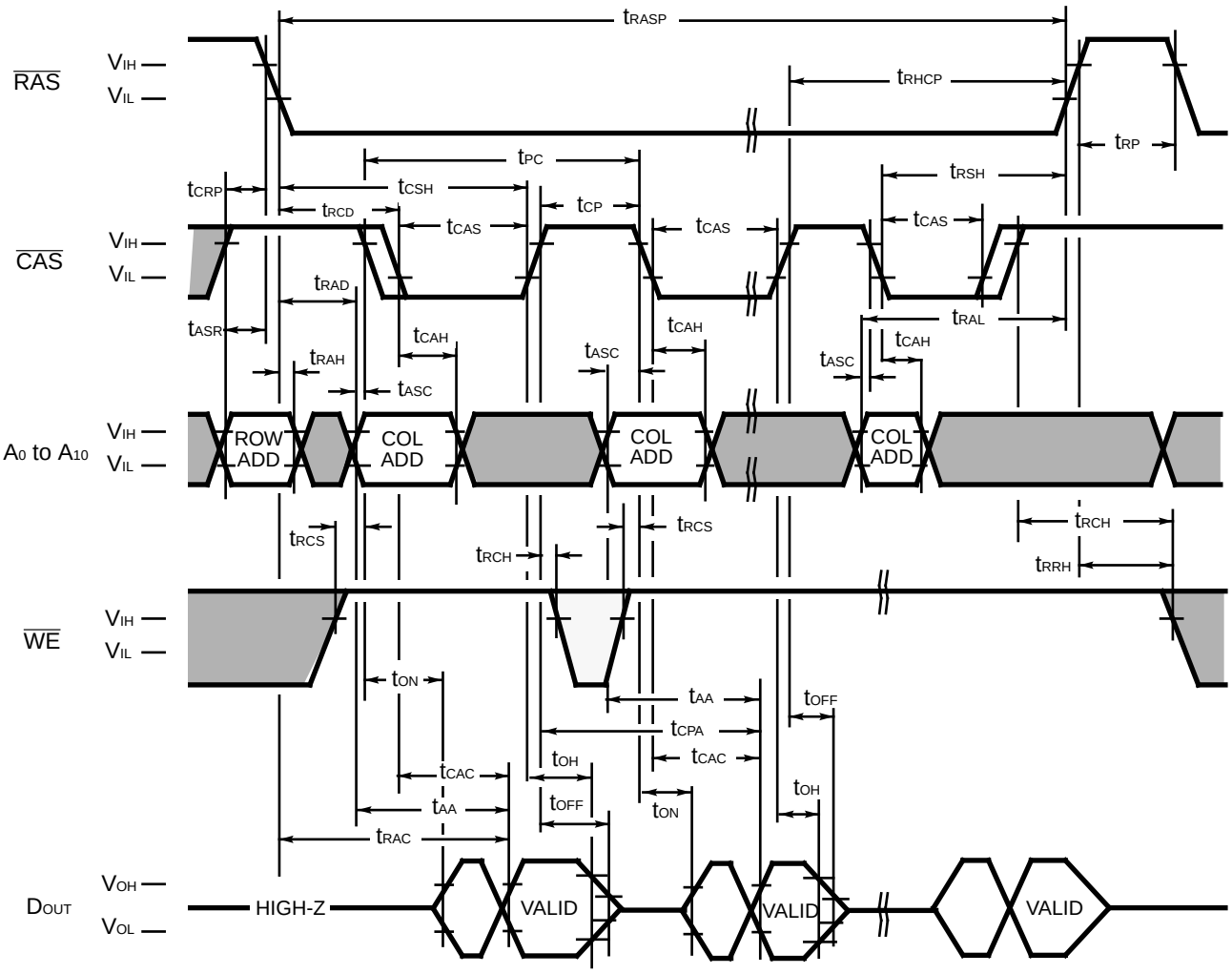
Fig. 7 - READ WRITE/READ-MODIFY-WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the D_{OUT} pin. After the current data is read out, modified data can be rewritten into the same address quickly.

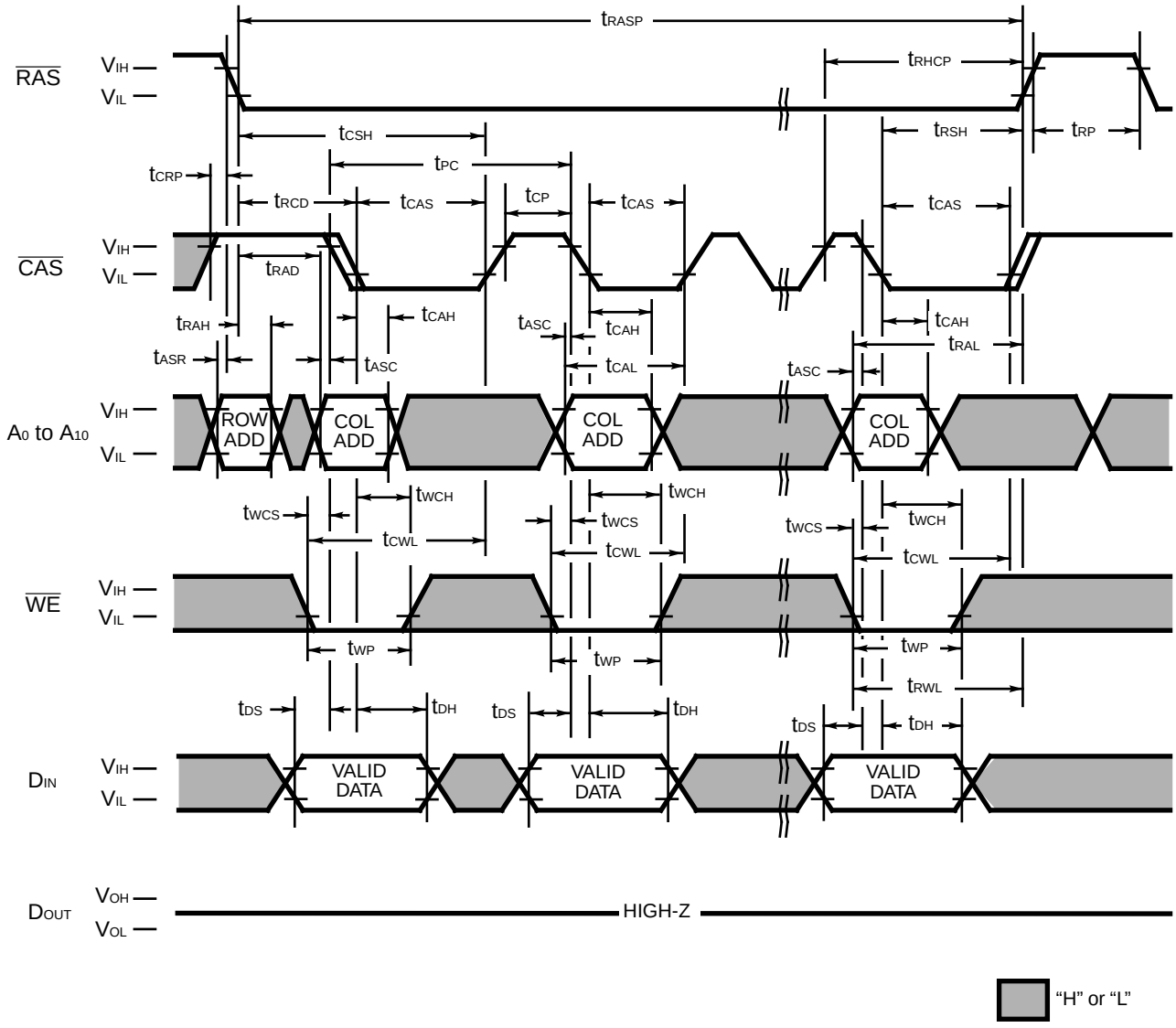
Fig. 8 - FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H" . Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occurs later. Any of the 2048 bits belonging to each row can be accessed.

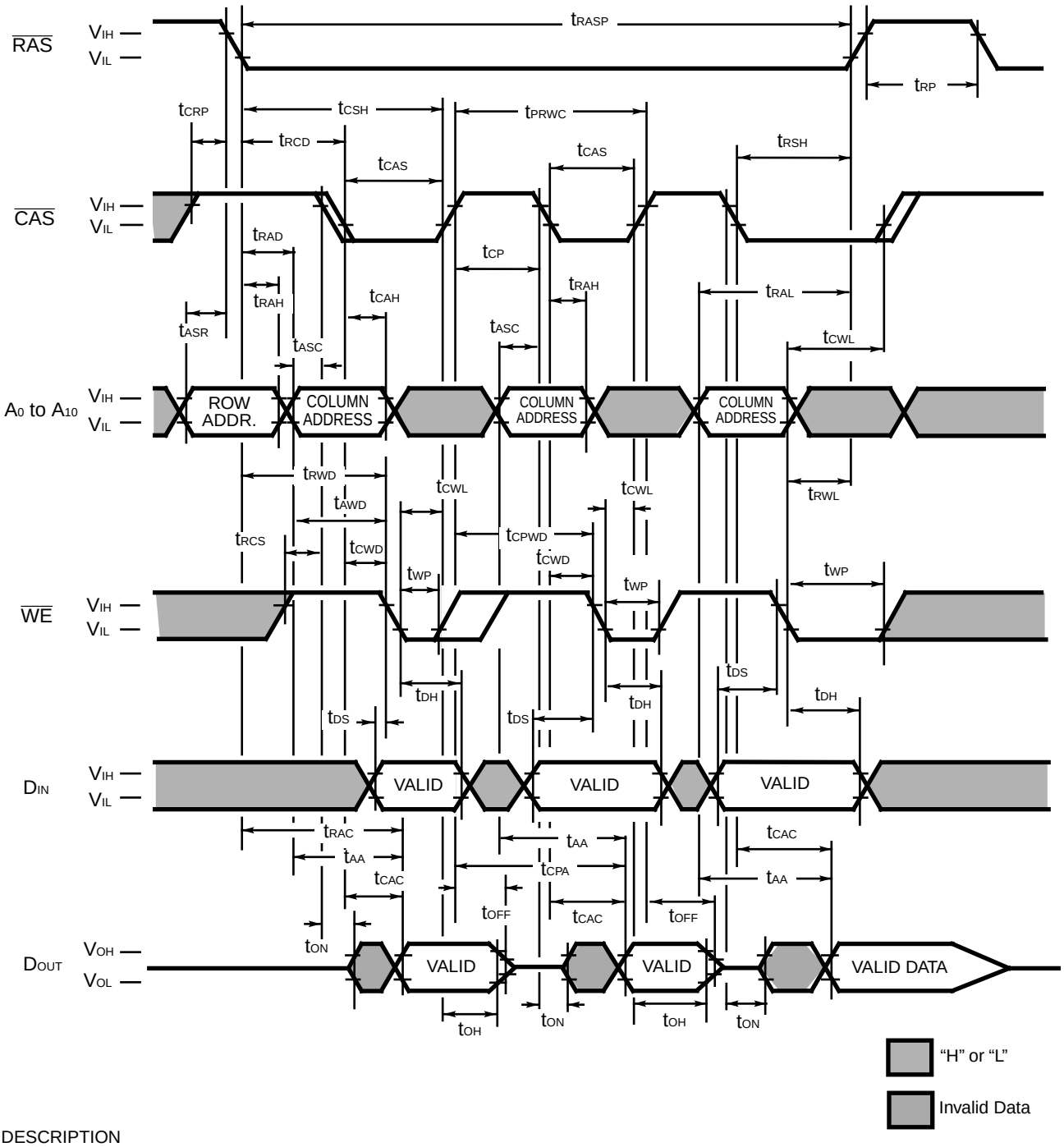
Fig. 9 - FAST PAGE MODE WRITE CYCLE (Early Write)



DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on D_{IN} pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, t_{CWL} must be satisfied. Any of the 2048 bits belonging to each row can be accessed.

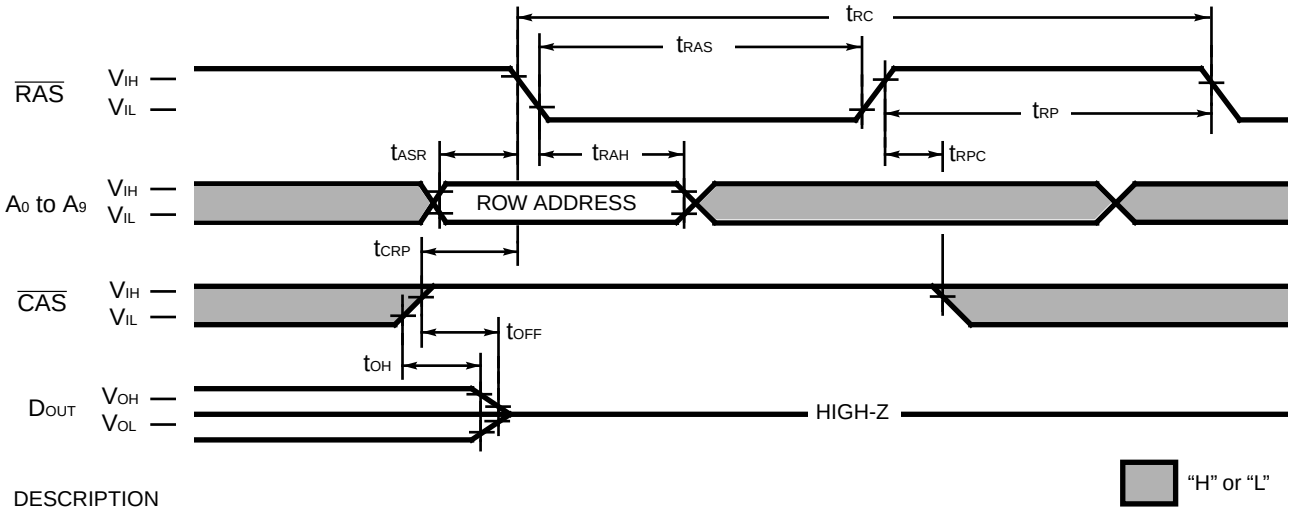
Fig. 10 - FAST PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During fast page mode, the read-modify-write cycle can be executed by changing $\overline{WE}$ high to low after the data appears at D_{OUT} pin as well as normal cycle. Any of the 2048 bits belonging to each row can be accessed.

Fig. 11 - $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$, D_{IN}, A_{10} = "H" or "L")

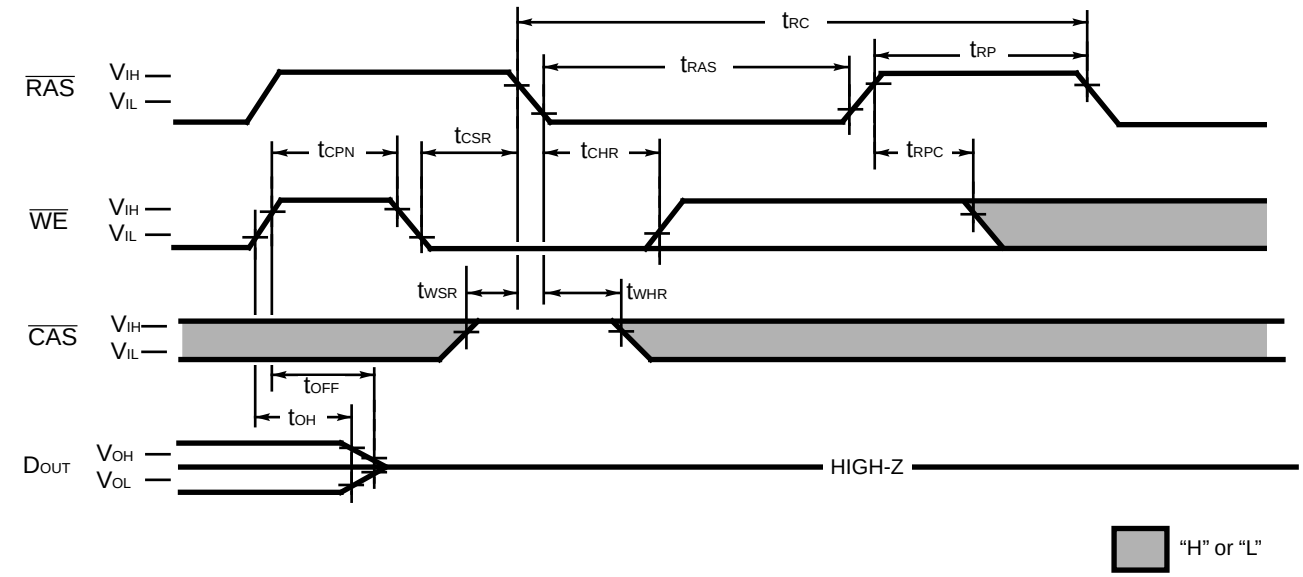


DESCRIPTION

The refresh of DRAM is executed by normal read, write or read-modify-write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 16.4 ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-written to the cell. The MB814100A has three types of refresh modes, $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

The $\overline{RAS}$ only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, the D_{OUT} pin is kept in a high impedance state.

Fig. 12 - $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (A_0 to A_{10}, D_{IN} = "H" or "L")

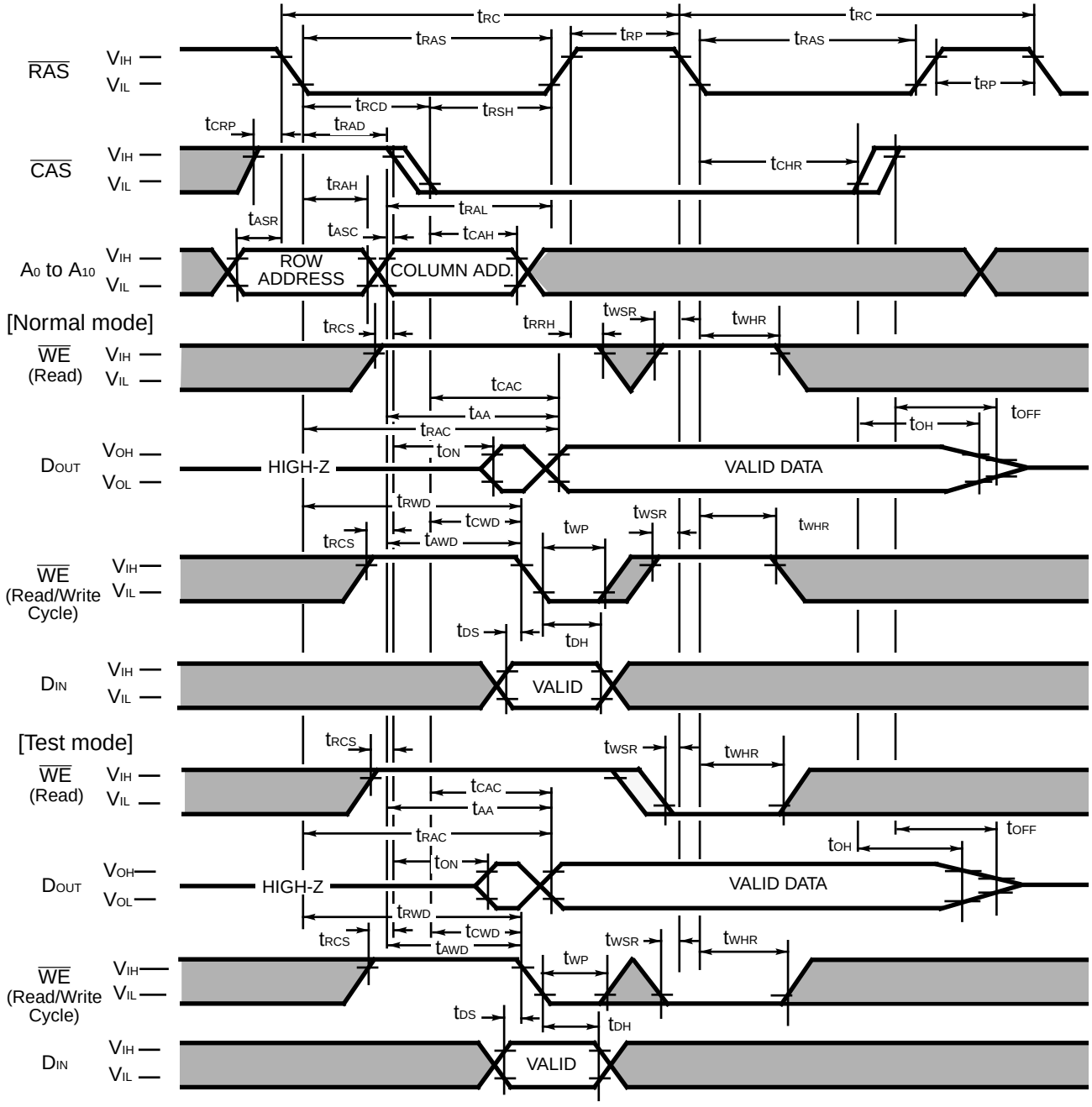


DESCRIPTION

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB814100A executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

$\overline{WE}$ must be held "H" for the specified set up time (t_{WSR}) before $\overline{RAS}$ goes "L" in order not to enter "test mode".

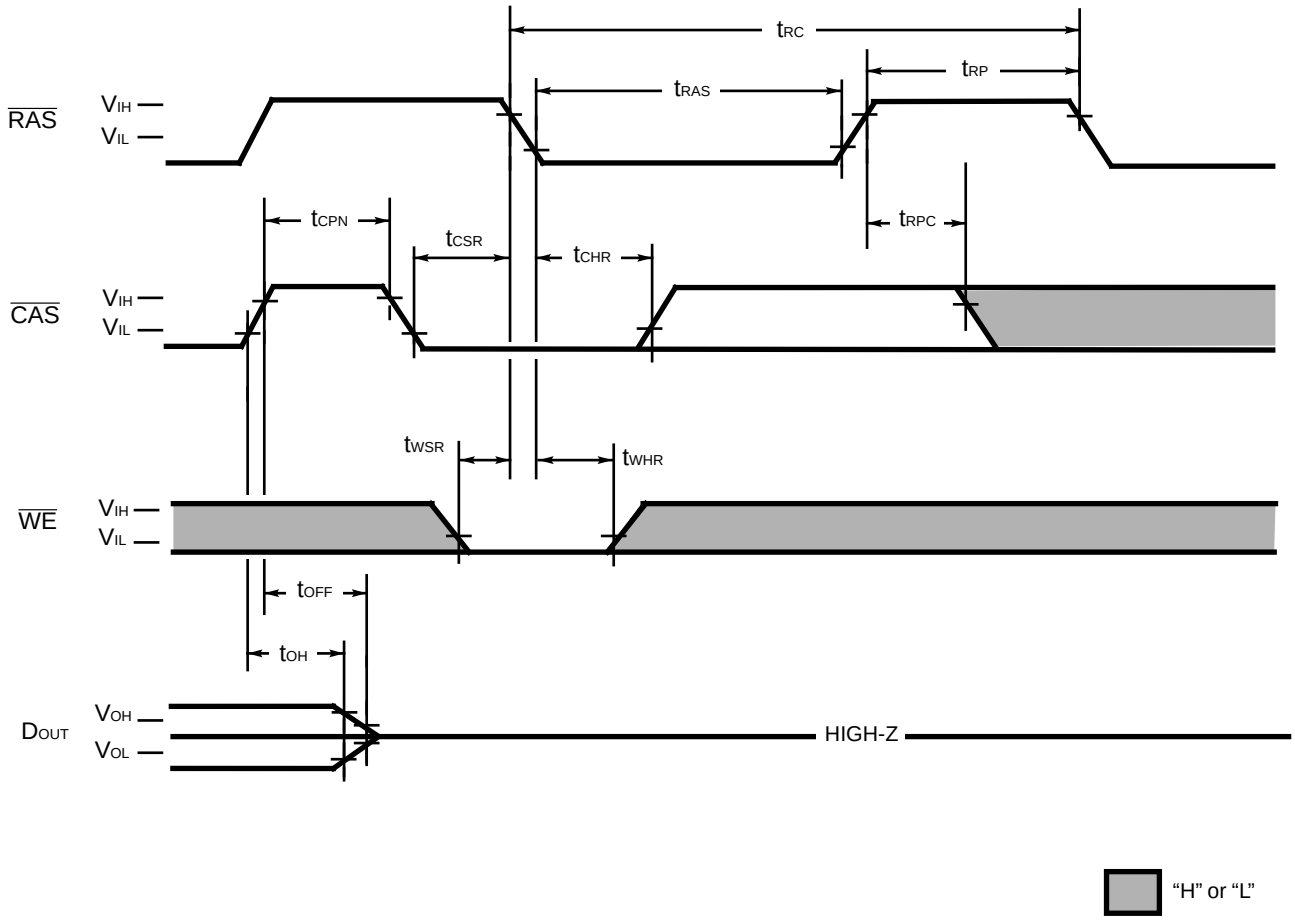
Fig. 13 - HIDDEN REFRESH CYCLE



DESCRIPTION

The hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.
$\overline{WE}$ must be held "H" for the specified set up time (t_{WSR}) before $\overline{RAS}$ goes "L" for the secound time in order not to enter "test mode" to be specified later.

Fig. 14 - TEST MODE SET CYCLE (A_0 to A_{10}, D_{IN} = ”H” or ”L”)



DESCRIPTION

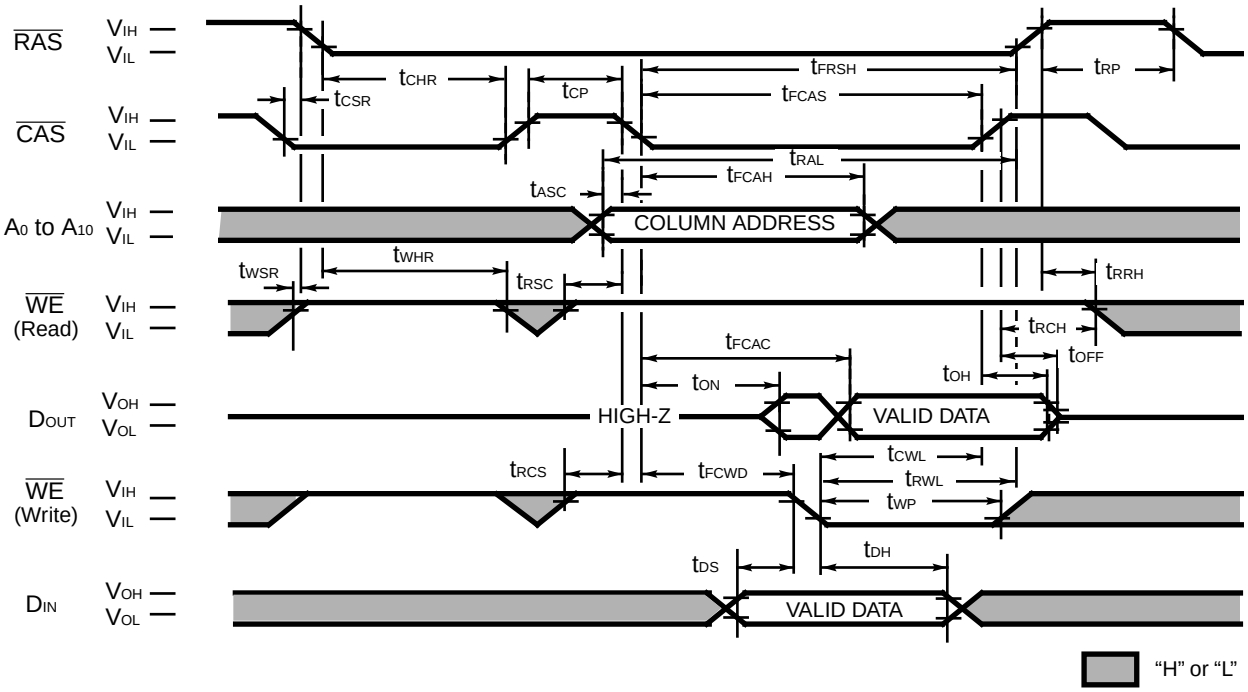
Test Mode ;

The purpose of this test mode is to reduce device test time to one eighth of that required to test the device conventionally.
The test mode function is entered by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh for the entry cycle.
In the test mode, read and write operations are executed in units of eights bits which are selected by the address combination of RA_{10}, CA_0 and CA_{10}. In the write mode, data at D_{IN} is written into eight cells simultaneously. In the read mode, eight cells at the selected addresses are read back and checked in the following manner.

When the eight bits are all ”L” or all ”H”, a ”H” level is output.
When the eight bits show a combination of ”L” and ”H”, a ”L” level is output.

The test mode function is exited by performing a $\overline{RAS}$-only refresh or a $\overline{CAS}$-before-$\overline{RAS}$ refresh for the exit cycle.
In test mode operation, the following parameters are delayed approximately 5ns from the specified value in the data sheet.
t_{RC}, t_{RWC}, t_{RAC}, t_{AA}, t_{RAS}, t_{CSH}, t_{RAL}, t_{RWD}, t_{AWD}, t_{PC}, t_{PRWC}, t_{CPA}, t_{RHCP}, t_{CPWD}

Fig. 15 - $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A_0 through A_{10} are defined by the on-chip refresh counter.
Column Address: Bits A_0 through A_{10} are defined by latching levels on A_0-A_9 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 1024 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 1024 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

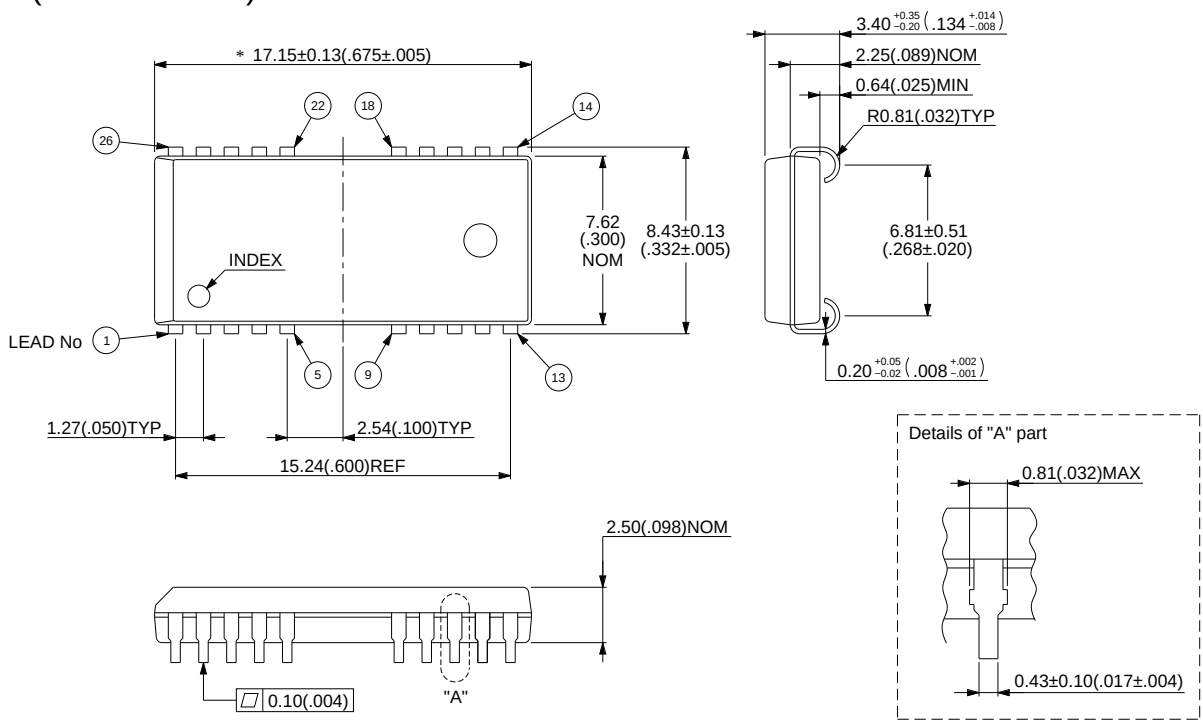
No.	Parameter	Symbol	MB814100A-60		MB814100A-70		MB814100A-80		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	50	—	55	—	60	ns
90	Column Address Hold	t_{FCAH}	30	—	30	—	35	—	ns
92	$\overline{CAS}$ to $\overline{WE}$ Delay	t_{FCWD}	50	—	55	—	60	—	ns
93	$\overline{CAS}$ Puls width	t_{FCAS}	50	—	55	—	60	—	ns
94	$\overline{RAS}$ Hold Time	t_{FRSH}	50	—	55	—	60	—	ns

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

■ PACKAGE DIMENTIONS

(Suffix: -PJN)

26 pin, Plastic SOJ
(LCC-26P-M04)

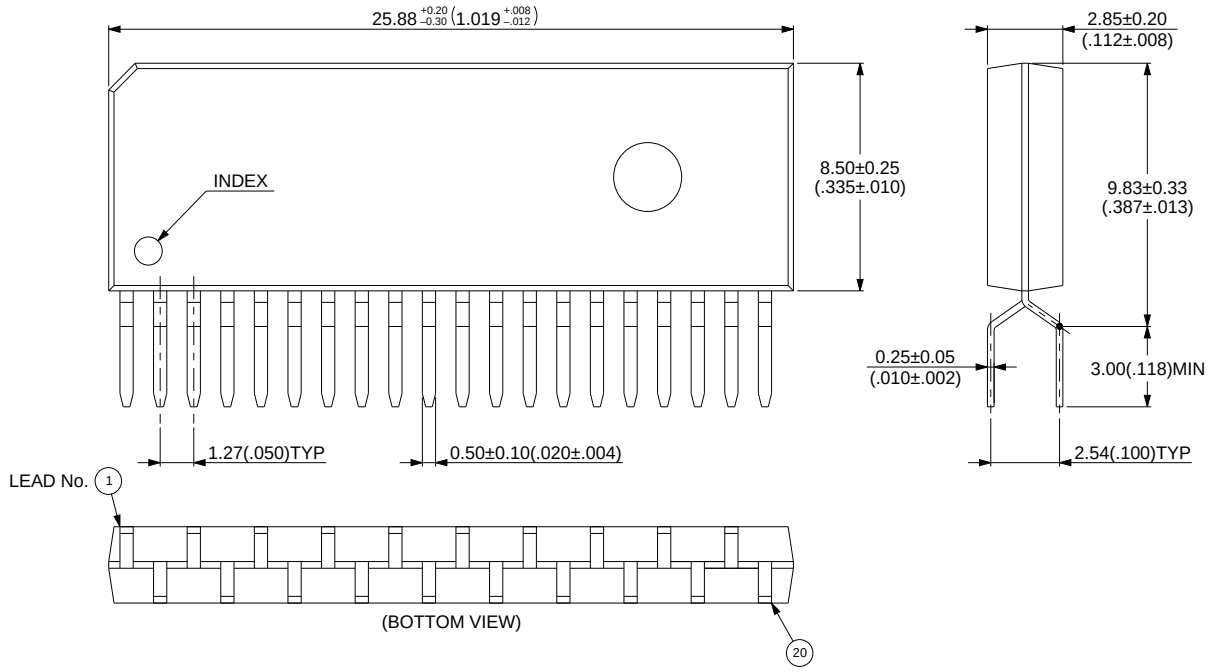


Dimensions in mm(inches).

■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PZ)

20 pin, Plastic ZIP
(ZIP-20P-M02)

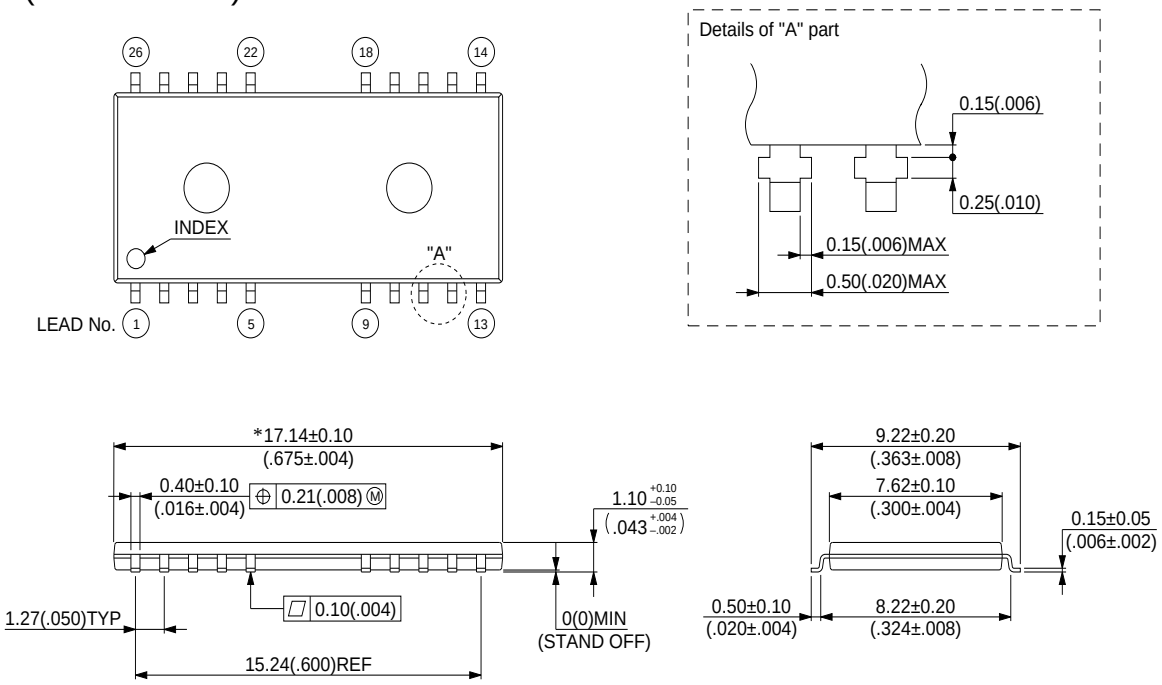


Dimensions in mm(inches).

■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

26 pin, Plastic TSOP(II)
(FPT-26P-M01)

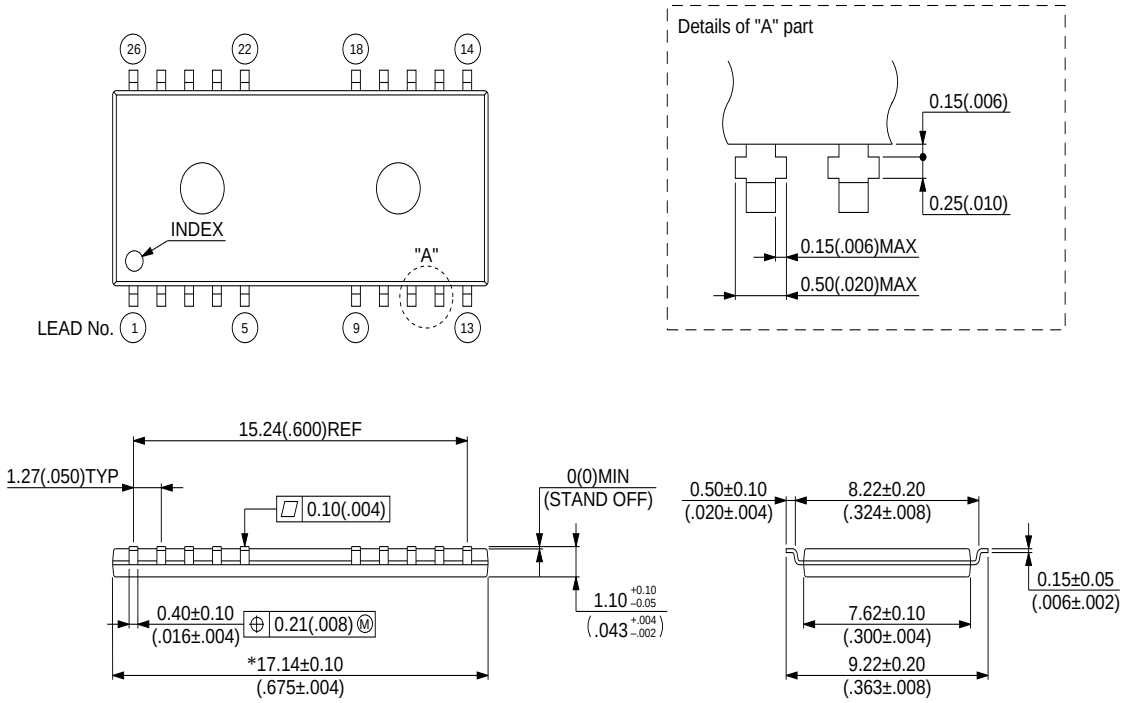


Dimensions in mm(inches).

■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)

26 pin, Plastic TSOP(II)
(FPT-26P-M02)



Dimensions in mm(inches).

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

F9703

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.