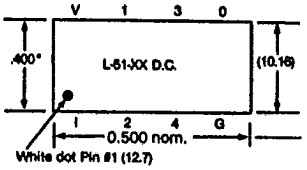
Active Delay Lines

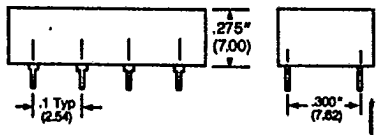
T-47-13

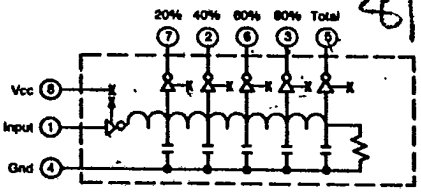
Delay Range 25 thru 500 nsec

STYLE L-51 (8 pins)

5 equally-spaced taps







Dimensions in inches (mm).

INPUT CONDITIONS
(See Page 3)

Operating Temp.....0° to +70°C
Storage Temp..... −55°C to +125°C
(All lines internally terminated)

I_{IH} Logic "1" Input Current.....50μA Max.
I_{IL} Logic "0" Input Current.... −2mA Max.
V_{OH} Logic "1" Voltage Out.....2.7V Min.
V_{OL} Logic "0" Voltage Out .....0.5V Max.

DRIVE CAPABILITIES
(TTL LOADS)

Logic "0" { 10 Loads/Tap Max.
20 Loads/Unit Max.

Logic "1" 20 Loads/Unit Max.

Supply Current ..... 75 mA Typ.
Voltage Range ..... 4.75V to 5.25V

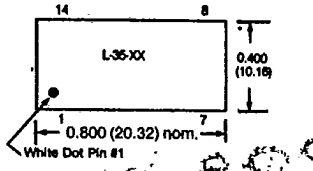
TOTAL DELAY (nsec ± 5%)	TAP INTERVALS (nsec*)	RISE TIME (ns MAX) (0.8 to 2.0V)	JBM P/N L-51-XX
25	5.0 ± 3ns	2.0	L-51-50
30	6.0 ± 3ns		L-51-51
35	7.0 ± 3ns		L-51-52
40	8.0 ± 3ns		L-51-53
45	9.0 ± 3ns		L-51-54
50	10.0 ± 3ns		L-51-55
75	15.0 ± 3ns		L-51-56
100	20.0 ± 3ns	2.0	L-51-57
150	30.0 ± 3ns	2.5	• L-51-58
200	40.0 ± 3ns	3.0	• L-51-59
250	50.0 ± 3ns	3.0	L-51-60
300	60.0 ± 5%	3.5	• L-51-61
350	70.0 ± 5%	3.5	L-51-62
400	80.0 ± 5%	4.0	• L-51-63
450	90.0 ± 5%	4.0	L-51-64
500	100.0 ± 5%	4.0	L-51-65

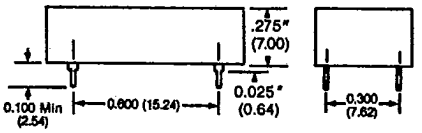
*25ns – 250ns TAP/TAP; 300ns – 500ns cumulative @ 25°C, 5.00VDC.
Delays may change 2% or 1ns for a respective 5% increase or decrease in supply voltage.

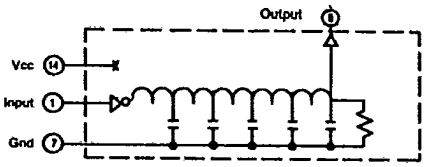
Delay Range 5 thru 1000 nsec

STYLE L-35 (14-pin outline)

Untapped







Dimensions in inches (mm).

TOTAL DELAY (nsec)	RISE TIME (ns MAX) (.8 to 2.0V)	JBM P/N L-35-XX
5 ± 1ns	2.0	L-35-00
7		L-35-01
10		L-35-02
15		L-35-03
20 ± 1ns		L-35-04
25 ± 5%		L-35-05
30		L-35-06
40		L-35-07
50		L-35-08
70		L-35-09
100		L-35-10
150	2.0	L-35-11
200	3.0	• L-35-12
300	3.5	• L-35-13
400	4.0	• L-35-14
500	4.0	L-35-15
600	4.5	• L-35-25
700	4.5	L-35-26
750	4.5	L-35-27
800	5.0	• L-35-28
900	5.0	L-35-29
1000 ± 5%	5.0	L-35-30

Consult factory for other delays, tolerances, and logic families.