

2M x 32 DRAM Module

Features

- 72-Pin Single-In-Line Memory Module

- Performance:

		-60	-70
t_{RAC}	RAS Access Time	60ns	70ns
t_{CAC}	CAS Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Manufactured with 16Mb DRAMS (2M x 8)
- Thin outline (.104")
- Single 5V $\pm$ 0.5V Power Supply

- Low current consumption
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$ -Only, CBR, and Hidden Refresh
- 2098 refresh cycles distributed across 32ms
- 11/10 Addressing (Row/Column)
- Optimized for use in byte-write, non-parity applications
- Tin/lead versions only
- DRAMs in TSOP package

Description

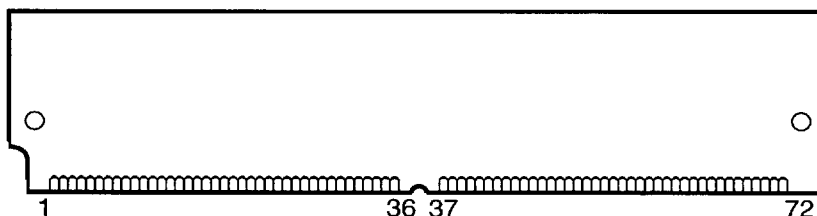
The IBM11D2320H is an 8MB 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 2Mx32 high speed memory array and is configured as one 2Mx32 bank. The assembly is intended for use in 16, 32 and 64 bit applications. It is manufactured with four 2Mx8 devices, each in a 400mil TSOP pkg. and is compatible with applica-

tions that support 11/10 (Row/Column) addressing.

The use of TSOP packages allows tight SIMM spacing (.3" on center).

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint.

Card Outline



2M x 32 DRAM Module**Pin Description**

$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

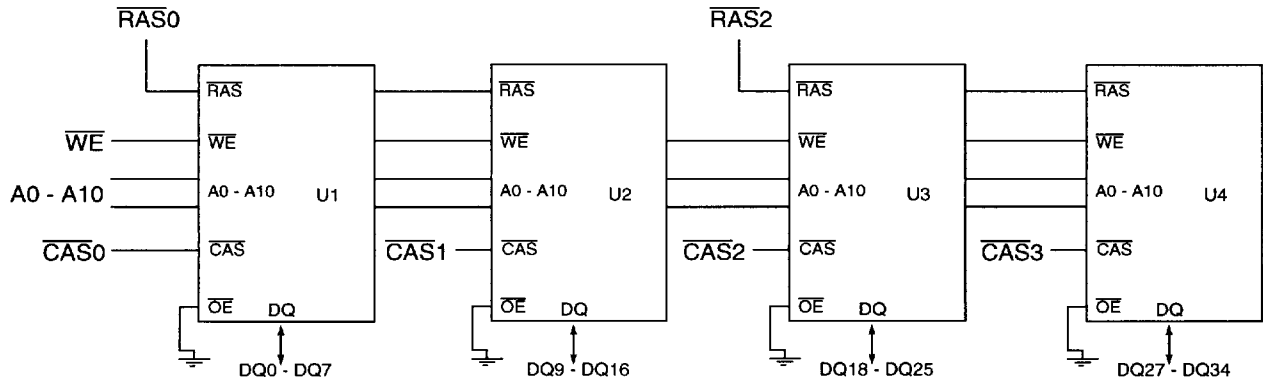
Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	25	DQ24	49	DQ9
2	DQ0	26	DQ7	50	DQ27
3	DQ18	27	DQ25	51	DQ10
4	DQ1	28	A7	52	DQ28
5	DQ19	29	NC	53	DQ11
6	DQ2	30	V_{CC}	54	DQ29
7	DQ20	31	A8	55	DQ12
8	DQ3	32	A9	56	DQ30
9	DQ21	33	NC	57	DQ13
10	V_{CC}	34	$\overline{\text{RAS2}}$	58	DQ31
11	NC	35	NC	59	V_{CC}
12	A0	36	NC	60	DQ32
13	A1	37	NC	61	DQ14
14	A2	38	NC	62	DQ33
15	A3	39	V_{SS}	63	DQ15
16	A4	40	$\overline{\text{CAS0}}$	64	DQ34
17	A5	41	$\overline{\text{CAS2}}$	65	DQ16
18	A6	42	$\overline{\text{CAS3}}$	66	NC
19	A10	43	$\overline{\text{CAS1}}$	67	PD1
20	DQ4	44	$\overline{\text{RAS0}}$	68	PD2
21	DQ22	45	NC	69	PD3
22	DQ5	46	NC	70	PD4
23	DQ23	47	$\overline{\text{WE}}$	71	NC
24	DQ6	48	NC	72	V_{SS}

1. DQ numbering is compatible with a non-parity (x36) SIMM.

Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimensions	Notes
IBM11D2320H-60	2M x 32	60ns	11/10	Sn/Pb	4.25" x 1" x .104"	
IBM11D2320H-70		70ns				
IBM11D2320H-60T		60ns				1
IBM11D2320H-70T		70ns				1
1. DRAM package designator appended to speed portion of part number on assemblies beginning with DRAM die rev E.						

Block Diagram



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Truth Table

Function	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Row Address	Column Address	All DQ bits
Standby	H	H→X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{\text{RAS}}$ -Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh	H→L	L	H	X	X	High Impedance
Hidden Refresh	Read	L→H→L	H	Row	Col	Data Out
	Write	L→H→L	L	Row	Col	Data In

Presence Detect

Pin	2M x 32	
	-60	-70
PD1	NC	NC
PD2	NC	NC
PD3	NC	V _{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min ($V_{CC} + 0.5$, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min ($V_{CC} + 0.5$, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.98	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A = 0$ to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	$V_{CC} + 0.5$	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS} .
2. V_{IH} may overshoot to $V_{CC} + 2.0\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ (or $V_{CC} + 1.0\text{V}$ for $\leq 8.0\text{ns}$). Additionally, V_{IL} may undershoot to -2.0V for pulse widths $\leq 4.0\text{ns}$ (or -1.0V for $\leq 8.0\text{ns}$). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance ($T_A = 0$ to $+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$)

Symbol	Parameter	2M x 32 Max	Units
C_{I1}	Input Capacitance (A0-A10)	30	pF
C_{I2}	Input Capacitance ($\overline{\text{RAS}}$)	24	pF
C_{I3}	Input Capacitance ($\overline{\text{CAS}}$)	17	pF
C_{I4}	Input Capacitance ($\overline{\text{WE}}$)	38	pF
$C_{I/O}$	Output Capacitance (All DQ)	15	pF

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DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$)

Symbol	Parameter		2M x 32		Units	Notes
			Min	Max		
I_{CC1}	Operating Current	-60	—	360	mA	1, 2, 3
	Average Power Supply Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: $t_{RC} = t_{RC \text{ min}}$)	-70	—	320		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{IH}$)		—	4	mA	
I_{CC3}	$\overline{\text{RAS}}$ Only Refresh Current	-60	—	360	mA	1, 3
	Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{IH}$: $t_{RC} = t_{RC \text{ min}}$)	-70	—	320		
I_{CC4}	EDO Mode Current	-60	—	200	mA	1, 2, 3
	Average Power Supply Current, EDO Mode ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, Address Cycling: $t_{HPC} = t_{HPC \text{ min}}$)	-70	—	160		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$)		—	4	mA	
I_{CC6}	$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current	-60	—	360	mA	1, 3
	Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Cycling: $t_{RC} = t_{RC \text{ min}}$)	-70	—	320		
$I_{i(L)}$	Input Leakage Current	$\overline{\text{RAS}}$	-20	+20	μA	
	Input Leakage Current, any input ($0.0 \leq V_{IN} \leq (V_{CC} - 6.0\text{V})$)	$\overline{\text{CAS}}$	-10	+10		
	All Other Pins Not Under Test = 0V	All others	-40	+40		
$I_{o(L)}$	Output Leakage Current (D_{OUT} is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$)		-10	+10	μA	
V_{OH}	Output High Level Output "H" Level Voltage ($I_{OUT} = -5\text{mA}$)		2.4	V_{CC}	V	
V_{OL}	Output Low Level Output "L" Level Voltage ($I_{OUT} = +4.2\text{mA}$)		0.0	0.4	V	

1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
 2. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
 3. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$. In the case of I_{CC4} , it can be changed once or less when $\overline{\text{CAS}} = V_{IH}$.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0V ± 0.5V)

- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
- An initial pause of 100μs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
- AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	40	—	50	—	ns	
t _{CP}	$\overline{\text{CAS}}$ Precharge Time	10	—	10	—	ns	
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	60	10K	70	10K	ns	
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	15	10K	20	10K	ns	
t _{ASR}	Row Address Setup Time	0	—	0	—	ns	
t _{RAH}	Row Address Hold Time	10	—	10	—	ns	
t _{ASC}	Column Address Setup Time	0	—	0	—	ns	
t _{CAH}	Column Address Hold Time	10	—	10	—	ns	
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	45	20	50	ns	1
t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	30	15	35	ns	2
t _{RSH}	$\overline{\text{RAS}}$ Hold Time	15	—	20	—	ns	
t _{CSH}	$\overline{\text{CAS}}$ Hold Time	60	—	70	—	ns	
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	ns	
t _{DZC}	$\overline{\text{CAS}}$ Delay Time from D _{IN}	0	—	0	—	ns	
t _{AR}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	—	—	—	—	ns	3
t _T	Transition Time (Rise and Fall)	3	30	3	50	ns	
- Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}. - Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}. - This timing parameter is not applicable to this product, but applies to a related product in this family.							

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Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	—	—	—	—	ns	1
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	12	—	15	—	ns	

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 3
t_{AA}	Access Time from Address	—	30	—	35	ns	2, 3
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	3
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	—	15	—	15	ns	5

1. Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. The $t_{RCD}(\max)$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled by t_{CAC} .

2. Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. The $t_{RAD}(\max)$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .

3. Measured with the specified current load and 100pF.

4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

5. $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

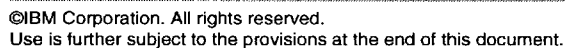
Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2
1. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{CPA} , t_{AA} . 2. Access time assumes a load of 100pF.							

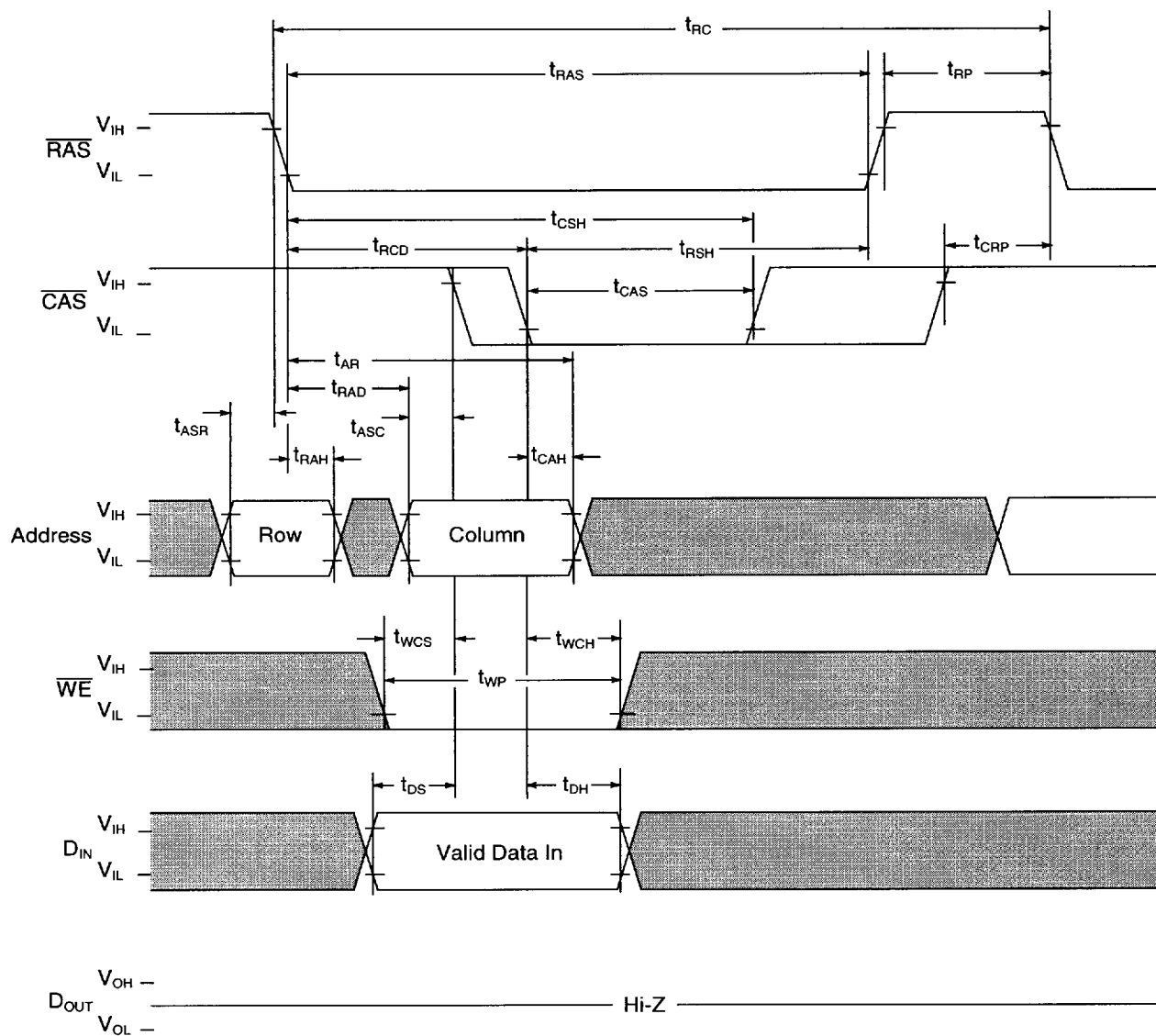
Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1
1. 2048 refreshes are required every 32ms.							

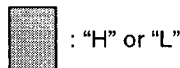
Read Cycle



Write Cycle (Early Write)

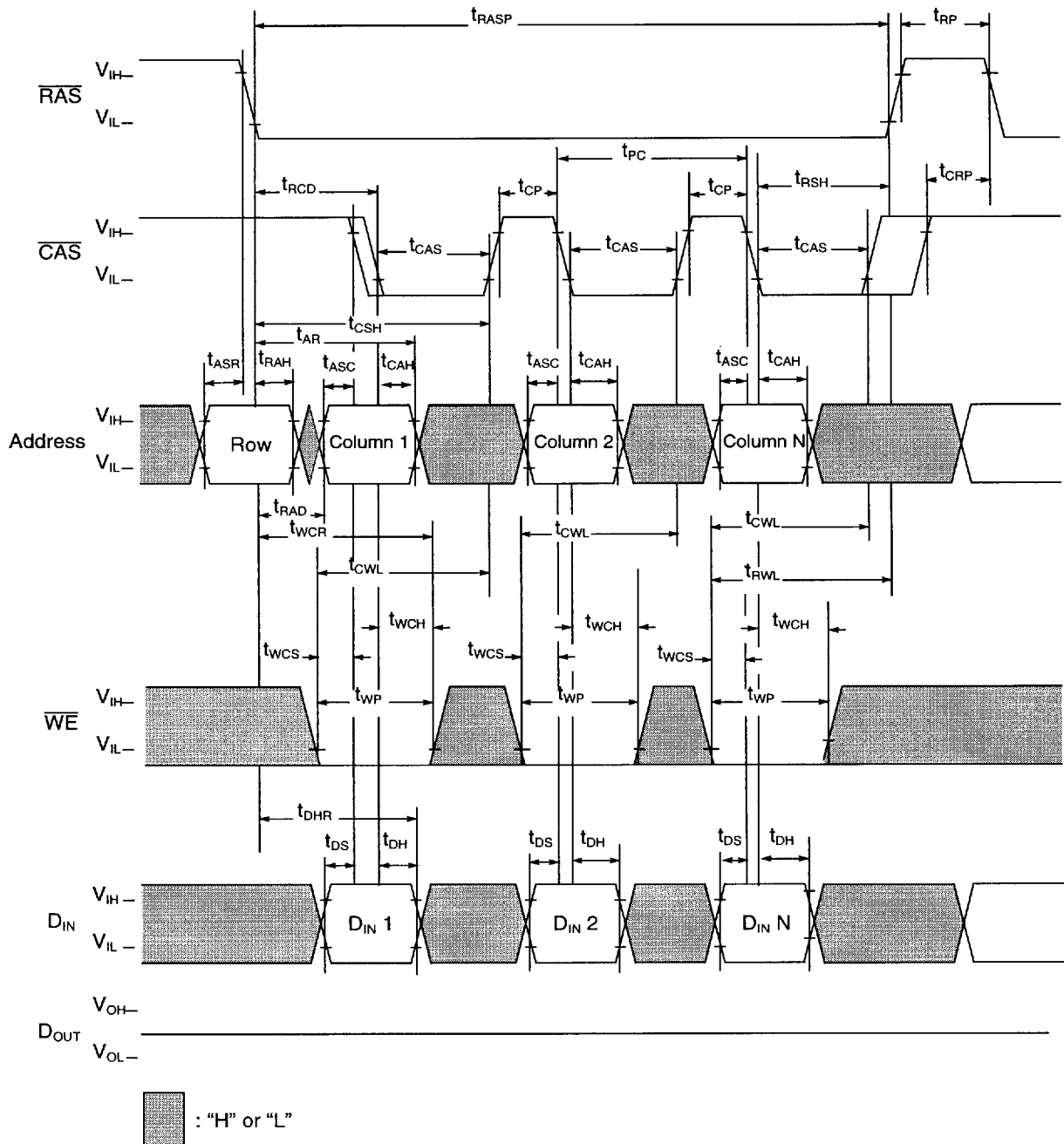


■ : "H" or "L"

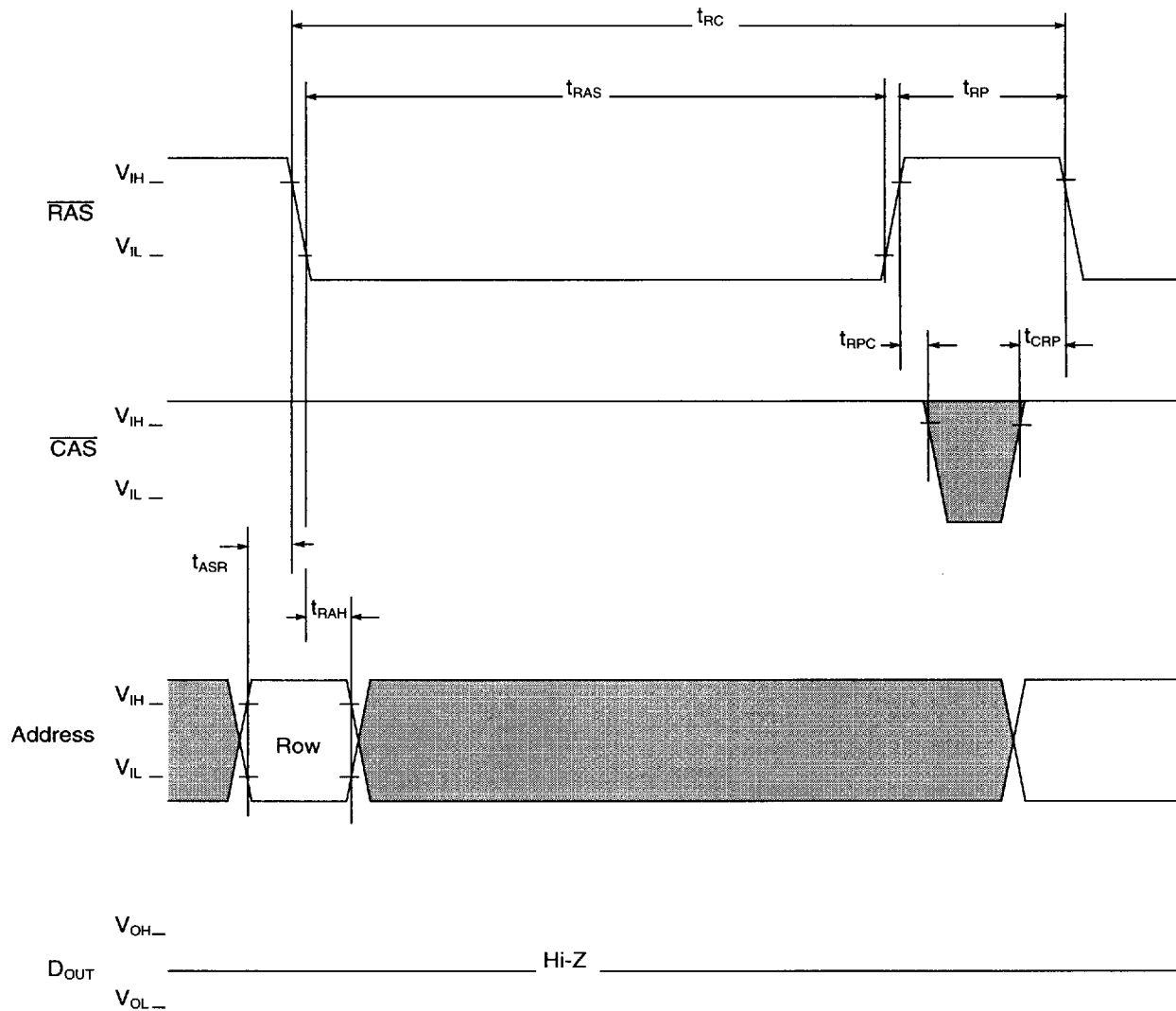


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Fast Page Mode Write Cycle



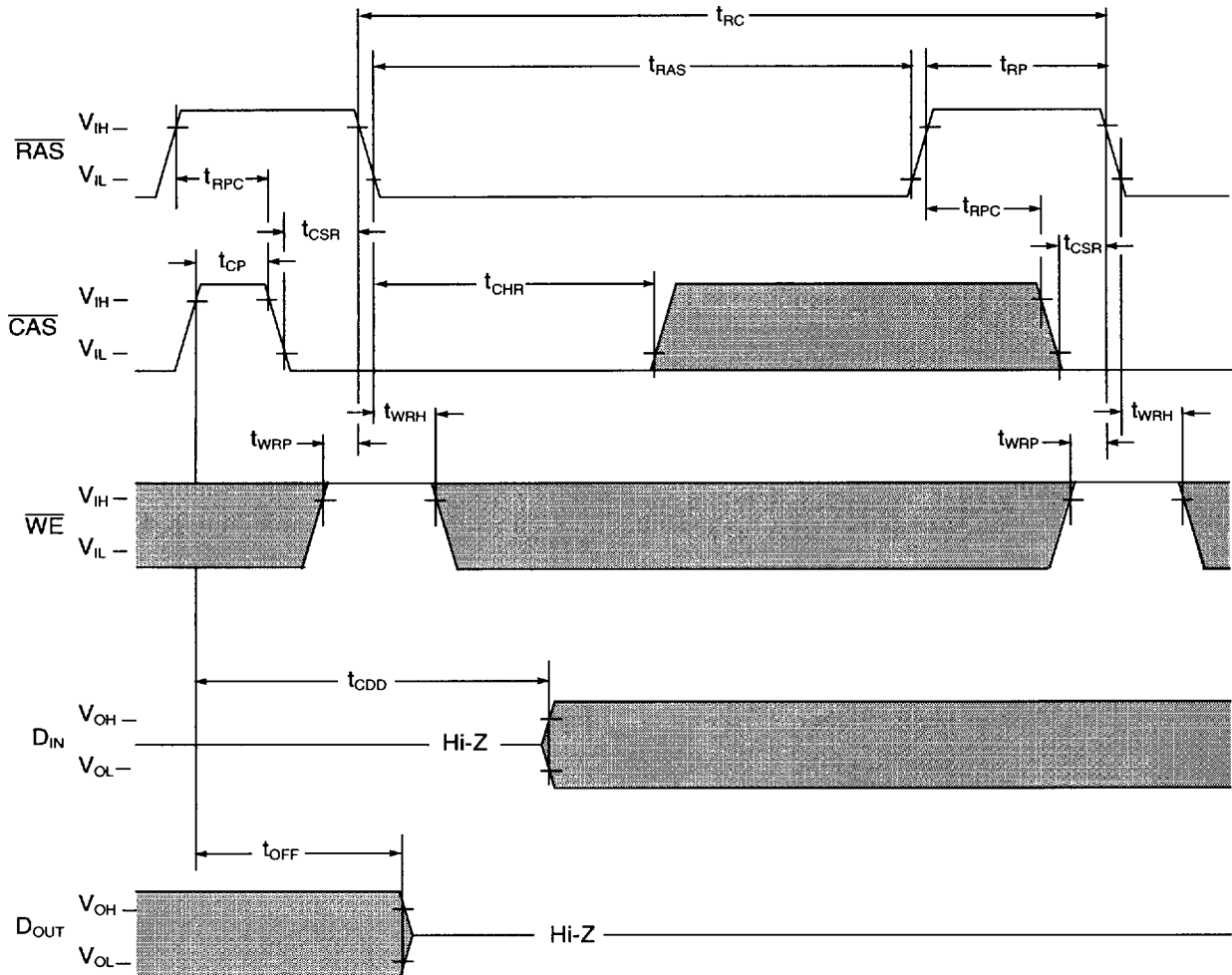
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RAS Only Refresh Cycle

 : "H" or "L"

Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

CAS Before RAS Refresh Cycle

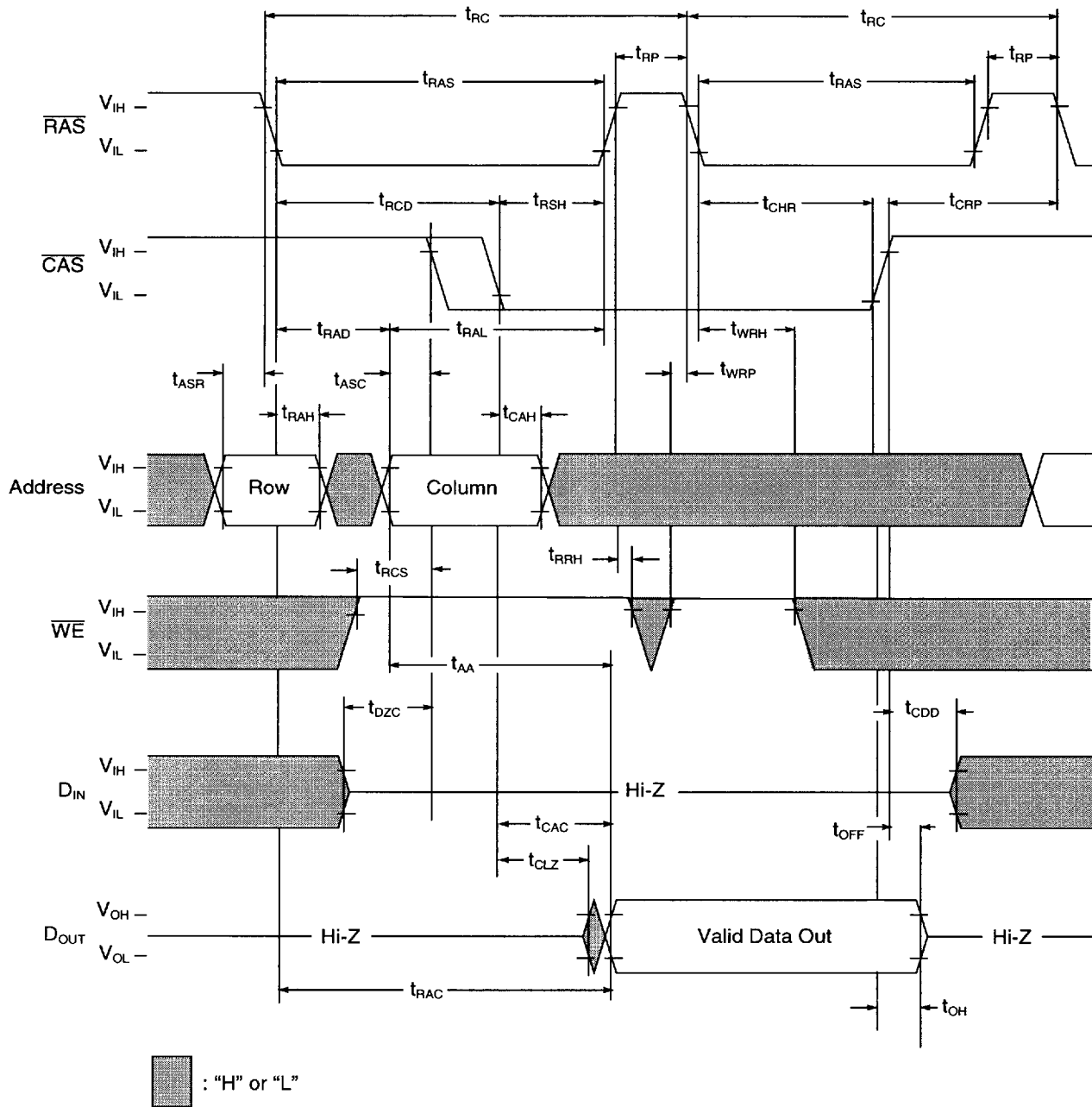


: "H" or "L"

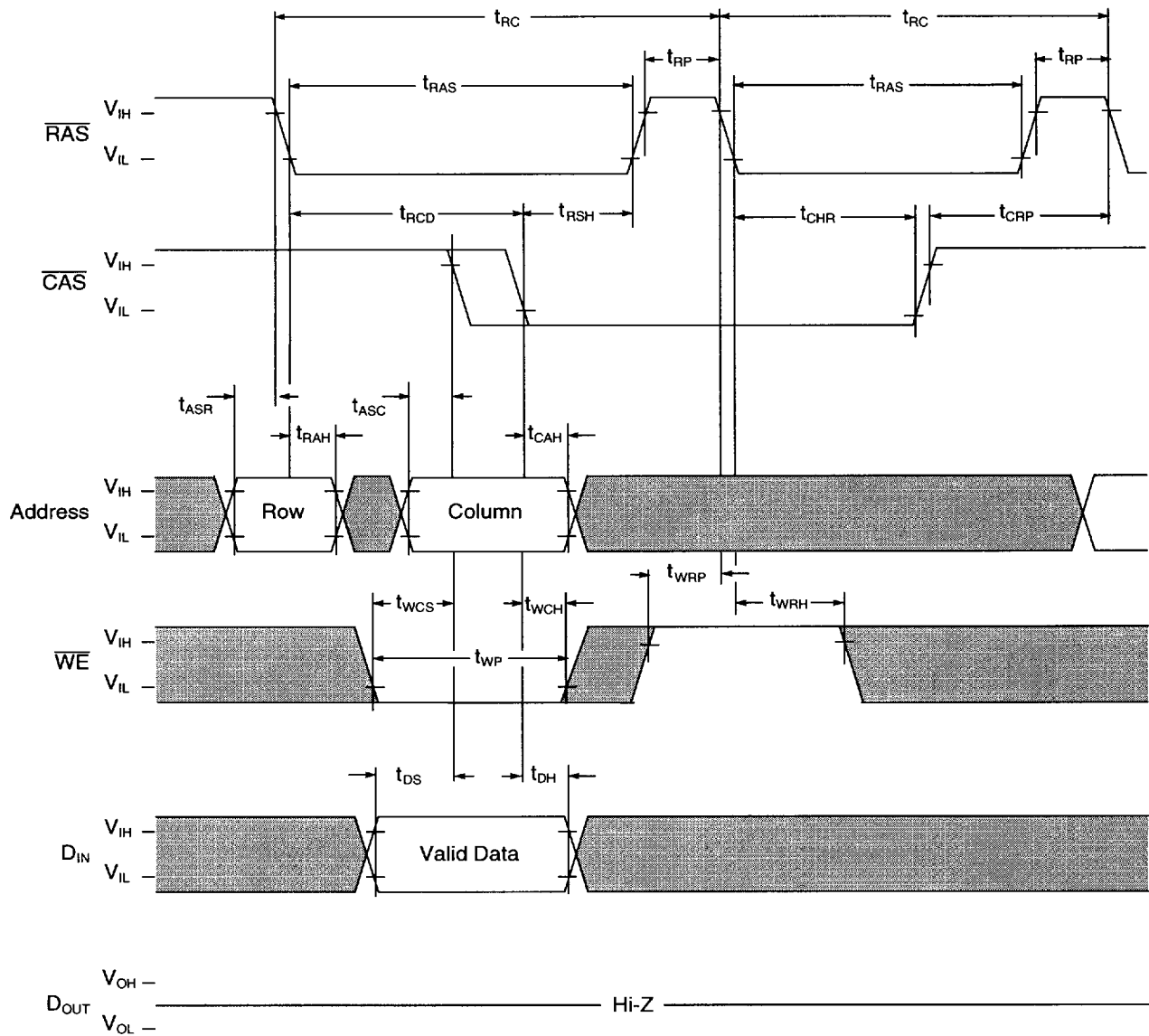
NOTE: Address is "H" or "L"

2M x 32 DRAM Module

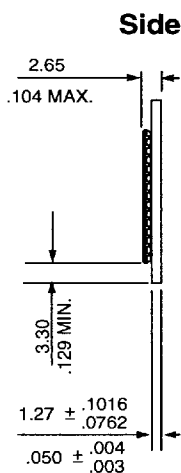
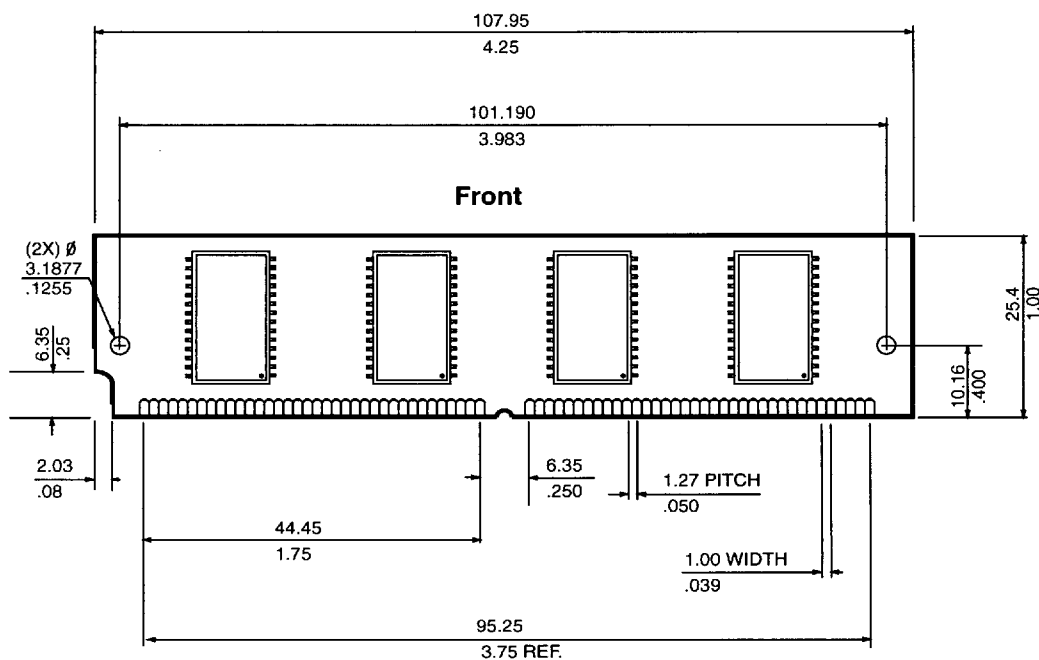
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Layout Drawing



Millimeters	Inches
1	0.039
2	0.079
3	0.118
4	0.157
5	0.197
6	0.236
7	0.276
8	0.315
9	0.354
10	0.394
11	0.433
12	0.472
13	0.512
14	0.551
15	0.591
16	0.630
17	0.669
18	0.709
19	0.748
20	0.787
22	0.866
24	0.945
25	0.984
26	1.024
28	1.103
30	1.182
32	1.261
34	1.340
36	1.419
38	1.498
40	1.578
42	1.657
44	1.736
46	1.815
48	1.894
50	1.973
52	2.053
54	2.132
56	2.211
58	2.290
60	2.369
62	2.448
64	2.528
66	2.607
68	2.687
70	2.766
72	2.845
74	2.925
76	3.004
78	3.083
80	3.153
82	3.232
84	3.311
86	3.391
88	3.470
90	3.549
92	3.629
94	3.708
96	3.787
98	3.866
100	3.945



Revision Log

Rev	Contents of Modification
3/96	Initial release.
6/96	Added package description to speed designation Updated ordering information
8/96	Corrected typo's