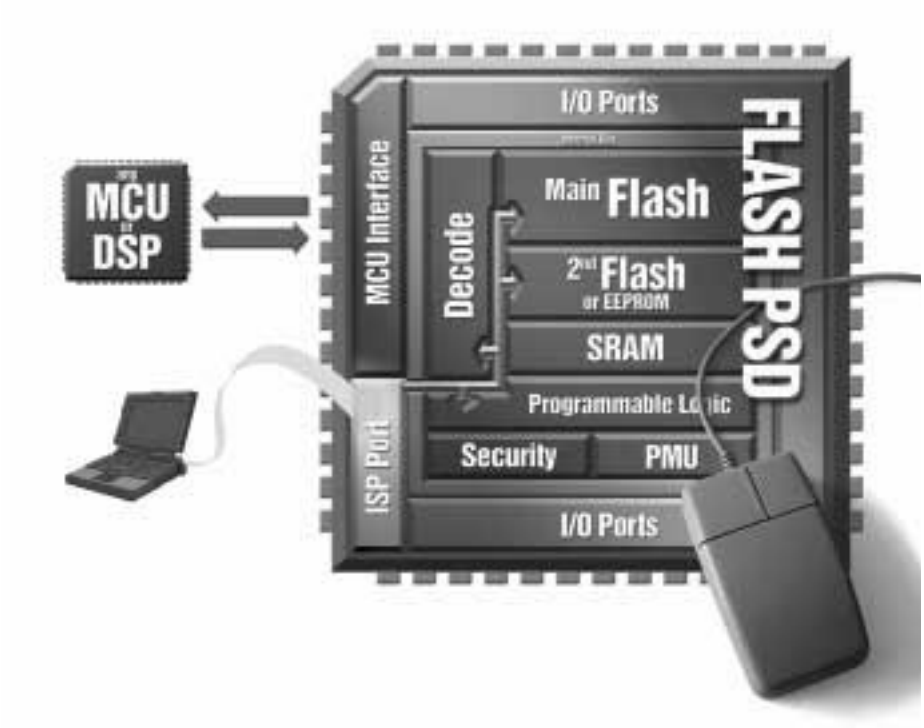
JTAG-ISP Information: Flash PSD

Application Note AN054

Aug, 2000

Revision 2.1



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Contents

1 Introduction

The flash PSD family (PSD8XX, PSD9XX, PSD4XXX) offers In-System Programming (ISP) allowing a completely blank PSD device to be programmed while soldered to a circuit board. This eliminates the need for sockets, bed-of-nails programming, maintaining an inventory of pre-programmed devices, and developing embedded microcontroller firmware for programming blank flash memory. While this simplifies manufacturing, JTAG-ISP is also a very cost effective way to implement firmware updates to end products after they are deployed in the field.

2 Specifications

Flash PSDs comply with the core requirements of the IEEE 1149.1 JTAG specification. However, flash PSDs do not support boundary scan functions. Instead, flash PSDs support In-System Programming using the JTAG channel.

Flash PSDs implement a "pseudo" boundary scan function in that they allow the manipulation of their I/O port pins (not all pins) through special JTAG-ISP commands. This means that the pins on PSD ports may be set to logic HI, LOW, or to HI-Z using these JTAG-ISP commands. This is a key feature to have when the PSD controls chip selects of other devices on the circuit board and these devices must be in a certain state during an ISP session. For example, it may be required to force certain chip select signals for other devices to their inactive state while the PSD is being programmed with the JTAG-ISP channel.

Flash PSDs may reside in a JTAG chain with other JTAG 1149.1 compliant devices.

3 Software

PSDsoft 2000 and PSDsoft Express (referred to in this document as PSDsoft) are MS Windows-based applications used for developing PSD designs and for driving the JTAG-ISP interface. For each design project, PSDsoft will produce a single data programming file (object file) to program into a PSD, which contains the PSD configuration as well as the microcontroller firmware.

The industry standard Boundary Scan Definition Language file (BSDL) defines the pins, JTAG operating modes, and internal registers of a JTAG device. This is needed by JTAG testing and programming equipment. A BSDL file for each flash PSD may be found in a directory installed with PSDsoft. See \PSDsoft\bsdl for PSDsoft 2000 and \PSDexpress\bsdl for PSDsoft Express.

4 JTAG-ISP Programming Support

Currently, only the Waferscale FlashLINK cable supports programming flash PSDs using the JTAG-ISP channel. Third party JTAG-ISP vendors will be identified on our website in the future.

FlashLINK is a low cost JTAG-ISP cable that plugs into any PC/laptop parallel port. The target system may operate at 2.7 to 5.5 VDC and the FlashLINK cable "adapts" automatically with no user configuration needed. FlashLINK is controlled by PSDsoft and will support device

chaining of multiple PSDs and devices from other manufacturers. The JTAG BYPASS mode is supported to facilitate chaining devices from other manufacturers.

FlashLINK may be purchased from our website for $59 USD with a credit card. FlashLINK may also be purchased as part of flash PSD development kits; see website for details.

There are several third-party insertion programmers (non JTAG-ISP programmers) available for programming flash PSDs listed on our website.

5 Enhanced ISP function

Waferscale is the first company to directly program the contents of flash memory with a JTAG interface. Until now, industry supported JTAG-ISP of programmable logic devices only, which have many fewer locations to program than memory devices. Because of the size of the flash memory in PSDs, Waferscale had to devise an optimized solution for ISP to reduce programming time. As a result, the scheme employs the optional use of two additional pins beside the four standard JTAG pins.

Standard JTAG pins: TCK, TMS, TDI, TDO
Optional JTAG-ISP pins: TSTAT, TERR\

These two optional JTAG-ISP pins facilitate hardware flow control for rapid exchange of data. In addition, the flash PSD internally incorporates a JTAG-ISP burst mode that increments the address pointer automatically between data accesses as well as data pipelining. These elements greatly reduce the programming time of the memory-intense PSD devices.

It is important to know that the two flags, TSTAT and TERR\, are still available when only four pins are used. In this case the flags are scanned out serially. Although this is not as optimal as using six pins, there is still a huge performance gain over using traditional industry ISP methods.

The TSTAT signal represents the immediate status of the current action in progress. For example, TSTAT = 0 means the current programming/erasing of a particular byte or sector is not complete, TSTAT = 1 means the action is finished.

The TERR\ signal represents one of two error conditions. Either a timeout of an attempt to program/erase a byte or sector has occurred or an attempt was made to program a “1” to a Flash memory bit that was already a “0” (remember that Flash memory erases to a “1” and is programmed to a “0”). This signal will relieve the device programmer of the task of waiting on a worst-case maximum timeout for an error condition. As soon as the device programmer sees TERR\ go active, it will stop and handle the error.

It is required that TSTAT and TERR\ be used together, not individually. TSTAT and TERR\ signals may be configured to operate in an open-drain mode to facilitate the chained connection of several flash PSD devices together on the same circuit board. See Section 9 of this document for details on chaining devices.

6 Program/Erase Flow Control

There are two ways to manage the control of data flowing between a JTAG device programmer (FlashLINK) and a flash PSD device. PSDsoft allows a choice of these methods by using four JTAG-ISP pins or six JTAG-ISP pins.

6.1 Four JTAG-ISP pins – TCK, TMS, TDI, TDO

This method involves scanning out the information on the internal flags, TSTAT and TERR\ over the standard four JTAG lines (TCK, TMS, TDI, TDO). These flags are important when programming and erasing flash memory. As flash memory ages (near and above 100,000 erase cycles), it takes longer to program and erase individual flash cells. If there were no status flags like TSTAT and TERR\, FlashLINK would not know how long to wait for an individual program or erase cycle to complete, so it would have to wait the maximum worst case time for each flash location (1200 usec!). That's 44 hours for a 128 Kbyte memory. But typical programming times for PSD flash locations is 14 usec each, which is 1.8 seconds for 128 Kbytes of memory. You can expect to see these short program and erase times throughout the life of a flash PSD.

6.2 Six JTAG-ISP pins – TCK, TMS, TDI, TDO, TSTAT, TERR\

FlashLINK will access the TSTAT and TERR\ handshake signals directly at the PSD pins for each program/erase action. Since the information at the TSTAT and TERR\ pins do not have to be scanned out serially, it is faster than using four pins. For a single PSD in a JTAG chain, using six pins is 10% to 15% faster than four pins. If there are many devices in the JTAG chain (PSDs or other devices), the benefits of using six pins is greater since the scan path is longer. It is advised to use six pins in any design if you can afford the two extra pins, especially for PSD4000 series and PSD835/935 devices since the memory density is higher and there are abundant I/O pins available.

7 JTAG-ISP Connection Schemes

Most PSD designers choose to use dedicated JTAG-ISP pins. This means that the pins always function as JTAG-ISP, and not multiplexed with other I/O signal functions. In fact, to be completely compliant with IEEE 1149.1, JTAG pins must be dedicated to JTAG functions at all times.

PSD designers choose to use six dedicated JTAG-ISP pins rather than four pins to reduce JTAG-ISP programming time by 10% to 15%. Many PSD813/833/913 designers use only four JTAG-ISP pins because there is less memory to program. Most PSD834/835/934/935 and PSD4000 series designers use six JTAG-ISP pins because the larger memories take longer to program. See Section 7.1 for details on four dedicated JTAG-ISP pins, and section 7.2 for six pins.

The JTAG-ISP pins on PSD8XX and PSD4235 devices can be multiplexed with general I/O functions. This is helpful when many general I/O pins are needed in the system and there are not

quite enough I/O pins on the PSD. Typically, multiplexing JTAG-ISP pins is done only with the PSD8XX family and not the PSD4235. The PSD4235 has abundant I/O pins. Multiplexing JTAG-ISP pins is not supported on the PSD9XX family or the PSD4135. See Section 7.3 for details on multiplexing JTAG-ISP pins. Most users of PSDs do not multiplex JTAG-ISP pins. Instead, they configure the pins in PSDsoft to be dedicated to JTAG-ISP at all times.

On a blank flash PSD device, the four standard JTAG-ISP pins (TCK, TMS, TDI, TDO) are active and ready for JTAG functions. PSDs are shipped from the factory in a fully erased (blank) condition with JTAG-ISP pins enabled.

7.1 Four Dedicated JTAG-ISP Pins

Figure 1 shows the connections for four dedicated JTAG-ISP pins. This is the most basic connection scheme.

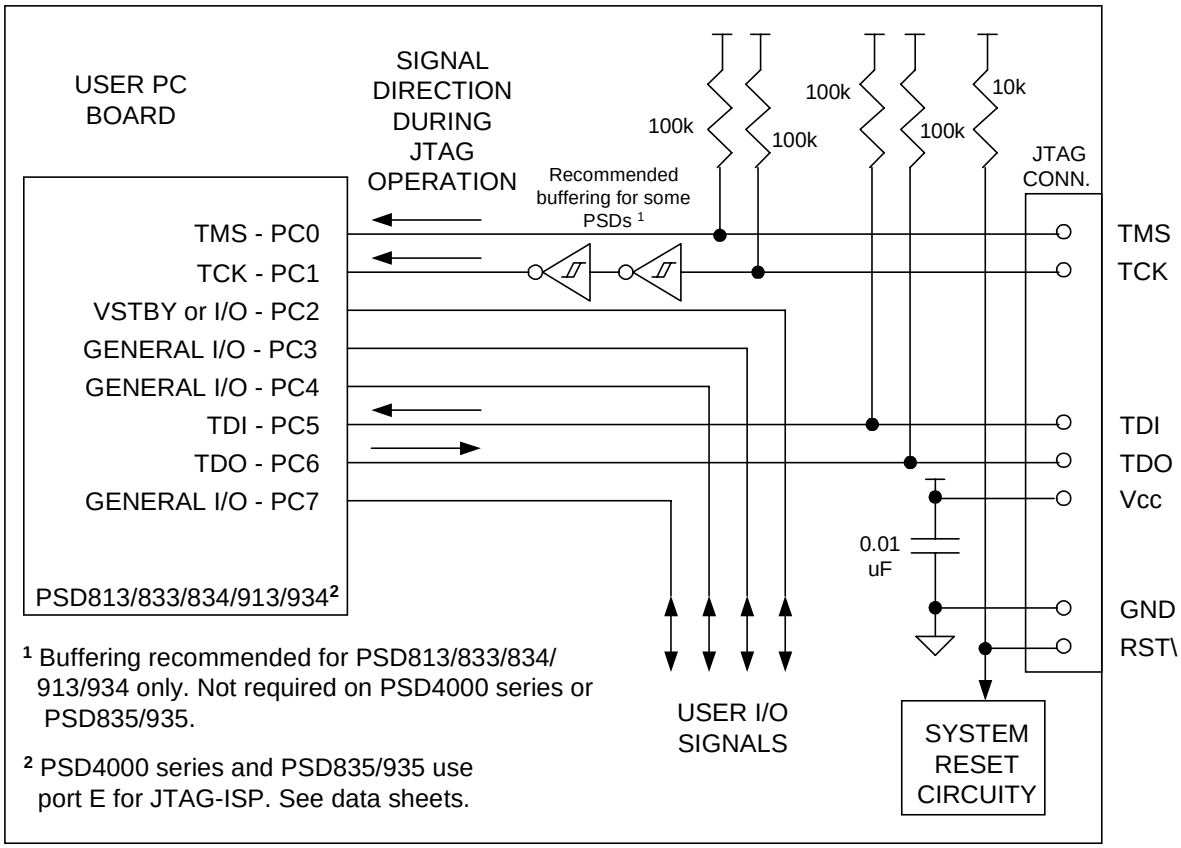


Figure 1 - Dedicated JTAG-ISP signals (basic four signals only)

Additional notes:

- The default setting in PSDsoft is four dedicated JTAG pins, non-multiplexed.

- It is highly recommended to connect RST\ from FlashLINK into your system reset. All memory inside of the PSD is inaccessible to the microcontroller during JTAG-ISP operations. As such, the microcontroller will fetch garbage and behave unpredictably.

PSDsoft automatically drives the RST\ signal active during all JTAG operations, which will hold the microcontroller in a safe state of reset when needed. As a convenience, PSDsoft will also drive RST\ active when the reset "button" is clicked with a mouse. The RST\ signal is driven from FlashLINK active low and open-collector, with a 10K pullup to Vcc.

- Vcc (2.7V to 5.5V) from the target system must be routed to the JTAG-ISP connector to supply to the FlashLINK cable assembly (15 mA max at 5.5 V). It is recommended to position a decoupling capacitor (0.01uF) between Vcc and GND at the JTAG-ISP connector.

- Schmitt-trigger buffering on the TCK input is recommended for PSD813/833/834/913/934 devices to reduce the chance of false TCK transitions from spikes or slow ramp rates. The PSD4000 series and PSD835/935 need no external buffering because their TCK input is Schmitt buffered in silicon.

- It is recommended to place pullups (values 10K to 100k) on all the JTAG-ISP signals lines as shown.

7.2 Six Dedicated JTAG-ISP Pins

Programming with six JTAG-ISP is 10% to 15% faster than four pins when a single PSD device is in a JTAG chain. Six-pin configuration reduces programming time even more when several devices are included in a JTAG chain. Figure 2 show the connections for six dedicated JTAG-ISP pins.

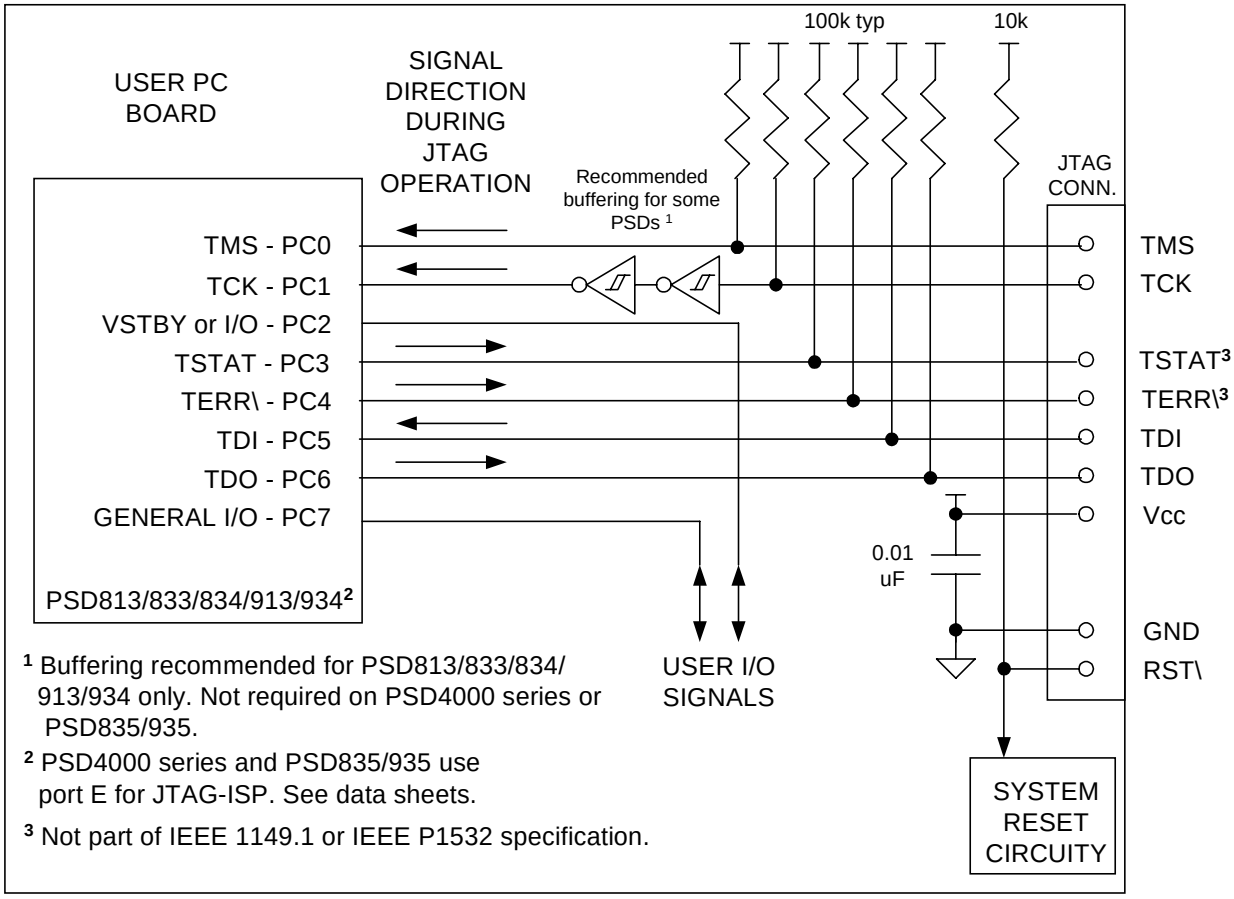


Figure 2 – Dedicated JTAG-ISP signals (all six signals)

Additional notes:

- The default setting in PSDsoft is four dedicated JTAG pins, non multiplexed. Click on either signal tstat or _terr (they work in a pair only) in the PSDsoft Pin Definition screen to get a total of six JTAG-ISP pins. Then click Add.

- It is highly recommended to connect RST\ from FlashLINK into your system reset. All memory inside of the PSD is inaccessible to the microcontroller during JTAG-ISP operations. As such, the microcontroller will fetch garbage and behave unpredictably. PSDsoft automatically drives the RST\ signal active during all JTAG operations, which will hold the microcontroller in a safe state of reset when needed. As a convenience, PSDsoft will also drive RST\ active when the reset "button" is clicked with a mouse. The RST\ signal is driven from FlashLINK active low and open-collector, with a 10K pullup to Vcc.

- Vcc (2.7V to 5.5V) from the target system must be routed to the JTAG-ISP connector to supply to the FlashLINK cable assembly (15 mA max at 5.5 V). It is recommended to position a decoupling capacitor (0.01uF) between Vcc and GND at the JTAG-ISP connector.

- Schmitt-trigger buffering on the TCK input is recommended for PSD813/833/834/913/934 devices to reduce the chance of false TCK transitions from spikes or slow ramp rates. The PSD4000 series and PSD835/935 need no external buffering because their TCK input is Schmitt buffered in silicon.

- It is recommended to place pullups (values 10K to 100k) on all the JTAG-ISP signals lines as shown.

7.3 Multiplexed JTAG-ISP Pin Functions

PSD9XX devices, the PSD4135G2, or PSDsoft Express does not support multiplexing JTAG-ISP signals. Multiplexing is available on PSD8XX devices and the PSD4235G2 using PSDsoft 2000.

If multiplexing is required, then an additional signal is needed to ensure that the user-specific I/O signals on the circuit board do not contend with the JTAG-ISP signals during programming. It is recommended to use an external signal to control the multiplexing. For example, if a product using a programmed PSD needs a field update but the PSD port pins are no longer supporting JTAG-ISP because they are in I/O mode instead. There needs to be a way to reclaim the pins on the PSD port to support JTAG-ISP once again. To solve this problem, one can design the PSD (in PSDsoft) to sense when a JTAG-ISP programmer cable is connected to the product, then force the multiplexed pins to serve JTAG-ISP functions.

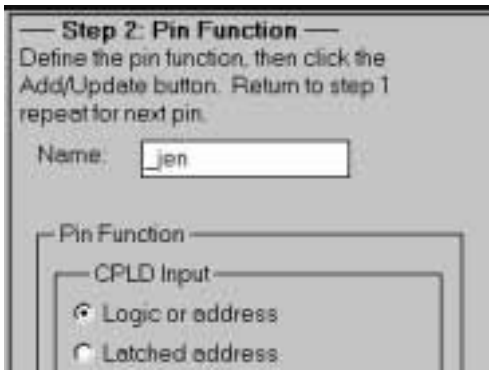
It is possible to reclaim the pins for JTAG-ISP by other means (other than an external signal), such as using a signal generated on-board the end-product (instead of FlashLINK), or the microcontroller can write to PSD JTAG control register at run-time to enable the JTAG pins, but the following method is recommended.

Example of multiplexing JTAG signals using FlashLINK:

For this example, we'll use an external signal as an input to the PSD's PLD to enable the JTAG pins (see Figure 3). This external signal, called JTAG Enable (JEN\), can enter the PSD on any pin that is an input to the PLD, and is not one of the four basic JTAG-ISP signals. JEN\ must be defined in PSDsoft and then used in an equation, which enables four pins on the PSD port to function as JTAG-ISP signals (TCK, TMS, TDI, TDO) when JEN\ is active.

In PSDsoft 2000 (PSDsoft Express does not support multiplexing of JTAG-ISP pins), click on any of the JTAG-ISP pins (TCK, TMS, TDI, TDO) and click delete. This will remove all four of the JTAG-ISP signals from the pin definition screen. Now these four pins are not dedicated to JTAG-ISP full time and are available for other I/O signal functions. You may define their function as any I/O function you wish.

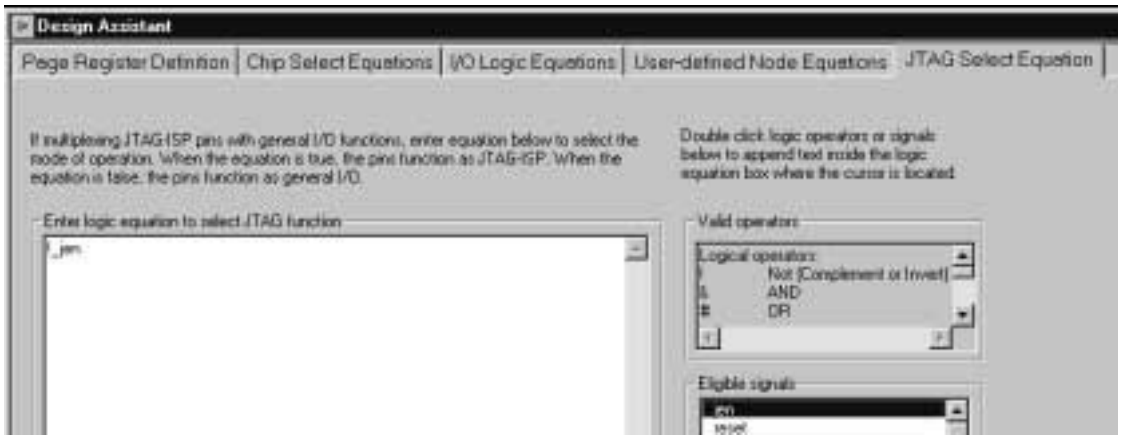
Next, choose any pin in the Pin Definition screen that can be a PLD input (but not one of the basic four JTAG-ISP pins), name it _jen, and define its function as logic input as shown below:



Finally, in the PSDsoft 2000 Design Assistant, select the JTAG Select Equation tab and enter! _jen for the equation. Click the Show Eq button at the bottom and you should see the resultant equation:

jtagsel = !_jen;

Here is what the screen should look like:



That is all that is needed in PSDsoft 2000 to configure for multiplexing JTAG signals.

JEN\ is an open-collector signal driven low (active) by the FlashLINK cable a few milliseconds prior to any JTAG communications taking place and will remain low until no more JTAG communications are required. A few milliseconds after JTAG communications stop, JEN\ will return high (inactive). When JEN\ is high, the four pins become general I/O signals again. This allows the FlashLINK cable to remain physically connected to the product during development because the FlashLINK cable will not drive any JTAG-ISP signal when JEN\ is high (FlashLINK goes to high impedance). JEN\ is pulled up to Vcc in the FlashLINK cable through a 100K resistor.

In this example using FlashLINK, all six JTAG-ISP pins are used, and the JEN\ signal is connected to the FlashLINK cable. Figure 3 illustrates the connection scheme:

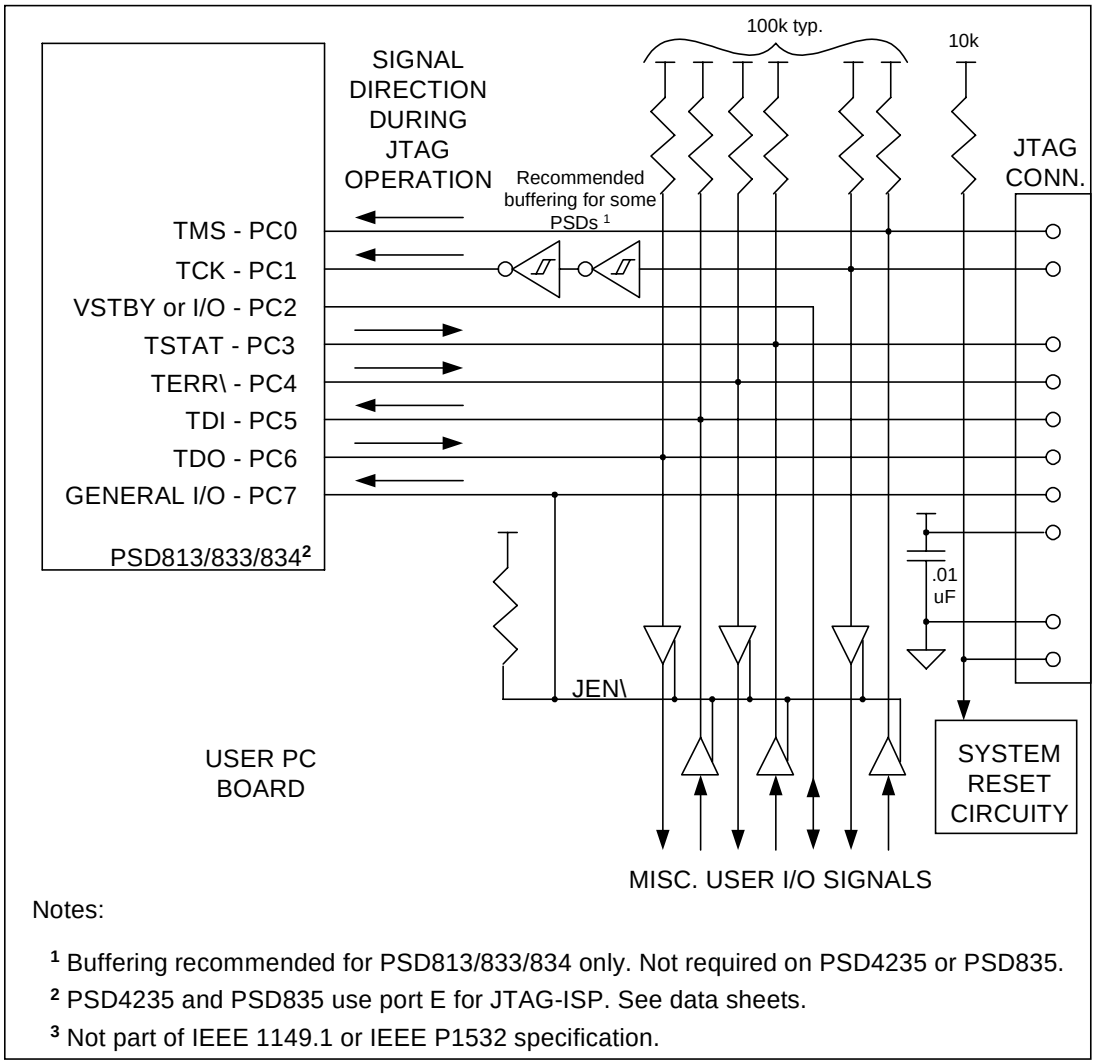


Figure 3 - Multiplexing JTAG-ISP signals

Additional notes:

- It is the user's responsibility to ensure that no user-specific logic is driving the JTAG signals during JTAG operation or no user-specific logic is being driven by JTAG signals in a destructive way.

- The signal JEN\ does not have to enter the PSD on pin PC7. JEN\ can enter on any I/O pin that feeds the PLD.

- It is highly recommended to connect RST\ from FlashLINK into your system reset. All memory inside of the PSD is inaccessible to the microcontroller during JTAG-ISP operations. As such, the microcontroller will fetch garbage and behave unpredictably. PSDsoft automatically drives the RST\ signal active during all JTAG operations, which will hold the microcontroller in a safe state of reset when needed. As a convenience, PSDsoft will also drive RST\ active when the reset “button” is clicked with a mouse. The RST\ signal is driven from FlashLINK active low and open-collector, with a 10K pullup to Vcc.

- Vcc (2.7V to 5.5V) from the target system must be routed to the JTAG-ISP connector to supply to the FlashLINK cable assembly (15 mA max at 5.5 V). It is recommended to position a decoupling capacitor (0.01uF) between Vcc and GND at the JTAG-ISP connector.

- A 10k pullup on JEN\ is needed to ensure that the misc. user signals are not disabled while the FlashLINK cable is disconnected.

- Schmitt-trigger buffering on the TCK input is recommended for PSD813/833/834 devices to reduce the chance of false TCK transitions from spikes or slow ramp rates. The PSD4235 and PSD835 need no external buffering because their TCK input is Schmitt buffered in silicon.

- It is recommended to place pullups (values 10K to 100k) on all the JTAG-ISP signals lines as shown.

- For PSD813/833/834 devices, be sure not to set bit 6 of the PMMR2 register at run-time if you use port C pin PC7 for the signal JEN\. Setting this bit will block it from entering the PLD to save power and JEN\ will not activate the JTAG-ISP pins. The default state of this bit is zero and it should be left that way in this case. PMMR2 is one of the PSD control registers in the "csiop" block.

- For PSD813/833/834/835/4235 devices do not set bit 7 of the JTAG control register at run-time. If you do, this will turn on the JTAG-ISP pins for JTAG at all times regardless of what the JEN\ signal is doing. See data sheet for details. The JTAG control register is one of the PSD control registers in the "csiop" block.

To program the flash PSD in this multiplexed example, this sequence occurs:

1. The device programmer (FlashLINK) activates the JEN\ signal by driving it low to enable the JTAG-ISP functions on the PSD pins. FlashLINK also drives the RST\ signal active to hold the microcontroller in a state of reset.
2. Because JEN\ is also connected to the enable lines on the tri-state buffers, the JEN\ signal disables the user-specific signals that are driving multiplexed JTAG-ISP pins.
3. The four JTAG-ISP signals (TCK,TDI,TDO,TMS) are now active.
4. The FlashLINK sends an initialization command over the JTAG-ISP channel to the PSD that activates the TSTAT and TERR\ signals. After that, all six JTAG-ISP pins are enabled and active.
5. JTAG-ISP traffic occurs.
6. After the ISP session, all six JTAG-ISP pins will go back to non-JTAG functions as soon as the external JEN\ signal goes to the inactive state (logic HI). RST\ is released.
7. The signals JEN\ and RST\ lead and lag JTAG-ISP traffic by a few milliseconds.

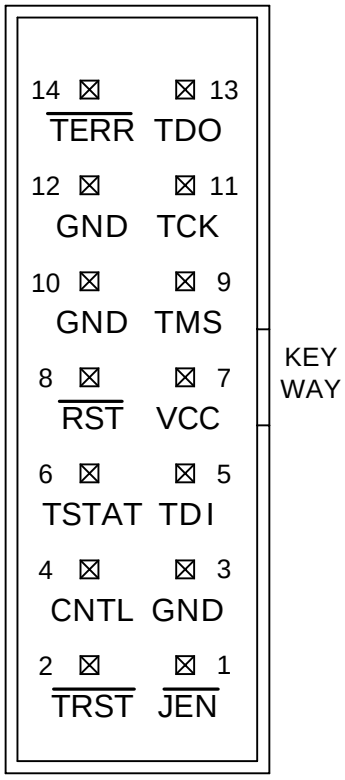
If the flash PSD device were blank, then the JTAG-ISP pins would be enabled and active immediately from power-on. However, JEN\ would still be needed to tri-state off the user specific signals.

8 JTAG-ISP Connector Definition

There is still no industry "standard" JTAG connector. Each manufacturer differs. Waferscale has a specific connector and pinout for the FlashLINK programmer adapter. The connector scheme on the FlashLINK adapter can accept a standard 14 pin ribbon connector (2 rows of 7 pins on 0.1" centers, standard keying) or any other user specific connector that can slide onto 0.025" square posts. The pinout for the FlashLINK adapter connector is shown in Figure 4.

A standard ribbon cable is good way to quickly connect to the target circuit board. If a ribbon cable is used, then the receiving connector on the target system should be the same connector type with the same pinout as the FlashLINK adapter shown in Figure 4. Keep in mind that the JTAG signal TDI is sourced from the FlashLINK adapter and should be routed on the target circuit card so that it connects to the TDI input pin of the PSD device. Although the name "TDI" infers "Data In" by convention, it is an output from FlashLINK and an input to the PSD device. Also keep in mind that the JTAG signal TDO is an input received by the FlashLINK adapter and is sourced by the PSD device on the TDO output pin. Use Figures 1, 2, 3, and 6 as a guide.

WAFERSCALE JTAG-ISP CONNECTOR DEFINITION



VIEW: LOOKING INTO FACE OF SHROUDED MALE CONNECTOR. 0.025" POSTS ON 0.1" CENTERS.

Connector reference: Molex 70247-1401

Recommended ribbon cable for quick connection of FlashLink adapter to end product:
Samtec: HCSD-07-D-06.00-01-S-N
or
Digikey: M3CCK-14065-ND

Note:
TDI is a signal source on the Flashlink and a signal destination on the target board.

TDO is a signal destination on the FlashLink and a signal source on the target board.

Figure 4 - Pinout for FlashLINK Adapter and Target System

Each FlashLINK is sold with a six-inch "flying lead" cable for maximum adaptability (a ribbon cable requires the use a certain connector on the target assembly). This flying lead cable, shown in Figure 5, mates to the FlashLINK adapter on one end and has loose sockets on the other end to slide onto 0.025 square posts on the target assembly.

If you do not use the flying lead cable provided with the FlashLINK, be sure to keep length to a minimum (9” or less) for a ribbon cable or any other cable that you may manufacture. Also, it is best to connect the FlashLINK cable directly to the PC parallel port connector without a printer cable extension. The FlashLINK is not guaranteed to function properly if the total length of the parallel port cable (from the PC to the FlashLINK adapter) exceeds six feet.

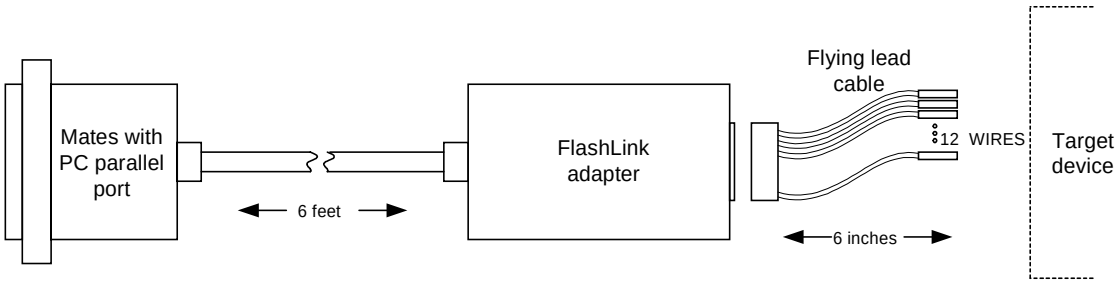


Figure 5 - FlashLINK cable assembly

The signals are defined Table 1.

PIN #	SIGNAL NAME	DESCRIPTION	Type	Flashlink is Signal
1	JEN\	Enables JTAG-ISP pins on PSD. Only used when JTAG-ISP signals are multiplexed with other I/O.(optional)	OC,100K	Source
2	TRST\ *	JTAG reset on target (optional per 1149.1)	OC,10K	Source
3	**GND**	Signal ground		
4	CNTL *	Generic control signal, (optional)	OC,10K	Source
5	**TDI**	JTAG IEEE 1149.1 serial data input		Source
6	TSTAT	JTAG-ISP programming status (optional)		Destination
7	**Vcc**	VDC Source from target (2.7 - 5.5 VDC)		
8	RST\	Target system reset (recommended)	OC,10K	Source
9	**TMS**	JTAG IEEE 1149.1 mode select		Source
10	GND	Signal ground		
11	**TCK**	JTAG IEEE 1149.1 clock		Source
12	GND	Signal ground		
13	**TDO**	JTAG IEEE 1149.1 serial data output		Destination
14	TERR\	JTAG-ISP programming error (optional)		Destination

Notes

1. **Bold** signals are required connections
2. All signal grounds are connected inside FlashLink adapter
3. OC = open collector, pulled-up to Vcc inside FlashLink adapter
4. * = Not supported by PSDsoft, signals remain inactive.
5. The target device must supply Vcc to the FlashLink Adapter (2.7 to 5.5 VDC, 15mA max @ 5.5V).

Table 1 - Pin descriptions for FlashLINK adapter assembly

All 14 signals may not be needed for a given application. Here's how they break down:

(6) Required signals (four JTAG-ISP pin config): **TDI, TDO, TMS, TCK, Vcc, GND**

(2) Optional signals for faster ISP (6 JTAG-ISP pin config): **TSTAT, TERR**

(1) Optional signal to control multiplexing of the JTAG signals: **JEN**

(1) Recommended signal to allow FlashLINK to reset target system during and after ISP: **RST**

(1) Optional IEEE-1149.1 signal for JTAG chain reset: **TRST**

(1) Optional generic control signal from FlashLINK to target system: **CNTL**

(2) Two additional ground lines to help reduce EMI if a ribbon cable is used. These ground lines "sandwich" the TCK signal in the ribbon cable. These lines are not needed for use with the flying lead cable. That is why the flying lead cable has only 12 of 14 wires populated.

9 JTAG Chaining

Multiple Flash PSD devices may be placed in a JTAG chain configuration. An example of this configuration is shown in Figure 6. Notice that Flash PSDs can reside in a JTAG chain with non-PSD devices. The non-PSD devices cannot be programmed using PSDsoft. These devices will be placed by PSDsoft in BYPASS mode while JTAG operations are occurring on PSD devices. Conversely, when non-PSD devices are being accessed by a JTAG controller other than FlashLINK, the PSDs operate in BYPASS mode.

PSDsoft will perform operations on only one Flash PSD device at a time. This means that while one Flash PSD device is being programmed or erased, the other Flash PSDs are in BYPASS.

As shown in Figure 6, the signals TSTAT and TERR\ are or-tied together (and are configured as open-drain outputs in PSDsoft). The Flash PSD devices that are in BYPASS mode will not assert TSTAT and TERR\, only the Flash PSD that is performing JTAG operations will assert these signals.

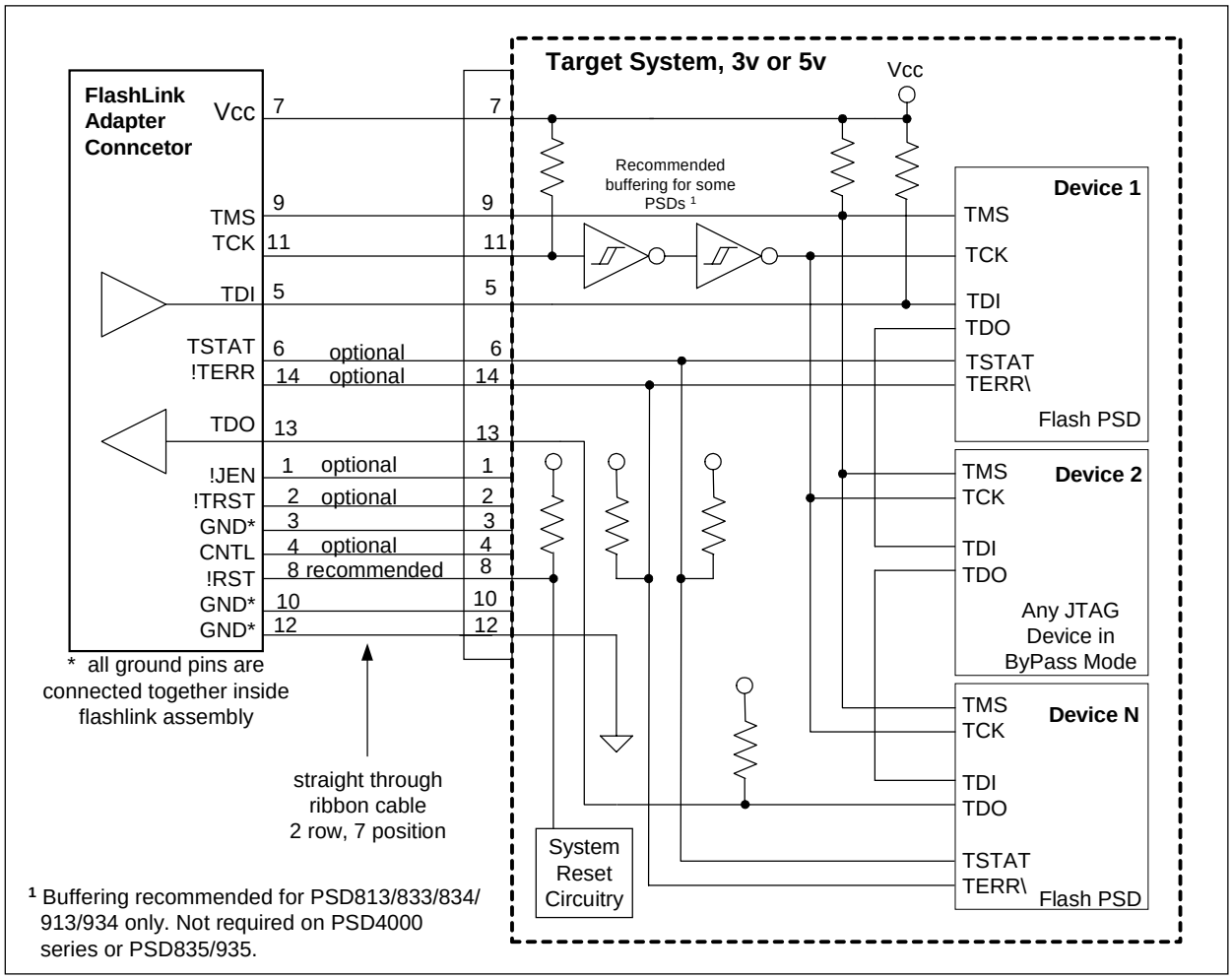


Figure 6 - JTAG Chaining Example

10 General Notes

- All sections of the PSD813F1 and PSD913F1 are programmable via the JTAG-ISP interface except the 64 byte "OTP row" of EEPROM.
- The Software Data Protect (SDP) mode of the PSD813F1 and PSD913F1 cannot be enabled via the JTAG-ISP interface. An insertion type programmer may enable SDP mode, or the microcontroller may enable SDP mode at run-time.