SIEMENS

ISDN Echo-Cancellation Circuit (IEC-T)

PEB 20901
PEB 20902

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PEB 20901-C	Q67100-H8679	C-DIP-40
PEB 20901-N	Q67100-H6113	PL-CC-44 (SMD)
PEB 20901-P	Q67100-H8678	P-DIP-40
PEB 20902-C	Q67100-H8680	C-DIP-24
PEB 20902-N	Q67100-H6114	PL-CC-28 (SMD)
PEB 20902-P	Q67100-H8681	P-DIP-24

The PEB 2090 ISDN Echo-Cancellation Circuit (IEC-T) is an advanced CMOS circuit for transmission over public telephone lines. The transmission technique used is according to the U_{k0} interface specification of the Deutsche Bundespost. The adaptive filter concept of the IEC-T is based on a highly digital approach which utilizes sophisticated digital signal processing capability.

The PEB 2090 enables digital full duplex voice/data transmission via the standard twisted pair telephone cable (U interface) with a user bit rate of 144 kbit/s according to the ISDN standards. Together with the flexible IOM® interface, it is fully compatible to operate with the PEB 2070 (ICC) and PEB 2080 (SBC) devices and also enables a repeater (two IEC's back to back) for longer telephone loops.

The IEC-T is capable of operating in the following applications by means of pin strapping: the exchange, the network termination, the terminal equipment, and the trunk module connecting a PBX to the public network.

At present, the complete U interface functions are available in a two-chip set.

Features

- Full duplex transmission and reception of the U_{k0} interface signals according to the FTZ Guideline 1 TR 220 of the Deutsche Bundespost (DBP).
- Adaptive echo cancellation.
- Adaptive equalization.
- Automatic polarity adaptation.
- Clock recovery (frame and bit synchronization) in all applications.
- Transposition of ternary to binary data (4B 3T) and vice versa (coding, decoding, scrambling, descrampling, phase adaptation).
- Built in wake-up unit for activation from power-down state.
- Activation and deactivation procedure according to CCITT I.430 and to FTZ Guideline 1 TR 210 of the DBP.
- Optimized for working in conjunction with SBC and ICC telecom IC's via IOM interface.
- Handling of commands and indications contained in the IOM C/I channel for (de-)activation, supervision of power supply unit and equipment for wire testing.
- Data availability via the MONITOR channel.
- Switching of test loops.
- Generation of a synchronized 7.68-MHz clock for the SBC in the NT mode.

The IEC-T in a Two-Chip Set

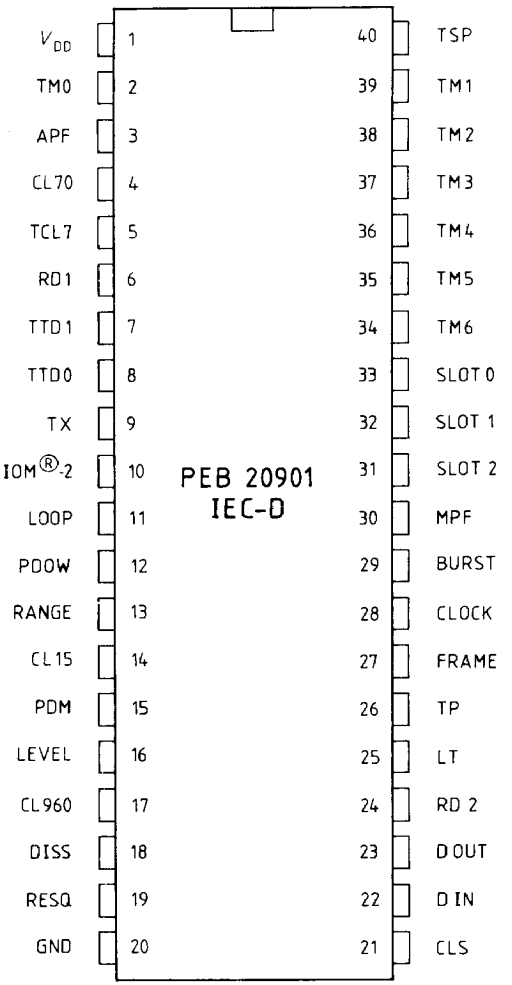
A 'Digital' Circuit, called IEC-D (PEB 20901) contains the digital receiver functions and the IOM-U_{k0} interface functions.

An 'Analog' Circuit, called IEC-A (PEB 20902) contains the crystal oscillator and all of the analog functions of the line port, namely the A/D converter in the receive path and pulse shaping D/A converter and line driver in the transmit path.

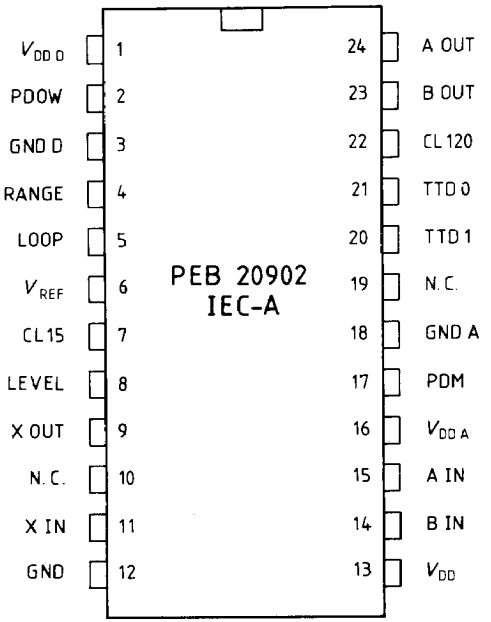
Pin Configurations

(top view)

PEB 2091 IEC Digital Part



PEB 20902 IEC Analog Part



Pin Definitions and Functions of PEB 20901

Pin. No.	Symbol	Input (I) Output (O)	Function
19	RESQ	I	**Power On Reset** (active low) must be low at least 300 µs. The clock on CLOCK pin has to be applied during reset in the LT modes and in NT-PBX mode. If not used, the RESQ pin must be clamped to high.
40	TSP	I	**Test Single Pulses.** IEC transmits single pulses of equal polarity spaced 1 ms (active high). If not used, the TSP pin must be clamped to low.
10	IOM-2	I	**Enable IOM-2 Mode.** If pin is high, the IEC is in the IOM-2 mode, otherwise it is in original IOM-1 mode.
18	DISS	O	**Disable Supply** (active high).
30	MPF	I	**Monitor Power Feed.** Serial data of power feed current (active high).
3	APF	I	**Alarm Power Feed.** Power feed overload with short response time. If not used, the APF pin must be clamped to low (active high).
6, 24	RD1, RD2	O	Two pins to control independently two relay drivers. They are set via IOM MONITOR channel.
20	GND	I	Ground-pin for digital functions of IEC.
1	V_{DD}	I	V_{DD} pin for digital functions of IEC.
26	TP	I	**Testpin.** Only for internal test purposes. Must be clamped to low during normal operations.
2,39,38, 37,36,35, 34	TM0...TM6	I	**Testpins.** Only for internal test purposes. Must be clamped to high during normal operations.
5	TCL7	I	**Testpin.** Only for internal test. Must be clamped to low during normal operation.
4	CL7O	O	**Testpin.** Only for internal test.
25	LT	I	Programs the IEC-D to LT mode (LT pin high) or NT mode (LT pin low).
29	BURST	I	Programs the IEC-D to 256-kbit/s-LT, LT-RP, NT, NT-PBX, NT-RP, or NT-TE mode (BURST pin low) or to 2048-kbit/s-LT-BURST, NT-PBX-BURST mode (BURST pin high).

Pin Definitions and Functions of PEB 20901 (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
33, 32, 31	SLOT0, SLOT1, SLOT2	I	These pins program the IEC-D to the different 256-kbit/s modes if BURST pin is low or assign the time slot in the BURST modes.
22	DIN	I	IOM data input synchronous to CLOCK.
23	DOUT	O	IOM data output synchronous to CLOCK.
28	CLOCK	I/O	Double IOM data clock.
27	FRAME	I	IOM frame signal.
21	CLS	I/O	In all LT modes: Power feed off signal from power controller. Must be clamped to low, if not used. In NT modes: 7.68-MHz clock output synchronized to the line signal. In NT-PBX modes: 512-kHz clock output synchronized to the line signal. In TE (IOM-2) mode: 768-kHz clock synchronized to the line signal. In TE (IOM-1) mode: 1.536-MHz clock synchronized to the line signal.
12	PDOW	O	Activates power-down mode of the IEC-A.
13	RANGE	O	Activates 6 dB attenuation for the ADC input signal.
11	LOOP	O	Activates the analog test loop.
17	CL 960	O	960-kHz clock. The TX signal is derived from this clock by dividing it by 8.
9	TX	O	120-kHz clock. The transmitted data are synchronized to this clock. In the one-chip solution, this clock is given out on pin TM0 during normal operation.
7	TTD1	O	Ternary data to be transmitted.
8	TTD0	O	Ternary data to be transmitted. TTD0 and TTD1 are binary coded. The combination TTD0 = 1 and TTTD1 = 0 is not used. They change with the rising edge ± 10 ns of CL120.
14	CL15	I	15.36-MHz clock.
16	LEVEL	I	Gives the polarity of the differential input signal and is used to awake signal detection.
15	PDM	I	15.36 Mbit/s output signal of the ADC in phase with C15.

Pin Definitions and Functions of PEB 20902

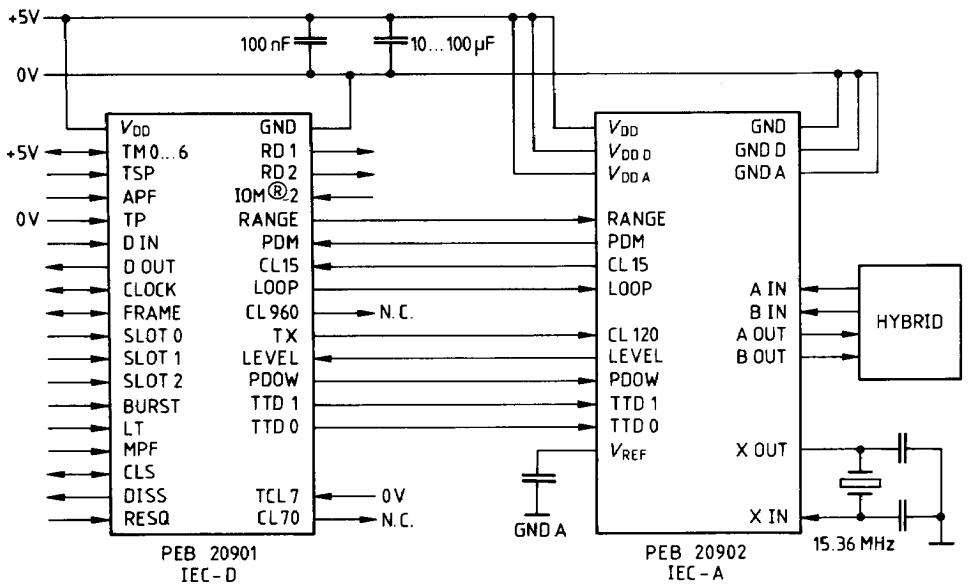
Pin No.	Symbol	Input (I) Output (O)	Function
2	PDOW	I	Activates power-down mode, only oscillator and level detect are operating during power-down.
4	RANGE	I	Activates 6 dB attenuation for the ADC input signal.
5	LOOP	I	Activates the analog test loop.
22	CL120	I	120 kHz clock input. Transmitter is synchronized to this clock.
20	TTD1	I	Digital input signal to the DAC.
21	TTD0	I	Digital input signal to the DAC. TTD0 and TTD1 are interchangeable. They must change with the rising edge (± 10 ns) of CL120.
7	CL15	O	15-MHz clock. Capacitive load should be minimized.
8	LEVEL	O	Detects the zero crossing of the differential input signal and is used to activate the IEC-D.
17	PDM	O	15 MHz, 1-bit output signal of the ADC in phase with CL15. Changes with rising edge of CL15 +2..4 ns. Capacitive load should be minimized.
15, 14	AIN, BIN	I	Received line-signal from hybrid.
24, 23	AOUT, BOUT	O	Transmitted line-signal to hybrid.
3	DGND	I	Ground-pin for digital functions of IEC-A.
1	$V_{DD\ D}$	I	V_{DD}-pin for digital functions of IEC-A.
18	AGND	I	Ground-pin for digital functions of IEC-A.
16	$V_{DD\ A}$	I	V_{DD}-pin for digital functions of IEC-A.
12	GND	I	Ground-pin for digital functions of IEC-A.
13	V_{DD}	I	V_{DD}-pin for digital functions of IEC-A.
6	V_{REF}	O	V_{REF}-pin to buffer internally generated voltage with capacitor 10 nF versus AGND.
11	XIN	I	In all NT modes, crystal connection. In all LT modes, 15.36-MHz clock input synchronized to IOM clocks.
9	XOUT	O	In all NT modes, crystal connection. In all LT modes, to be left open.

All digital outputs use positive logic and CMOS levels. Drive capability is 10 pF for CL15 and PDM and 25 pF for LEVEL. All input signals are active high and use CMOS logical levels. XIN and XOUT supply a load of 2-3 pF vs. ground to the crystal.

The maximum power consumption without load at CL15 is 15 mW in power-down mode, 100 mW with open outputs AOUT/BOUT and 150 mW during normal transmission.

The sensitivity of the ADC can be reduced, if necessary, by putting a resistor between AIN and BIN (10..20 kΩ).

Application Diagram of IEC-D and IEC-A (Two-Chip Solution)



Operation Modes and Functions

IOM Concept and Applications of the IEC-T

The IEC-T is designed to be used in: the Line Terminator (LT) part of the Digital Subscriber Module (DSM), the Network Termination (NT), the Digital Trunk Basic Access (PBX) and in the Terminal Equipment (TE).

Figure 1
Connecting S-Bus to Public Network

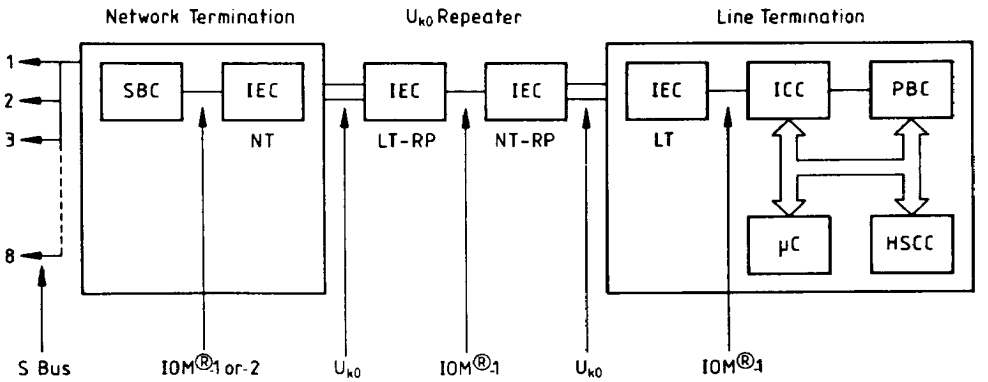


Figure 2
Connecting Private to Public Network

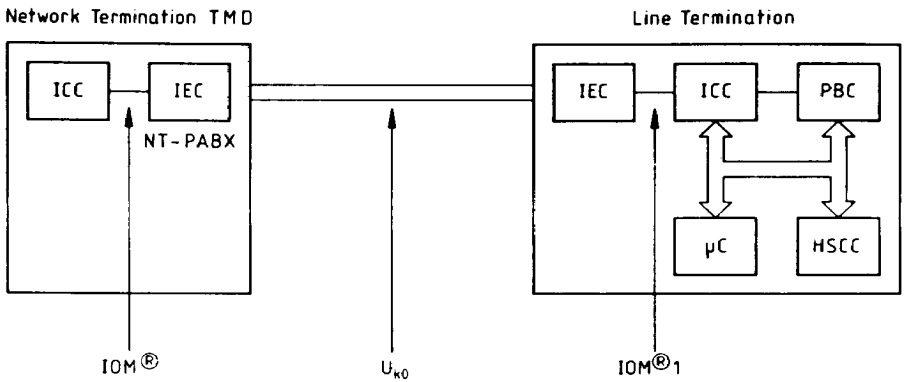


Figure 3
Connecting Terminal Equipment within Private Network (1st Generation)

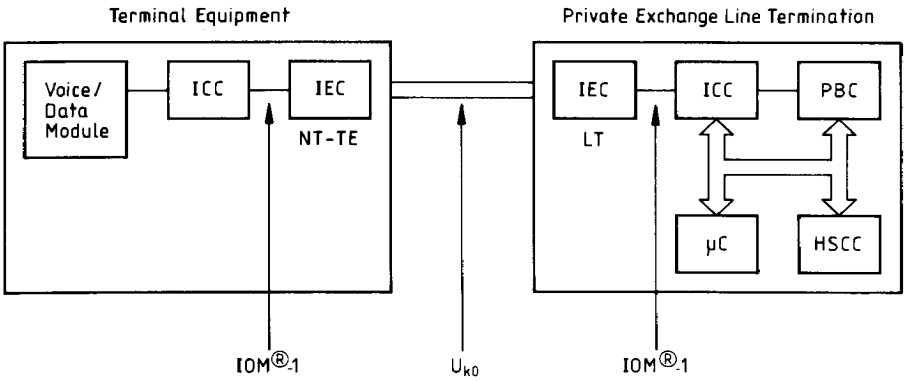
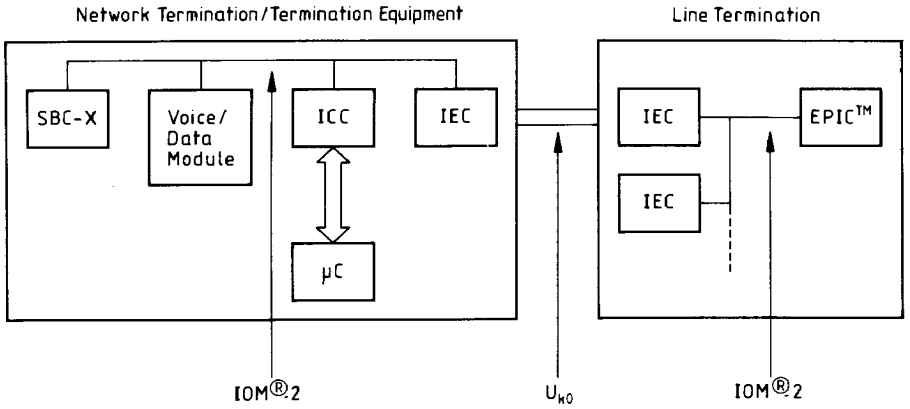


Figure 4
Connecting Network Termination or Terminal Equipment to Exchange (2nd Generation)

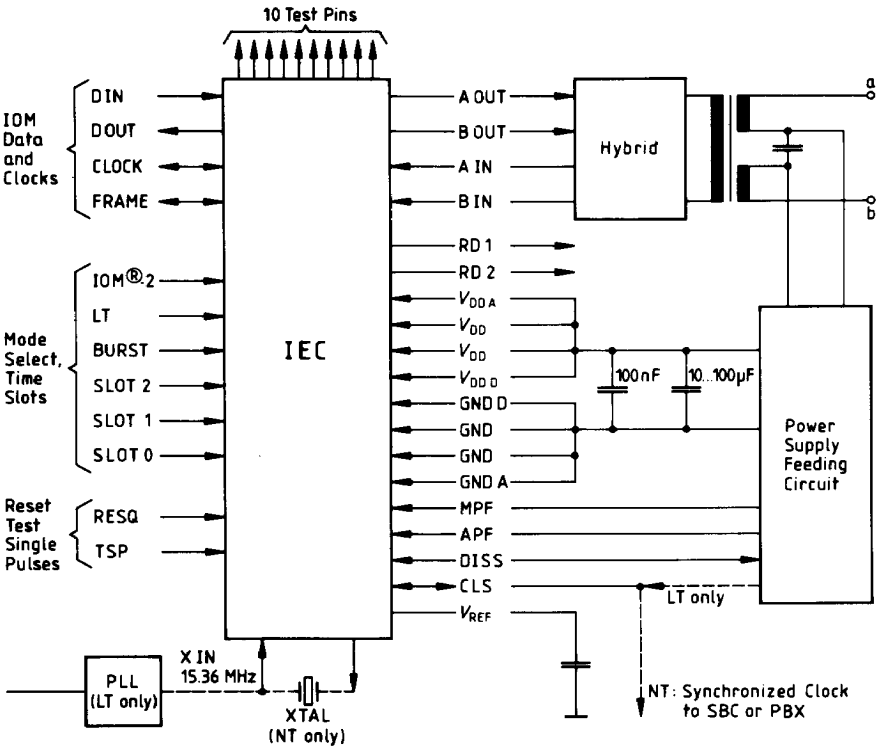


To cater to these various applications, the IEC-T can be programmed via pin strapping to different modes **(see following table)**.

Table 1
Programming the IEC-T Operation Modes

Signal on Input Pin					MODE
LT	BURST	SLOT2	SLOT1	SLOT0	
0	0	0	0	0	LT
1	0	0	0	1	LT-RP: Repeater downstream
1	1	*	*	*	LT-BURST: LT MUX mode
0	0	0	0	0	NT
0	0	0	0	1	NT-RP: Repeater upstream
0	0	1	0	0	NT-PBX: PBX continuous mode
0	0	1	0	1	NT-TE: Terminal Equipment
0	1	*	*	*	NT-PBX BURST: PBX MUX mode

Figure 5
Interfaces of the IEC-T



* In these modes SLOT2, SLOT1, SLOT0 are used for selecting the time slot rather than the mode.

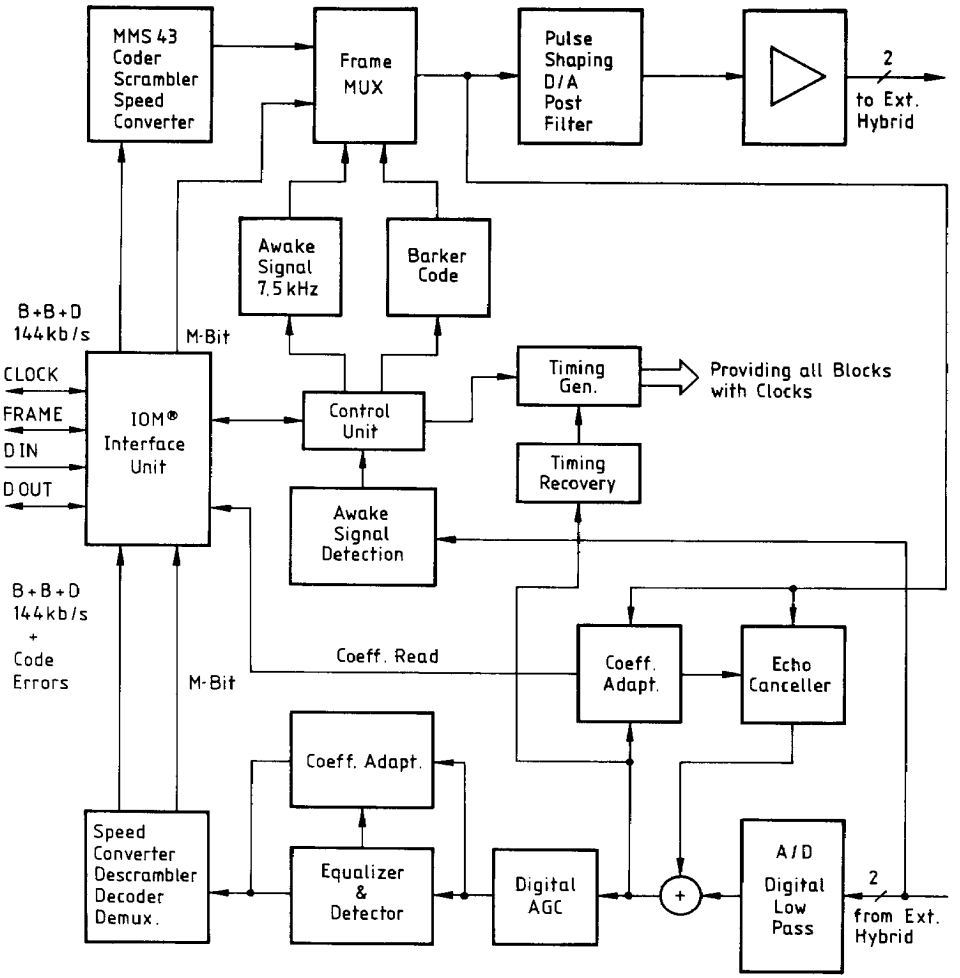
Mode Dependent Functions

Table 2
Mode Dependent Functions

Pin	LT	LT-BURST1	LT-BURST2	LT-RP	NT-RP	NT	NT-PBX	NT-PBX-BURST1	NT-PBX-BURST2	NT-TE1	NT-TE2
LT	1	1	1	1	0	0	0	0	0	0	0
BURST	0	1	1	0	0	0	0	1	1	0	0
IOM-2	0 or 1	0	1	0	0	0 or 1	0 or 1	0	1	0	1
SLOT 0	0	Time-	Time-	1	1	0	0	Time-	Time-	1	1
SLOT 1	0	Slot	Slot	0	0	0	0	Slot	Slot	0	0
SLOT 2	0	select	select	0	0	0	1	select	select	1	1
DIN	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	256 kbit/s	256 kbit/s	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	768 kbit/s
DOUT	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	256 kbit/s	256 kbit/s	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	768 kbit/s
CLOCK	512 kHz IN	4096 kHz IN	512..5000 kHz IN	512 kHz IN	512 kHz OUT	512 kHz OUT	512 kHz IN	4096 kHz IN	512..5000 kHz IN	512 kHz OUT	1536 kHz OUT
FRAME	8 kHz IN	8 kHz IN	8 kHz IN	8 kHz IN	8 kHz 1:1 OUT	8 kHz 1:1 OUT	8 kHz IN	8 kHz IN	8 kHz IN	8 kHz 1:1 OUT	8 kHz 1:1 OUT
CLS	PFOFF IN	PFOFF IN	PFOFF IN	PFOFF IN	7.68 MHz OUT	7.68 MHz OUT	512 kHz OUT	512 kHz OUT	512 kHz OUT	1536 MHz OUT	768 kHz OUT
XIN	15.36 MHz	15.36 MHz	15.36 MHz	15.36 MHz	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL
XOUT	NC	NC	NC	NC	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL

Survey of IEC Functional Blocks

Figure 6
Functional Block Diagram of IEC-T



Description of the Digital Module Interface

The IEC-T is provided with an IOM interface which operates in both a continuous and a burst mode in order to interface units which realize OSI layer-1 functions like the SBC (PEB 2080) and to layer-2 functions like the ICC (PEB 2070).

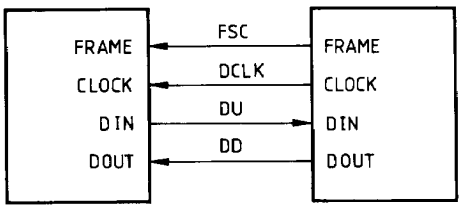
The IEC-T is designed for the original IOM interface (IOM-1), but with the IOM-2 pin it is possible to give the IEC-T some physical features of the IOM-2 interface. Logically, the IEC-T behaves like in IOM-1 mode.

There are three differences between IOM-1 and IOM-2 operation modes:

- In the BURST modes, IOM-2 frame synchronization is the same as in the 256-kbit/s modes. Additionally, the IEC-T enables clock frequencies on DCLK ranging from 512 to 5000 kHz in increments of 8 kHz.
- Each E-bit (MX-bit) is reflected in the T-bit (MR-bit) in the next IOM-2 frame. For IOM-2 interfaces, the E-bit is always used to access the MONITOR channel, which is acknowledged in the T-bit.
- The transparent channel on U_{k0} can't be used, because the T-bit is used for MONITOR channel access.

All other features of IOM-2, like other C/I and MONITOR channel codes, are not implemented in the IEC-T.

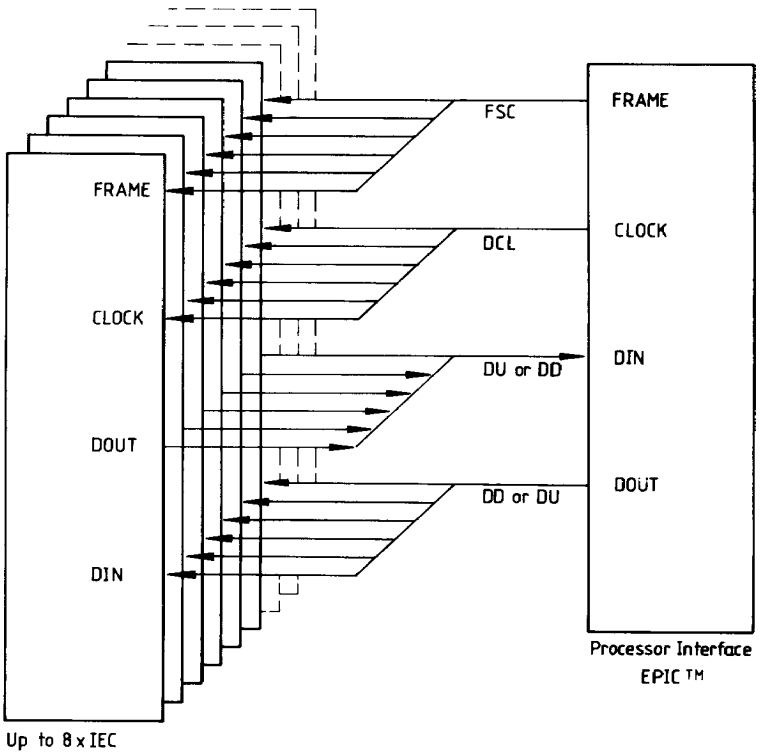
Figure 7
IOM Interface in Different Applications of the IEC-T



In the Exchange :	IEC	ICC
In the Repeater :	IEC	IEC
In the NT :	SBC	IEC
In the TMD :	IEC	ICC
In the TE :	ICC	IEC

Figure 8

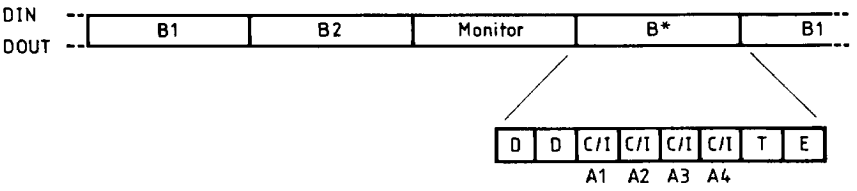
IOM Interface MUX Mode



For each application, the ISDN data rate of 144 kbit/s (2 B + D) is transmitted transparently via the modular interface. It is necessary to exchange control information for means of activation and deactivation of OSI layer-1 functions and switching of testloops. In some applications, access to maintenance information is additionally provided.

This information is transferred in a time multiplex procedure based on an 8-kHz frame-structure **(see following figure)**.

Figure 9
Frame Structure of the Digital Interface of IEC-T



Four octets are transmitted in each frame:

1st octet B1: B channel (64-kbit/s data) MSB first.

2nd octet B2: B channel (64-kbit/s data) MSB first.

3rd octet: MONITOR (8-bit monitor address for DIN, 8-bit monitor data with MSB first for DOUT.

4th octet B*: 2 bit D channel 16-kbit/s data

4 bit C/I channel.

T channel for 1-kbit/s transparent data with IOM-1 or for the handling of the monitor channel with IOM-2 (MX-bit).

E extension bit for control of monitor channel and to hand over the maintenance bit of U_{k0}.

In the multiplexed modes, the IOM data of up to eight IEC-Ts are multiplexed. The data streams consist of bursts of 4 octets per frame. The bursts are allocated to consecutive time slots in a frame by the static inputs SLOT0, SLOT1, SLOT2. Outside of the allocated time slot, the IEC-T must not read from DIN-pin and the DOUT-pin remains high impedance. The next table indicates the allocations.

Table 3
Allocation of Time Slots in IOM-1 and IOM-2 Modes

Time Slot No.	SLOT0	SLOT1	SLOT2	Bit No.
0	0	0	0	0...31
1	0	0	1	32...63
2	0	1	0	64...95
3	0	1	1	96...127
4	1	0	0	128...159
5	1	0	1	160...191
6	1	1	0	192...223
7	1	1	1	224...255

Clock Generation

The master clock is the clock signal with the highest frequency in the system.

NT Modes

The master clock is derived from a built-in crystal oscillator in the NT operating modes. The crystal is connected to the pins XIN and XOUT. The maximum capacitive load at XIN and XOUT is 60 pF each.

Nominal frequency:	15.36 MHz
Overall tolerance:	± 100 ppm

We recommend using a crystal (serial resonance) which meets the following specification:

Nominal frequency:	15.36 MHz
Overall tolerance:	± 60 ppm
Load capacitance:	20 pF
Resonance resistance:	20 Ω
Shunt capacitance:	7 pF

LT Modes

In the LT modes, the timing signal is derived from the clock via an external phase locked loop. The master clock is fed to pin XIN.

Nominal frequency:	15.36 MHz
Duty ratio:	0.4...0.6
Rise and fall times:	< 10 ns
Max. Difference of phase deviations of master clock/1920 and FSC:	± 18 µs
Max. low freq. phase wander within 1 period:	± 0.85 ps
Jitter (peak-to-peak):	see following figure

In the deactivated state, while no data has to be recognized on the line, no particular jitter requirements have to be kept.

Figure 10
Maximum Sinusoidal Input Jitter of Master Clock 15.36 MHz

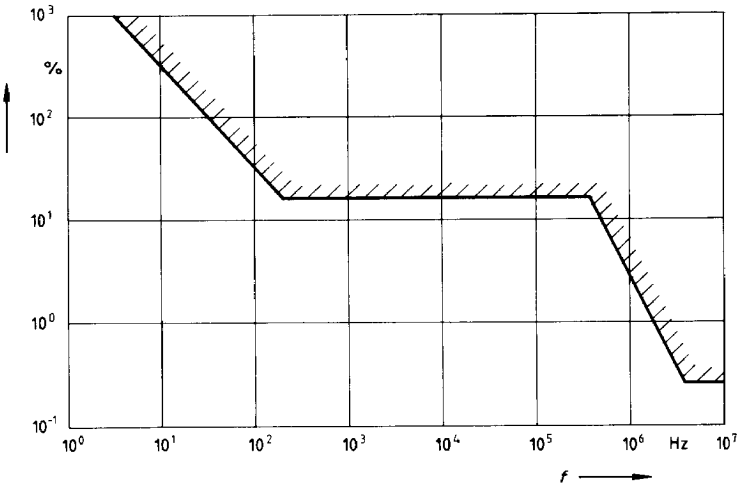
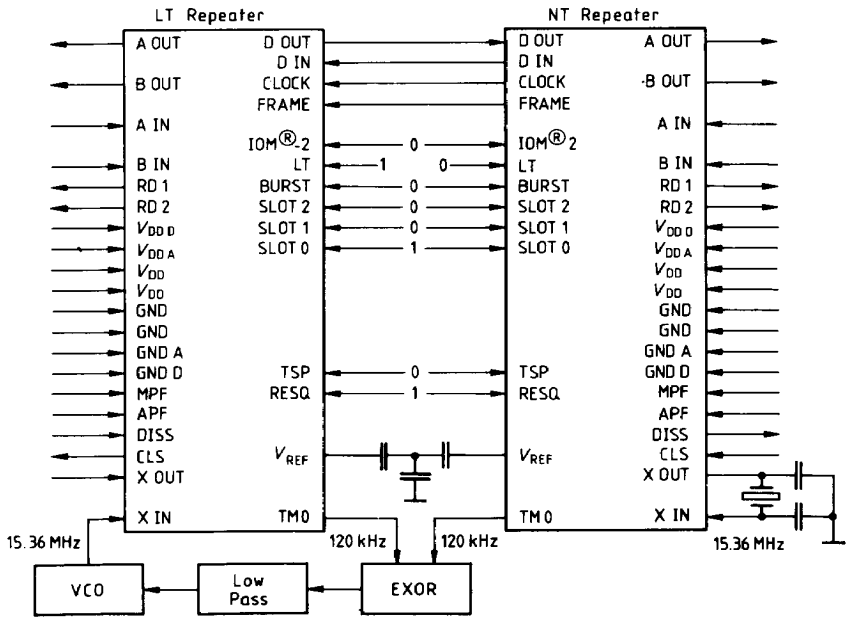


Figure 11
Interfaces of the IEC-T in NT-RP Mode



Description of the Line Port

The U_{k0} interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

Separation of the transmitted and received signals is done by means of echo cancellation.

The following functions are transmitted over the twisted pair:

- Bidirectional
  - B1, B2, D, T data channels
  - 120-kHz symbol clock
  - 1-kHz frame and 40-kHz block clock
  - Activation
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops
- From NT to LT side:
  - Indication of monitored code violations

On the U_{k0} interface, transmission ranges of 4.2 km on wires of 0.4 mm diameter and 8 km on 0.6 mm wires are achieved without additional signal regeneration on the loop.

The transmission ranges can be doubled by inserting one repeater for signal regeneration.

Frame Structure of the U_{k0} Interface

1 ms frames are transmitted via the U_{k0} interface, each consisting of:

- 108 symbols: 144-bit scrambled and coded B+B+D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, 36 bits) contains the user data of two IOM frames in the same order (8B + 8B + 2D) + (8B + 8B + 2D).

Different synchwords are used for each direction:

- Downstream from LT to NT +++−−−+−−+−
- Upstream from NT to LT −+−−+−−−+++

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

After successful synchronization, resynchronization will occur if the synchword is found to be consecutively 64 times in another position in the frame than the one expected after successful synchronization.

Coding from Binary to Ternary Data

Each 4-bit block of binary data is coded into 3 ternary symbols of MMS 43 block code according to the following table.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 4
MMS 43 Coding Table

	S1	S2	S3	S4
t ⟶	t ⟶	t ⟶	t ⟶	t ⟶
0 0 0 1	0 − + 1	0 − + 2	0 − + 3	0 − + 4
0 1 1 1	− 0 + 1	− 0 + 2	− 0 + 3	− 0 + 4
0 1 0 0	− + 0 1	− + 0 2	− + 0 3	− + 0 4
0 0 1 0	+ − 0 1	+ − 0 2	+ − 0 3	+ − 0 4
1 0 1 1	+ 0 − 1	+ 0 − 2	+ 0 − 3	+ 0 − 4
1 1 1 0	0 + − 1	0 + − 2	0 + − 3	0 + − 4
1 0 0 1	+ − + 2	+ − + 3	+ − + 4	− − − 1
0 0 1 1	0 0 + 2	0 0 + 3	0 0 + 4	− − 0 2
1 1 0 1	0 + 0 2	0 + 0 3	0 + 0 4	− 0 − 2
1 0 0 0	+ 0 0 2	+ 0 0 3	+ 0 0 4	0 − − 2
0 1 1 0	− + + 2	− + + 3	− − + 2	− − + 3
1 0 1 0	+ + − 2	+ + − 3	+ − − 2	+ − − 3
1 1 1 1	+ + 0 3	0 0 − 1	0 0 − 2	0 0 − 3
0 0 0 0	+ 0 + 3	0 − 0 1	0 − 0 2	0 − 0 3
0 1 0 1	0 + + 3	− 0 0 1	− 0 0 2	− 0 0 3
1 1 0 0	+ + + 4	− + − 1	− + − 2	− + − 3

Signal Elements used for Activation and Deactivation

Certain signal elements are used for activation and deactivation which cannot appear during normal operation. In this section, only the coding is described.

Table 5
Coding of the U_{k0} Signal Elements

Upstream from NT to LT	Downstream from LT to NT
INFO U1W: 16 times ternary +++++++−−−−−−−− A tone of: Frequency: 7.5 kHz Width: 2.13 ms	INFO U2W: 16 times ternary +++++++−−−−−−−− A tone of: Frequency: 7.5 kHz Width: 2.13 ms
INFO U1A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code	INFO U2A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code
INFO U1: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)	INFO U2: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)
INFO U3: Binary continuous "1" before scrambling. Frame (Transmitting Barker code)	INFO U4H: Binary continuous "1" before scrambling with duration of 1 ms. Frame (Transmitting Barker code)
INFO U5: Binary data from the digital interface. Frame (Transmitting Barker code)	INFO U4: Binary data from the digital interface. Frame (Transmitting Barker code)
INFO U0: Ternary continuous "0" No frame, no signal level	INFO U0: Ternary continuous "0" No frame, no signal level

The IEC detects an INFO U1, U2, or U3 if the contnuous binary data is found on the descrambler output after 8 subsequent U_{k0} frames. These INFO's are detected after 8 to 9 ms.

INFO U4H is recognized if the NT finds 16 subsequent binary 1's in the data stream.

INFO U0 is recognized if the IEC-T finds one complete frame with continuous zero level.

Analog Functions of the Line Port

Input signal

The peak input signal, measured between AIN and BIN, must be below 4 V peak-to-peak. The maximum SNR is achieved with 1.3 V_{pp} (range inactive) or 2.6 V_{pp} (range active) input signal voltage.

The input impedance, measured between AIN and BIN, is at least 50 k.

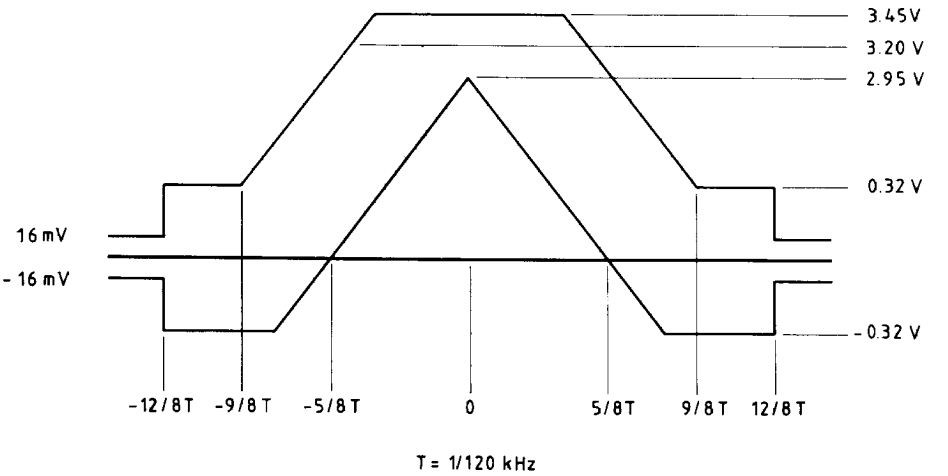
For short lines, the input signal to the ADC is automatically attenuated by 6 dB ± 1 dB in order to lower the high receive signal.

An external loop command in the C/I channel activates an internal analog test loop from the output pins to the input pins of the IEC-T. The signal is attenuated by 12 dB within this loop.

The pulse mask for a single positive pulse measured between AOUT and BOUT with a load of 172 Ω is given in the following figure.

Figure 12

Pulse Mask for a Single Positive Pulse



The peak-to-peak voltage of a single positive pulse measured between AOUT and BOUT terminated with 172 Ω is 3.20 V ± 8%.

The offset voltage, measured under the same conditions as above, is less than 2% of the peak amplitude.

The signal amplitude measured over a period of one minute varies less then 1%.

The output impedance measured between AOUT and BOUT is below 5 Ω in power-up and below 18 Ω in power-down mode. The required impedance of 150 Ω ± 5% seen from the line side of the transformer is established by putting two resistors of 41 Ω ± 1% each in the hybrid.

The load is given by the hybrid, the transformer and the subscriber line.

The transformer ratio should be 1 : 1.32 (circuit/line side) and the total inductivity seen from the line side between 5 and 10 mH.

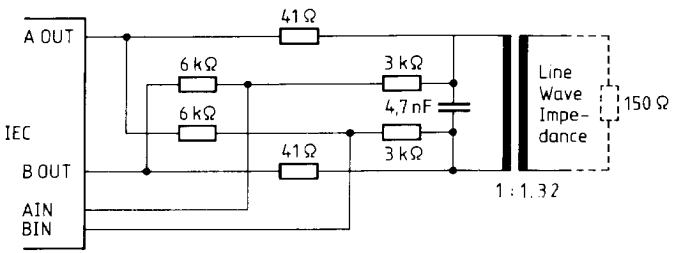
The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 100 kHz, is at least 60 dB below the signal for an evenly distributed but otherwise random sequence of + 1, 0, and -1.

External Hybrid

The hybrid balancing circuit is external to the IEC-T chip. Suggestions for the circuit configuration and dimensioning of the hybrid are given in the following figure.

Each resistor has to keep an absolute tolerance of 1%.

Figure 13
Example for Hybrid Balancing Circuit



Maintenance Functions

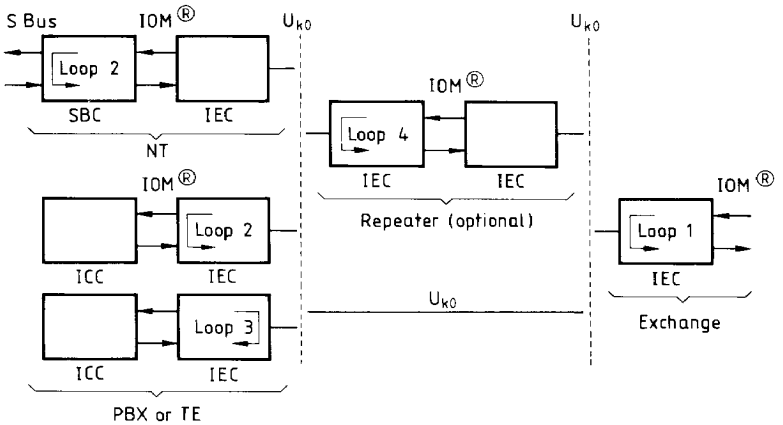
Loops

For test of the line cards, several test loops are provided which can be controlled from the exchange. When a test loop is closed, all channels (B + B + D) are looped back and data from the other end of the line is ignored. There are no separate loops for single channels.

All test loops are transparent loops. During test loops, the line signal is still transmitted. Nevertheless, the IEC-T NT or NT-RP receives this signal and synchronizes to it. The IEC-T NT or NT-RP cannot distinguish between line signals sent from LT or LT-RP during loop 1 or loop 4, and signals sent during normal operation.

Figure 14

Test Loops Closed by the IEC-T or Under its Remote Control



Loop 1, loop 4, and loop 3 are closed in the IEC-T as near to the U_{k0} interface as possible. Using internal switches, the signal from the line driver is fed back directly to the input. It is like a short-circuit between the pins AOUT and AIN as well as between BOUT and BIN. The input signal from the hybrid is ignored in this mode.

The analog loop mode is controlled via the IOM C/I channel

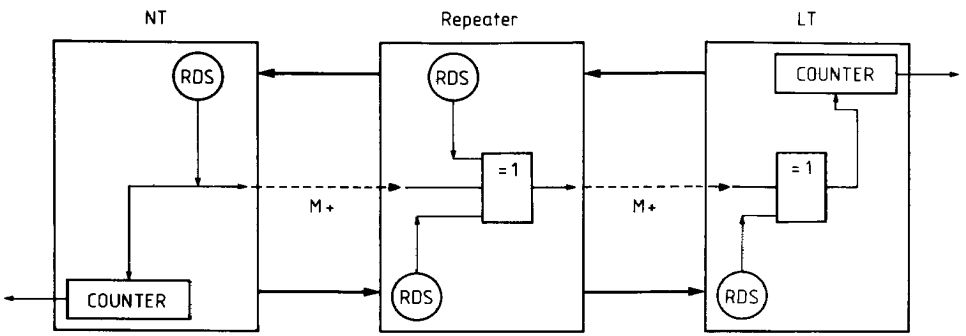
Monitoring of Code Violations

The RDS monitor computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+1,0,−1). At the end of each block, the running digital sum is the number of the next column in **table 4** which should contain the next received block. A code violation has occured if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0, three user symbols with zero polarity, is found in the received data.

In the NT modes, a positive M symbol is transmitted upstream if any code error has been detected within a frame (position 25 upstream in the U_{k0} frame from NT to LT).

The IEC-T contains an error counter which counts U_{k0} frames with at least one detected code violation. In the LT mode, additionally, the frames with a received positive M symbol are counted. The error counter can be read and simultaneously be reset from a certain state of activation via the IOM interface in all modes except the repeater modes. The counter is always stopped after reaching 255 which is the maximum value passed to the monitor channel.

Figure 15
Transmission of Detected Frame with RDS Errors



The counter is automatically reset during deactivation of the U_{k0} line. In the LT modes, it is enabled again to count code violations from the moment the RDS or AIU code is written into the IOM C/I channel, indicating that the line is synchronized. In the NT modes, it is enabled again from the moment the AID code is written into the IOM C/I channel.

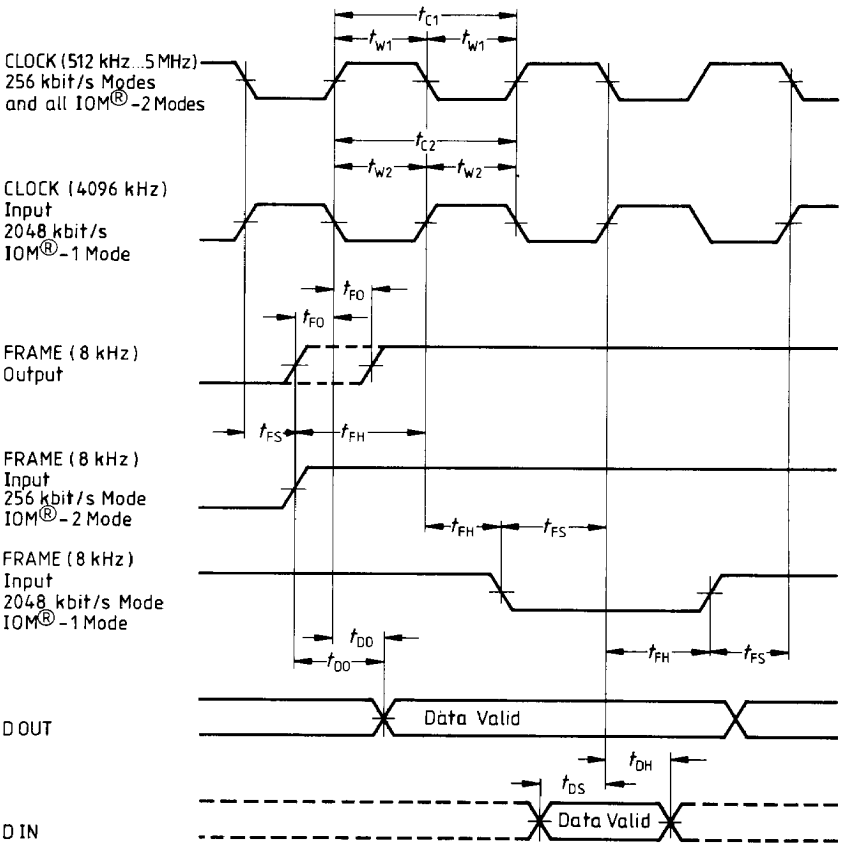
Each counted frame with a detected code violation leads to 10 to 20 binary bit errors on average. So a bit error rate of 10^{-7} in both directions leads to about 2 detected frame errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M symbol).

Static Characteristics

$V_{DD} = 4.75$ to 5.25 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
H-input voltage	V_{IH}	3.5			V	
L-input voltage	V_{IL}			1.0	V	
L-input leakage current	I_{IL}	−10			µA	V_{in} = DGND
H-input leakage current all inputs except AIN, BIN, XIN, XOUT, VREF	I_{IH}			10	µA	V_{in} = DVDD
H-output voltage all outputs except DOUT	V_{OH1}	4.0			V	$I_{OH1} = 0.4$ mA
H-output voltage DOUT (Open Drain)	V_{OH2}			V_{DD}	V	R to V_{DD}
L-output voltage all outputs except DOUT	V_{OL1}			0.33	V	$I_{OL1} = 0.4$ mA
L-output voltage DOUT (Open Drain)	V_{OL2}			0.5	V	$I_{OL2} = 6$ mA
Input capacitance DIN, MPF. CLOCK, FRAME, CLS (input) DOUT (open)	C_{IN}			10	pF	

Figure 26
Timing of Externals Signals on Digital Interface of IEC-T



Note: The rise and fall times are to be measured between 10% and 90%. A pulse width or delay is to be measured from $V_{DD}/2$ to $V_{DD}/2$ levels.

Dynamic Input Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CLOCK, FRAME, DIN, MPF	t_{rise}		30	ns
CLOCK, FRAME, DIN, MPF	t_{fall}		30	ns
FRAME	t_{fs}	30		ns
FRAME	t_{fh}	30		ns
DIN, MPF	t_{ds}	30		ns
DIN, MPF	t_{dh}	30		ns
CLOCK	t_{w1}	100		ns
CLOCK	t_{w2}	100		ns

Dynamic Output Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
CLOCK, FRAME, DISS, CLS, RD1, RD2	t_{rise}			30	ns	$C = 25$ pF
CLOCK, FRAME, DISS, CLS, RD1, RD2	t_{fall}			30	ns	$C = 25$ pF
DOUT	t_{fall}	0		200	ns	$C = 150$ pF $R = 1$ kΩ to V_{DD}
CLOCK 512 kHz 1536 kHz	t_{cl}	1875 565	1953 651	2035 735	ns ns	$C = 25$ pF
CLOCK 512 kHz 1536 kHz	t_{w1}	880 230		1075 420	ns ns	$C = 25$ pF
FRAME	t_{fo}	−30	0	30	ns	$C = 25$ pF
DOUT (high-low transition)	t_{do}	0 0		200 150	ns ns	$C = 150$ pF $R = 1$ kΩ to V_{DD} $C = 50$ pF $R = 1$ kΩ to V_{DD}

Analog Characteristics

$T_A = 70\,°C$, $V_{DD} = 4.75\ V$

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Receive Path					
Signal / (noise and distortion)	*SN*	57	62		dB
DC-level at AD-output relative to V_{DD}		0.45	0.5	0.55	
Threshold of level detect		12		41	mV
Transmit Path					
Signal / (noise distortion)	*SN*	60	65		dB
Output DC level		2,05	2.375	2.6	V
Offset between AOUT/BOUT				34.5	mV
Signal amplitude		2.95		3.45	V
Output impedance between AOUT/BOUT					
in power-up			3	5	Ω
in power-down			10	18	Ω

Power Consumptuion

Device	State of Operation	Limit Values typ.	Limit Values max.	Unit	Test Conditions
IEC-D	Power-up	140	160	mW	$V_{DD} = 5\ V$ open outputs
	Power-down	10	15	mW	
IEC-A	Power-up	125	140	mW	during normal transmission CL15 open
	Power-down	10	15	mW	

Environmetal Requirements

Storage and Transportation

The rated (limiting capability) storage and transportation temperature range prior to printed board assembly shall be as follows:

−60 °C to 125 °C (without supply voltage)
−10 °C to 80 °C (with applied voltages)

Operating Ambient Temperature

The operating ambient temperature shall be from 0 °C to 70 °C.