FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12510-9E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89130/130A Series

MB89131/P131/133A/P133A/135A/ MB89P135A/PV130A

■ DESCRIPTION

The MB89130/130A series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a great variety of peripheral functions such as timers, a serial interface, an A/D converter, and external interrupts. The MB89130A series also include a remote control transmitting output and wake-up interrupt function.

* : F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8L family CPU core
- Low-voltage operation (when an A/D converter is not used)
- Low current consumption (applicable to the dual-clock system)
- Minimum execution time : 0.95 µs at 4.2 MHz
- 21-bit timebase timer
- I/O ports : max. 36 ports
- External interrupt 1 : 3 channels
- External interrupt 2 (wake-up function) : 8 channels (only for the MB89130A series)
- 8-bit serial I/O : 1 channel

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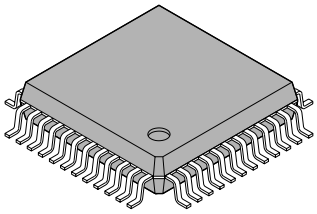
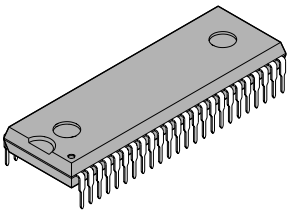
■ PACKAGE

48-pin plastic QFP



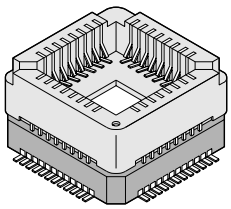
(FPT-48P-M13)

48-pin plastic SH-DIP



(DIP-48P-M01)

48-pin ceramic MQFP



(MQP-48C-P01)

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- 8/16-bit timer/counter : 1 channel
- 8-bit A/D converter : 4 channels
- Remote control transmitting frequency generator (for the MB89130A series only)
- Low-power consumption modes (stop, sleep, and watch mode)
- QFP-48 package, SH-DIP-48 package
- CMOS technology

■ PRODUCT LINEUP

Part number / Item	MB89131	MB89133A	MB89135A	MB89P133A	MB89P131
Classification	Mass-produced products (mask ROM products)			One-time PROM products	
ROM size	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	4 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)
RAM size	128 × 8 bits	256 × 8 bits			128 × 8 bits
CPU functions	The number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.95 µs at 4.2 MHz Minimum interrupt processing time : 8.57 µs at 4.2 MHz				
Ports	Output ports (N-ch open-drain ports) : 4 (All also serve as peripherals.) Output ports (CMOS) : 8 I/O ports (CMOS) : 24 (8 ports also serve as peripherals. For MB89130A, 16 ports also serve as.) Total : 36				
8/16-bit timer/ counter	8-bit timer/counter × 2 channels or a 16-bit event counter				
8-bit serial I/O	8 bits LSB/MSB first selectable				
8-bit A/D converter	8-bit resolution × 4 channels A/D conversion mode (minimum conversion time : 42 µs at 4.2 MHz) Sense mode (minimum conversion time : 11.4 µs at 4.2 MHz) Capable of continuous activation by an internal timer Reference voltage input				
External interrupt 1	3 independent channels (edge selection, interrupt vector, source flag) Rising/falling both edges selectable Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in the stop mode.)				

(Continued)

Item \ Part number	MB89131	MB89133A	MB89135A	MB89P133A	MB89P131
External interrupt 2 (wake-up function)	—	8 channels (only for level detection)			—
Remote control transmitting generator	—	1 channel (Pulse width and cycle selectable by program)			—
Standby mode	Sleep, stop, and clock mode				
Process	CMOS				
Operating voltage*	2.2 to 4.0 V (with the dual-clock option) 2.2 to 6.0 V (with the single-clock option)			2.7 V to 6.0 V	

* : Varies with conditions such as the operating frequency. (See "■ ELECTRICAL CHARACTERISTICS".)

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Part number / Item	MB89P135	MB89PV130A
Classification	One-time PROM products	Piggyback/evaluation product
ROM size	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	512 × 8 bits	1 K × 8 bits
CPU functions	The number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.95 µs at 4.2 MHz Minimum interrupt processing time : 8.57 µs at 4.2 MHz	
Ports	Output ports (N-ch open-drain ports) : 4 (All also serve as peripherals.) Output ports (CMOS) : 8 I/O ports (CMOS) : 24 (8 ports also serve as peripherals. For MB89130A, 16 ports also serve as peripherals.) Total : 36	
8/16-bit timer/counter	8-bit timer/counter × 2 channels or a 16-bit event counter	
8-bit serial I/O	8 bits LSB/MSB first selectable	
8-bit A/D converter	8-bit resolution × 4 channels A/D conversion mode (minimum conversion time : 42 µs at 4.2 MHz) Sense mode (minimum conversion time : 11.4 µs at 4.2 MHz) Capable of continuous activation by an internal timer Reference voltage input	
External interrupt 1	3 independent channels (selectable edge, interrupt vector, source flag) Rising/falling both edges selectable Used also for wake-up from the stop/sleep mode. (Edge detection is also permitted in the stop mode.)	
External interrupt 2 (wake-up function)	8 channels (only for level detection)	
Remote control transmitting frequency generator	1 channel (Pulse width and cycle selectable by program)	
Standby mode	Sleep, stop, and clock mode	
Process	CMOS	
Operating voltage	2.7 V to 6.0 V	2.7 V to 6.0 V
EPROM for use	—	MBM27C256A-20TVM

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89131	MB89133A	MB89135A	MB89P133A	MB89P131
FPT-48P-M13	○	○	○	○	○
DIP-48P-M01	×	○	×	○	×
MQP-48C-P01	×	×	×	×	×

Package	MB89P135A	MB89PV130A
FPT-48P-M13	○	×
DIP-48P-M01	×	×
MQP-48C-P01	×	○

○ : Available, × : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTPROM (one-time PROM) products, verify its differences from the product that will actually be used. Take particular care on the following points :

- The number of register banks available is different among the MB89131, MB89133A/135A and MB89P135A/PV130A.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- When operated at low speed, the product with an OTPROM will consume more current than the product with a mask ROM.
  However, the same is current consumption in sleep/stop modes. (For more information, see "■ ELECTRICAL CHARACTERISTICS".)
- In the case of the MB89PV130A, added is the current consumed by the EPROM which is connected to the top socket.

3. Mask Options

Functions that can be selected as options and how to designate these options vary with product.

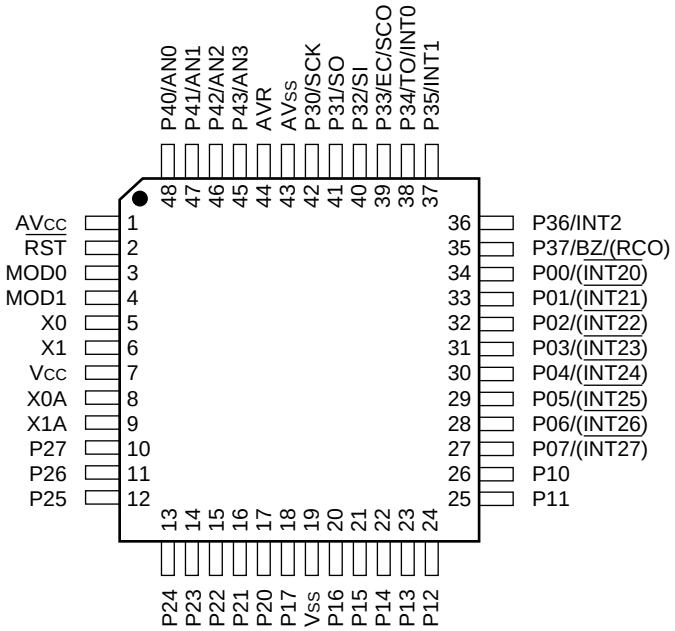
Before using options, check "■ MASK OPITONS".

Take particular care on the following point :

- P40 to P43 must be set to no pull-up resistor when an A/D converter is used.
- For MB89P135A, pull-up resistor option cannot be set for P40 to P43.
- Each option is fixed on the MB89PV130A.

■ PIN ASSIGNMENT

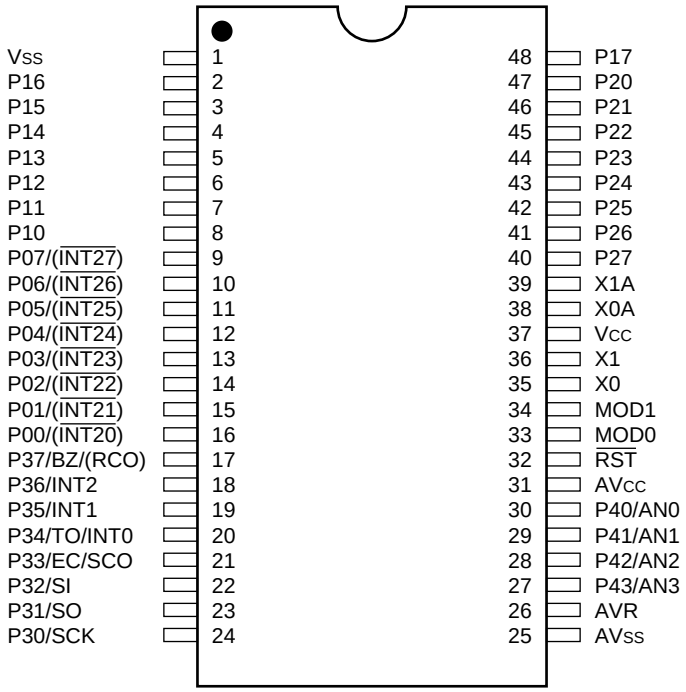
(TOP VIEW)



(FPT-48P-M13)

Note : Parenthesized function is available only for the MB89130A series.

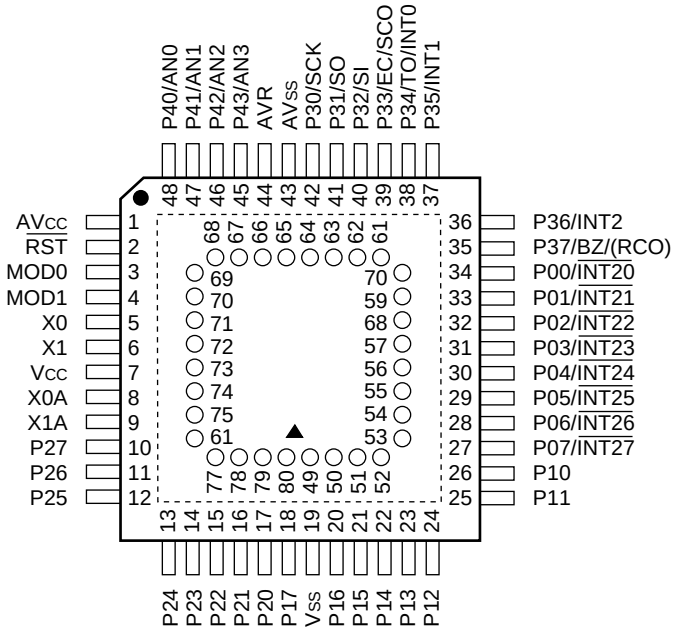
(TOP VIEW)



(DIP-48P-M01)

Note : Parenthesized function is available only for the MB89130A series.

(TOP VIEW)



(MQP-48C-P01)

- **Pin assignment on package top**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	V_{PP}	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{SS}	72	N.C.	80	V_{CC}

N.C. : Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
35	5	X0	A	Main clock crystal oscillator pins (max. 4.2 MHz)
36	6	X1		
38	8	X0A	B	Subclock crystal oscillator pins (32.768 kHz)
39	9	X1A		
33	3	MOD0	C	Operation mode selecting pins Connect directly to V_{SS}.
34	4	MOD1		
32	2	$\overline{RST}$	D	Reset I/O pin This pin is of N-ch open-drain output type with pull-up resistor, and a hysteresis input type. The internal circuit is initialized by the input of “L”. “L” is output from this pin by an internal reset source as a option.
16 to 9	34 to 27	P00 ($\overline{INT20}$) to P07 ($\overline{INT27}$)	I	General-purpose I/O ports On the MB89130A series, these ports also serve as an external interrupt input. External interrupt inputs are of hysteresis input type.
8 to 2, 48	26 to 20, 18	P10 to P17	E	General-purpose I/O ports
47 to 40	17 to 10	P20 to P27	G	General-purpose output ports
24	42	P30/SCK	F	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O. This port is of hysteresis input type.
23	41	P31/SO	F	General-purpose I/O port Also serves as a 8-bit serial I/O data output. This port is of hysteresis input type.
22	40	P32/SI	F	General-purpose I/O port Also serves as a 8-bit serial I/O data input. This port is of hysteresis input type.
21	39	P33/EC/SCO	F	General-purpose I/O port Also serves as the external clock input for the 8-bit timer/counter. This port is of hysteresis input type. The system clock output is provided as an option.
20	38	P34/TO/INT0	F	General-purpose I/O port Also serve as the overflow output for the 8-bit timer/counter and an external interrupt input. This port is of hysteresis input type.
19, 18	37, 36	P35/INT1, P36/INT2	F	General-purpose I/O ports Also serves as an external interrupt input. These ports are of hysteresis input type.

*1 : DIP-48P-M01

*2 : FPT-48P-M13

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Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
17	35	P37/BZ/ (RCO)	F	General-purpose I/O port Also serves as a buzzer output. This port is of hysteresis input type. On the MB89130A series, this port also serves as a remote control output.
30 to 27	48 to 45	P40/AN0 to P43/AN3	H	N-ch open-drain output ports Also serve as an analog input for the A/D converter.
37	7	V_{CC}	—	Power supply pin
1	19	V_{SS}	—	Power supply (GND) pin
31	1	AV_{CC}	—	A/D converter power supply pin Use this pin at the same voltage as V_{CC}.
26	44	AVR	—	A/D converter reference voltage input pin
25	43	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.

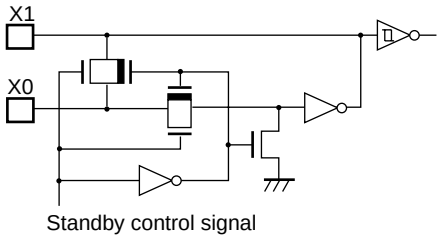
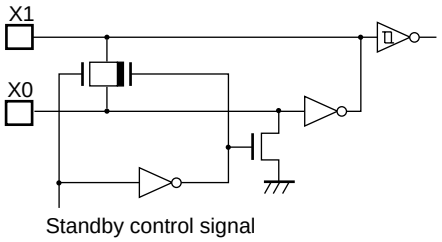
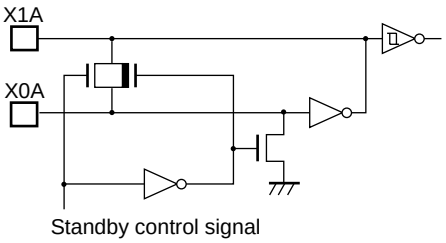
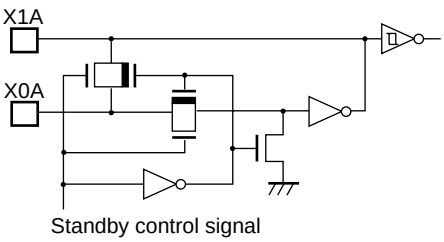
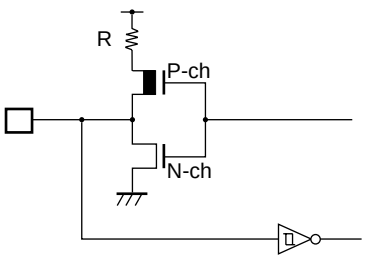
*1 : DIP-48P-M01

*2 : FPT-48P-M13

- **External EPROM pins (MB89PV130A only)**

Pin no.	Pin name	I/O	Function
49	V_{PP}	O	“H” level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
61 62 63	O1 O2 O3	I	Data input pins
64	V_{SS}	O	Power supply (GND) pin
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins
70	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
71	A10	O	Address output pin
73	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins
80	V_{CC}	O	EPROM power supply pin
56 57 72 74	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) Circuit for the MB89P133A/P131/P135A/PV130A External clock input selecting versions of MB89131/133A/135A Oscillation feedback resistor of approximately 1 MΩ/5 V
		• Crystal or ceramic oscillation type (main clock) Crystal or ceramic oscillation selecting versions of MB89131/133A/135A Oscillation feedback resistor of approximately 1 MΩ/5 V
B		• Crystal and ceramic oscillation type (subclock) Circuit for the MB89131/133A/135A Oscillation feedback resistor of approximately 4.5 MΩ/5 V
		• Crystal and ceramic oscillation type (subclock) Circuit for the MB89P131/P133A/P135A/PV130A Oscillation feedback resistor of approximately 4.5 MΩ/5 V
C		
D		• Output pull-up resistor (P-ch) of approximately 50 kΩ/5 V • Hysteresis input

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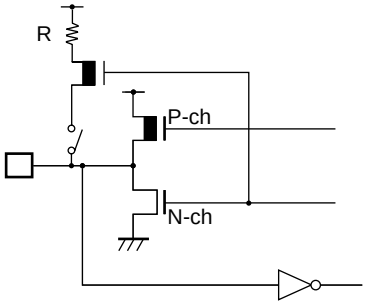
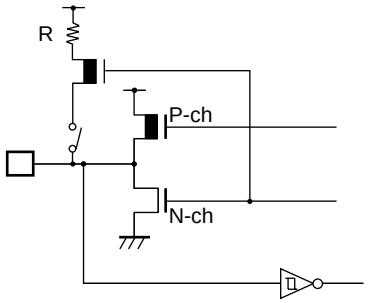
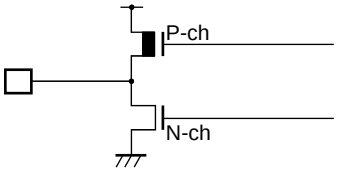
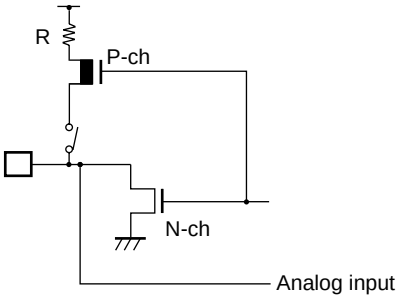
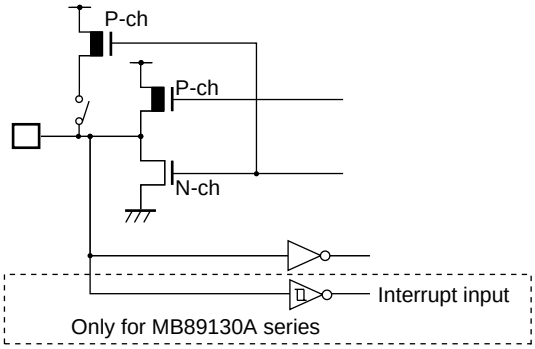
Type	Circuit	Remarks
E		• CMOS output • CMOS input • Pull-up resistor optional
F		• CMOS output • Hysteresis input • Pull-up resistor optional
G		• CMOS output
H		• N-ch open-drain output • Analog input • Pull-up resistor optional
I		• CMOS output • CMOS input • The interrupt input is a hysteresis input (available only for the MB89130A series) . • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although operation is assured within the rated range of V_{CC} power supply voltage, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

7. Turning on the supply voltage (only for the MB89P135A)

Power on sharply up to the option enabling voltage (2 V) within 13 clock cycles after starting of oscillation.

■ PROGRAMMING TO THE EPROM ON THE MB89P131

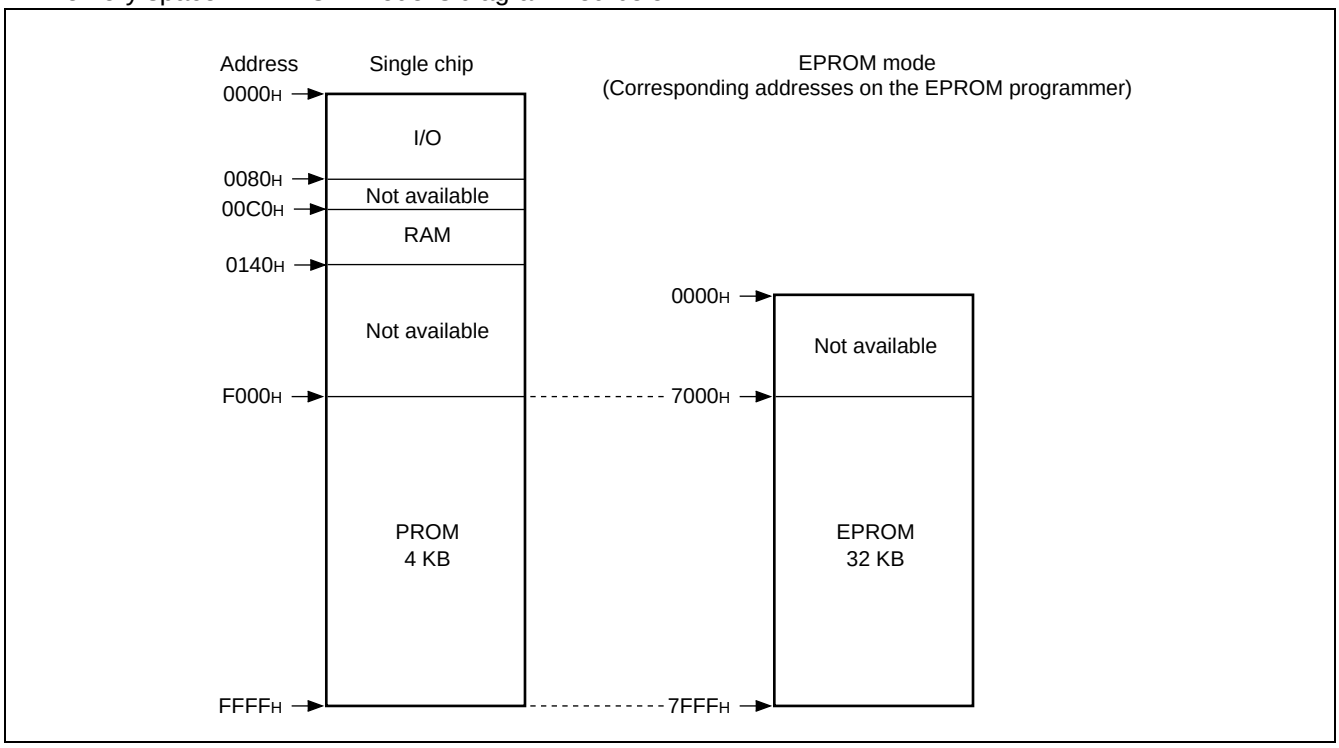
The MB89P131 is an OTPROM version of the MB89131.

1. Features

- 4-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P131 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 7000_H to $7FFF_H$ (note that addresses $F000_H$ to $FFFF_H$ while operating as a single chip correspond to 7000_H to $7FFF_H$ in EPROM mode) .

(3) Program with the EPROM programmer.

■ PROGRAMMING TO THE EPROM ON THE MB89P133A

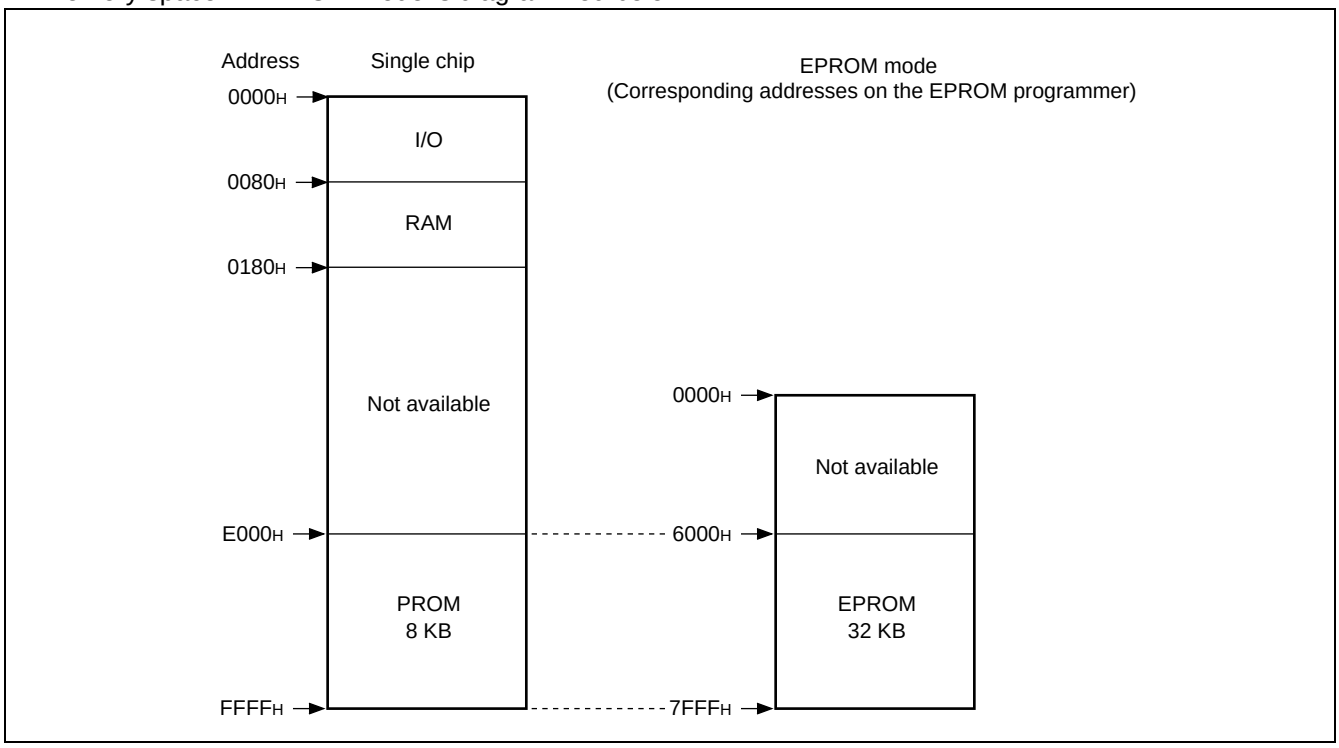
The MB89P133A is an OTPROM version of the MP89133A.

1. Features

- 8-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P133A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 6000_H to $7FFF_H$ (note that addresses $E000_H$ to $FFFF_H$ while operating as a single chip correspond to 6000_H to $7FFF_H$ in EPROM mode) .

(3) Program with the EPROM programmer.

■ PROGRAMMING TO THE EPROM ON THE MB89P135A

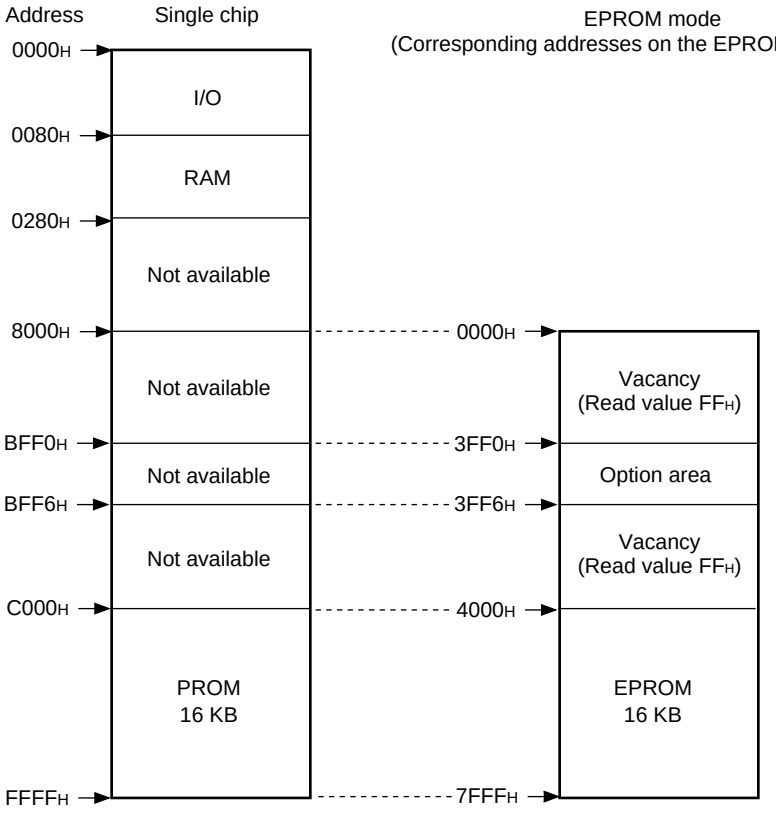
The MB89P135A is an OTPROM version of the MB89133A/135A.

1. Features

- 16-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P135A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000H to 7FFFH (note that addresses C000H to FFFFH while operating as a single chip correspond to 4000H to 7FFFH in EPROM mode) .

(3) Load option data into the EPROM programmer at 3FF0H to 3FF6H.

(4) Program with the EPROM programmer.

4. Setting OTPROM Options (MB89P135A Only)

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map :

- **OTPROM option bit map**

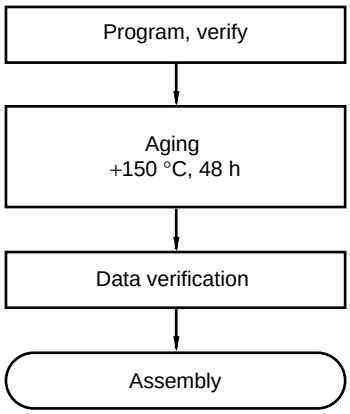
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Clock mode selection 1 : Single clock 0 : Dual clock	Reset pin output 1 : Yes 0 : No	Power-on reset 1 : Yes 0 : No	Oscillation stabilization time 00 : $2^2/F_{CH}$ 01 : $2^{12}/F_{CH}$	 10 : $2^{16}/F_{CH}$ 11 : $2^{18}/F_{CH}$
3FF1H	P07 Pull-up 1 : Yes 0 : No	P06 Pul-up 1 : Yes 0 : No	P05 Pull-up 1 : Yes 0 : No	P04 Pull-up 1 : Yes 0 : No	P03 Pull-up 1 : Yes 0 : No	P02 Pull-up 1 : Yes 0 : No	P01 Pull-up 1 : Yes 0 : No	P00 Pull-up 1 : Yes 0 : No
3FF2H	P17 Pull-up 1 : No 0 : Yes	P16 Pull-up 1 : No 0 : Yes	P15 Pull-up 1 : Yes 0 : No	P14 Pull-up 1 : Yes 0 : No	P13 Pull-up 1 : Yes 0 : No	P12 Pull-up 1 : Yes 0 : No	P11 Pull-up 1 : Yes 0 : No	P10 Pull-up 1 : Yes 0 : No
3FF3H	P37 Pull-up 1 : Yes 0 : No	P36 Pull-up 1 : Yes 0 : No	P35 Pull-up 1 : Yes 0 : No	P34 Pull-up 1 : Yes 0 : No	P33 Pull-up 1 : Yes 0 : No	P32 Pull-up 1 : Yes 0 : No	P31 Pull-up 1 : Yes 0 : No	P30 Pull-up 1 : Yes 0 : No
3FF4H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF5H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF6H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable

Note : Each bit is set to ‘1’ as the initialized value, therefore the pull-up option is selected.

■ HANDLING THE MB89P131/P133A/P135A

1. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.



2. Programming Yield

Due to its nature, bit programming test can't be conducted as Fujitsu delivery test.
For this reason, a programming yield of 100% cannot be assured at all times.

3. EPROM Programmer Socket Adapter

Part no.	Package	Compatible socket adapter Sun Hayato Co., Ltd.	Recommended programmer manufacturer and programmer name
			Minato Electronics Inc.
			1890A
MB89P131PF	QFP-48	ROM-48QF2-28DP-8L	Recommended
MB89P133APFM			—
MB89P133AP	SH-DIP-48	ROM-48SD-28DP-8L2	—

Inquiry : Sun Hayato Co., Ltd. : TEL (81) -3-3986-0403
FAX (81) -3-5396-9106

Minato Electronics Inc. : TEL : USA (1) -916-348-6066
JAPAN (81) -45-591-5611

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adapter

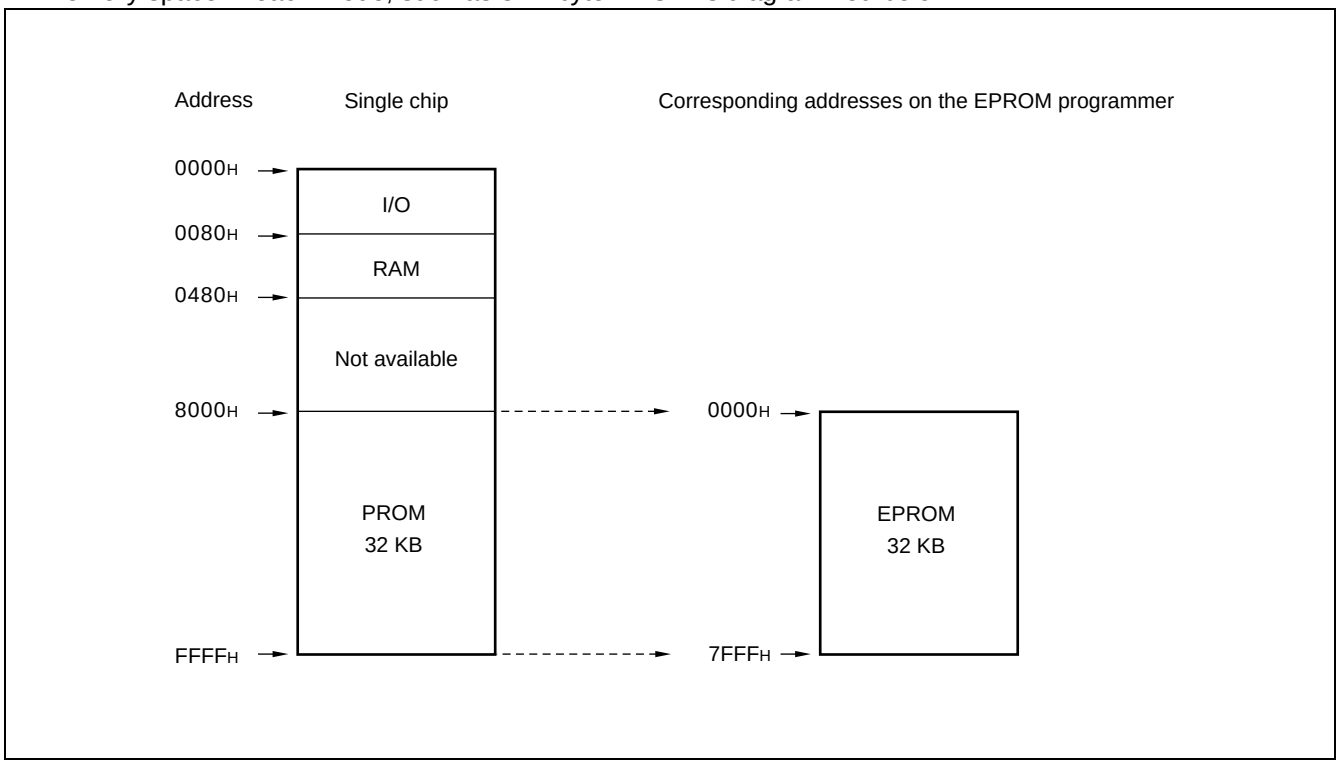
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer : Sun Hayato Co., Ltd.) listed below :

Package	Socket adapter part number
LCC-32 (Square)	ROM-32LC-28DP-S

Inquiry : Sun Hayato Co., Ltd. : TEL (81) -3-3986-0403
FAX (81) -3-5396-9106

3. Memory Space

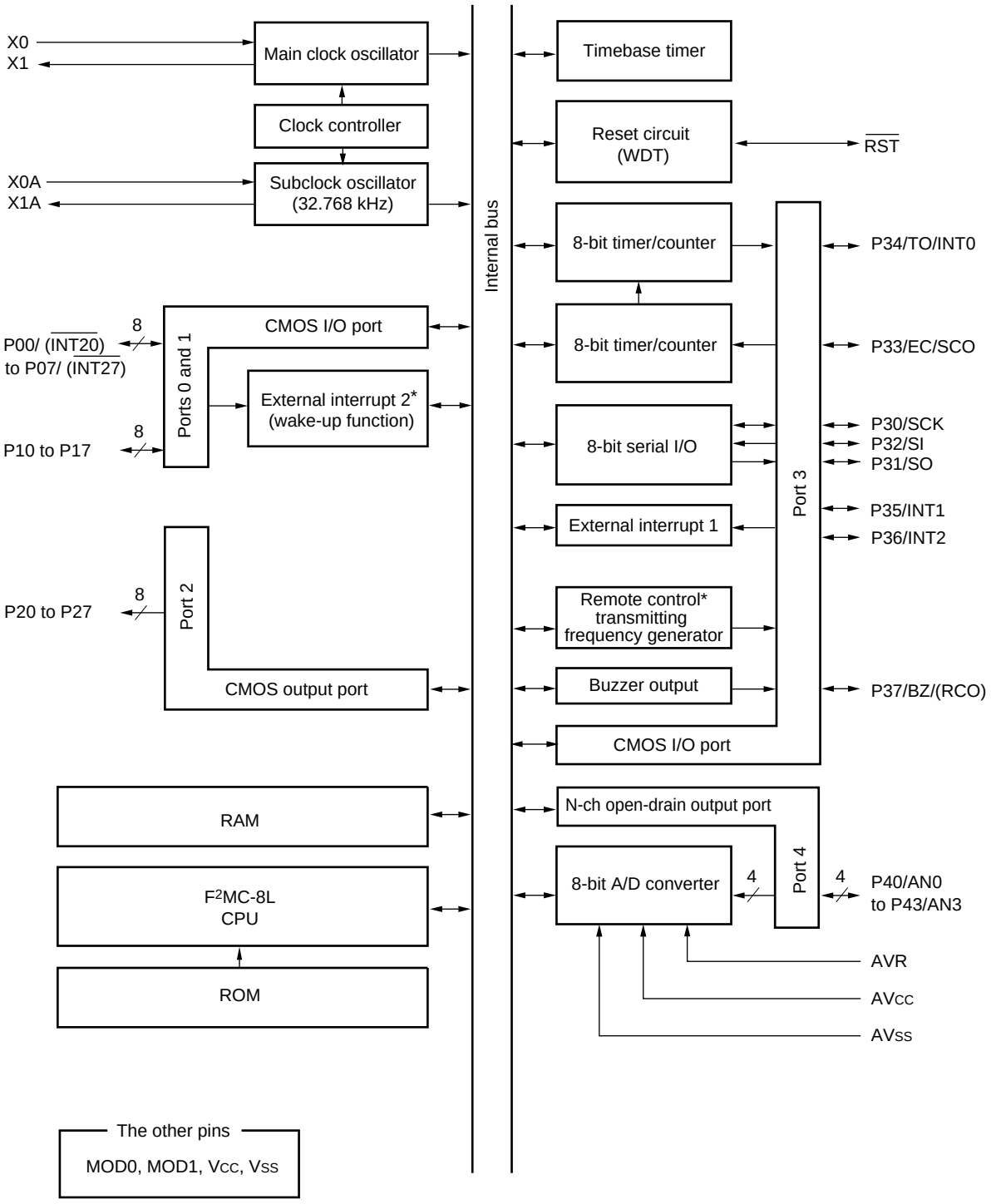
Memory space in each mode, such as 32-Kbyte PROM is diagrammed below.



4. Programming to the EPROM

(1) Set the EPROM programmer for the MBM27C256A.
(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.
(3) Program with the EPROM programmer.

■ BLOCK DIAGRAM



* : Only for the MB89130A series.

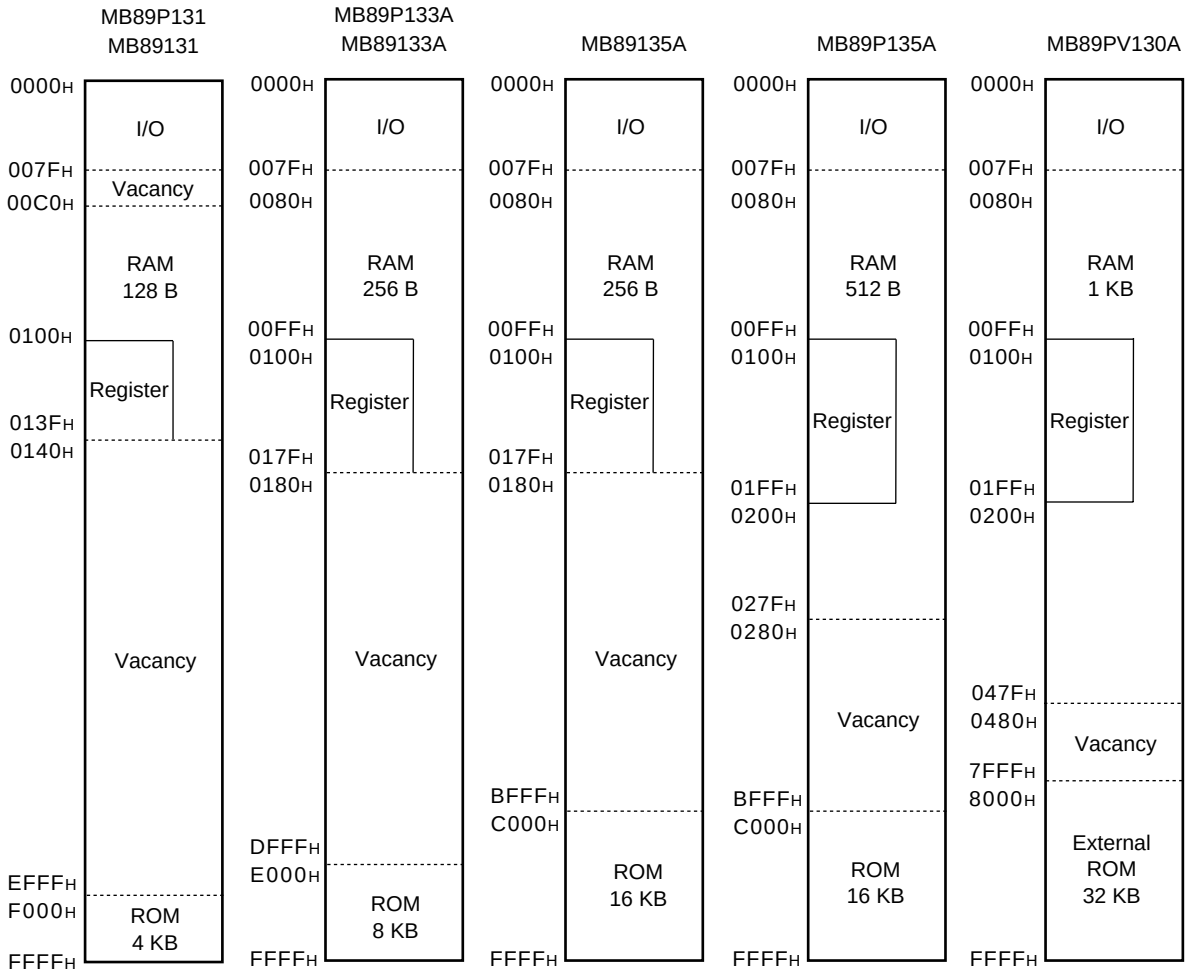
Note : Parenthesized pin function is only for the MB89130A series.

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89130/130A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address within the program area. The memory space of the MB89130/130A series is structured as illustrated below.

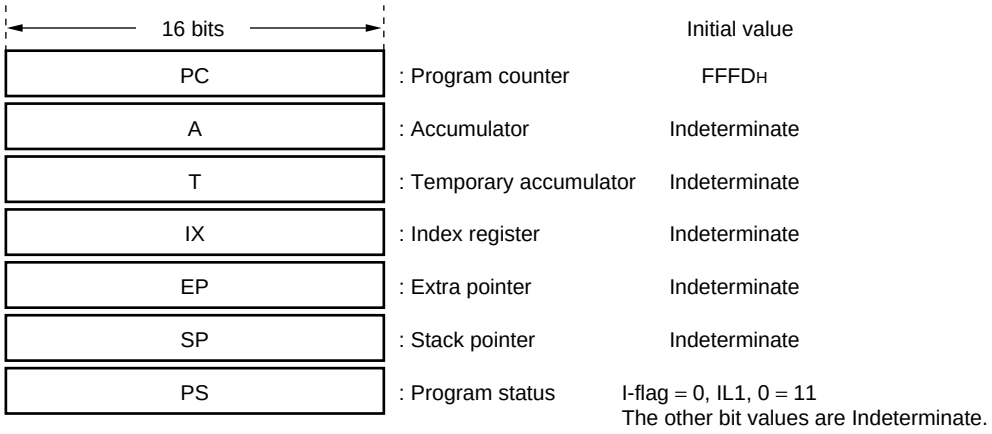
- **Memory Space**



2. Registers

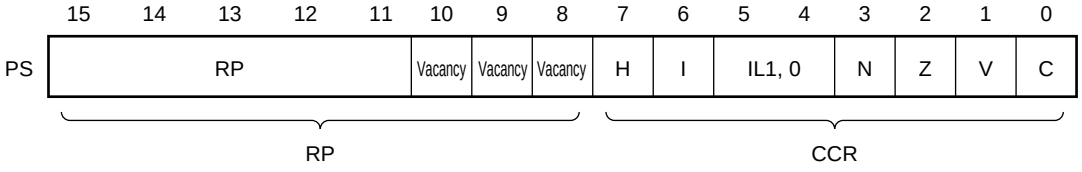
The F²MC-8L family has two types of registers; dedicated hardware registers in the CPU and general-purpose memory registers. The following registers are provided :

Program counter (PC) :	A 16-bit register for indicating the instruction storage positions.
Accumulator (A) :	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T) :	A 16-bit register which is used for arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX) :	A 16-bit register for index modification
Extra pointer (EP) :	A 16-bit pointer for indicating a memory address
Stack pointer (SP) :	A 16-bit pointer for indicating a stack area
Program status (PS) :	A 16-bit register for storing a register pointer, a condition code



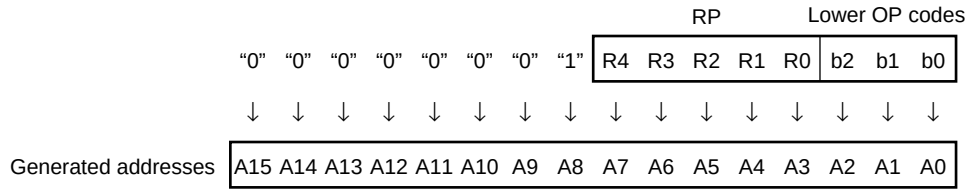
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) . (See the diagram below.)

- **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

H-flag : Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag : Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' otherwise.

Z-flag : Set to '1' when an arithmetic operation results in '0'. Cleared to '0' otherwise.

V-flag : Set to '1' if the complement on '2' overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

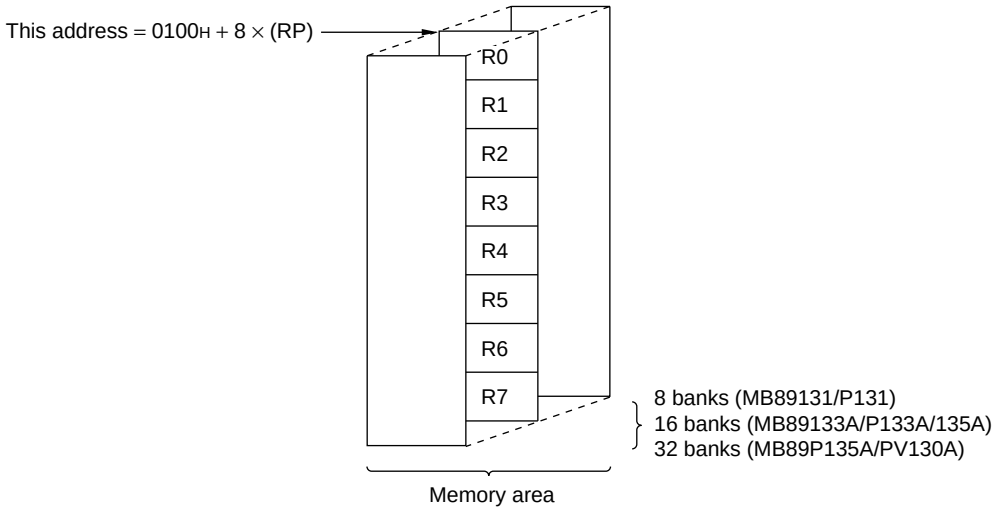
C-flag : Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : An 8-bit resister for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 8 banks can be used on the MB89131/P131 and a total of 16 banks can be used on the MB89133A/P133A/135A and a total of 32 banks can be used on the MB89P135A/PV130A. The bank currently in use is indicated by the register bank pointer (RP) .

- **Register Bank Configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H			Vacancy
06H			Vacancy
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Timebase timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(R/W)	BZCR	Buzzer register
10H			Vacancy
11H			Vacancy
12H	(R/W)	SCGC	Peripheral control clock register
13H			Vacancy
14H	(R/W)	RCR1	Remote control transmitting control register 1*
15H	(R/W)	RCR2	Remote control transmitting control register 2*
16H			Vacancy
17H			Vacancy
18H	(R/W)	T2CR	Timer 2 control register
19H	(R/W)	T1CR	Timer 1 control register
1AH	(R/W)	T2DR	Timer 2 data register
1BH	(R/W)	T1DR	Timer 1 data register
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH			Vacancy
1FH			Vacancy

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20_H	(R/W)	ADC1	A/D converter control register 1
21_H	(R/W)	ADC2	A/D converter control register 2
22_H	(R/W)	ADCD	A/D converter data register
23_H	(R/W)	EIC1	External interrupt 1 control register 1
24_H	(R/W)	EIC2	External interrupt 1 control register 2
25_H	Vacancy		
26_H to 31_H	Vacancy		
32_H	(R/W)	EIE2	External interrupt 2 enable register*
33_H	(R/W)	EIF2	External interrupt 2 flag register*
34_H to $7B_H$	Vacancy		
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$	Vacancy		

* : Only for the MB89130A series

Note : Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.2	V	*
	AVR	V_{SS} – 0.3	V_{SS} + 7.2	V	AVR must not exceed V_{CC} + 0.3 V
Program voltage	V_{PP}	V_{SS} – 0.6	V_{SS} + 13.0	V	Only for the MB89P131/P133A/P135A
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	10	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	20	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–10	mA	
“H” level average output current	I_{OHAV}	—	–2	mA	Average value (operating current × operating rate)
“H” level total maximum output current	ΣI_{OH}	—	–30	mA	
“H” level total average output current	ΣI_{OHAV}	—	–10	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set to the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

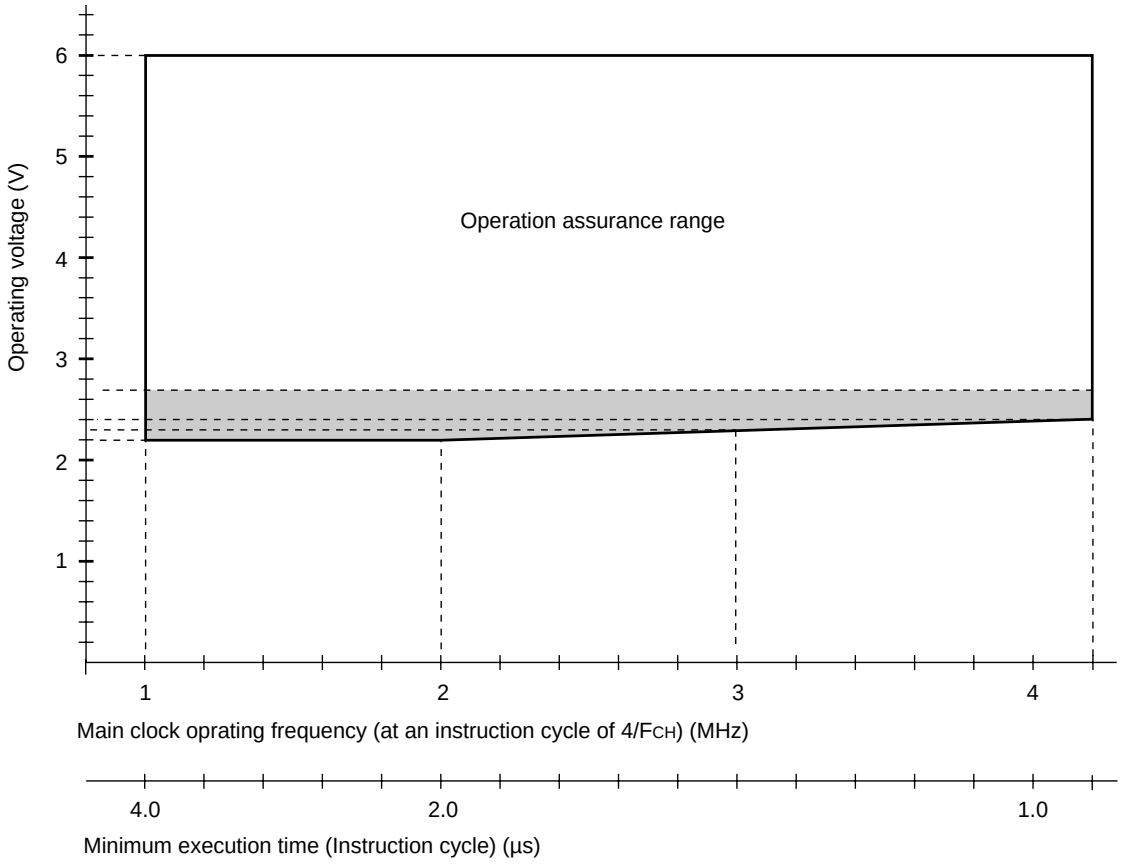
2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89131/133A/135A
		2.7*	6.0*	V	Normal operation assurance range* MB89P131/P133A/135A/PV130A
		1.5	6.0	V	Retains the RAM state in the stop mode
	AVR	2.0	AV_{CC}	V	
Operating temperature	T_A	−40	+85	°C	

* : These values vary with the operating frequencies and the analog assurance range. See Figure 1 and 2, and "5. A/D Converter Electrical Characteristics."

Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MB89P131/P133A/P135A/PV130A, and single-clock MB89131/133/133A/135/135A)



Note : The shaded area is assured only for the MB89131/133/133A/135/135A.

Figure 2 Operating Voltage vs. Main Clock Operating Frequency (Dual-clock MB89131/133/133A/135/135A)

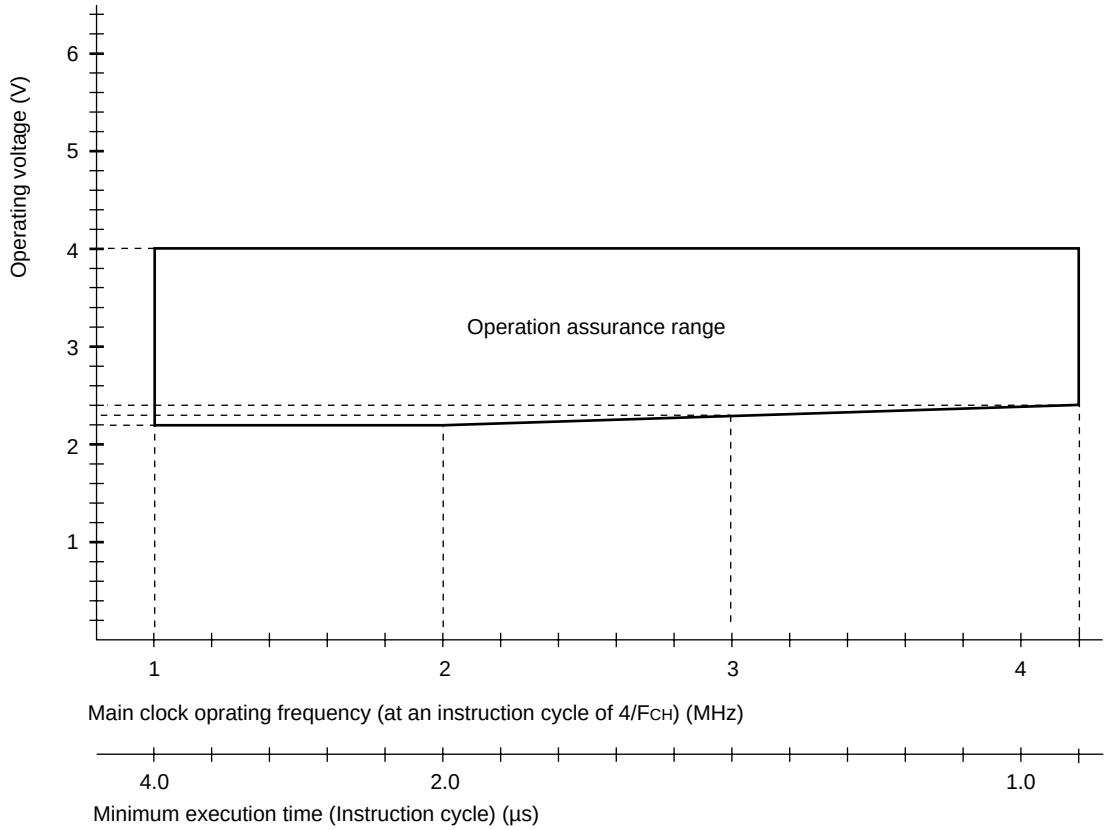


Figure 1 and 2 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

($AV_{CC} = V_{CC} = +5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, P30 to P37, $\overline{INT20}$ to $\overline{INT27}$		0.8 V_{CC}	—	V_{CC} + 3.0	V	$\overline{INT20}$ to $\overline{INT27}$ are available only for the MB89130A series.
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, P30 to P37 $\overline{INT20}$ to $\overline{INT27}$		V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{INT20}$ to $\overline{INT27}$ are available only for the MB89130A series.
Open-drain output pin applied voltage	V_D	P40 to P43		V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37	$I_{OH} = -2.0$ mA	2.4	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43	$I_{OL} = 1.8$ mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	$I_{OL} = 4.0$ mA	—	—	0.6	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P43, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P43, $\overline{RST}$	$V_I = 0.0$ V	25	50	100	kΩ	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC1}	V_{CC} (External clock operation)	F_{CH} = 4.00 MHz V_{CC} = 5.0 V t_{inst}*2 = 1.0 µs	—	4	7	mA	MB89131/133A/135A
				—	6	10	mA	MB89P131/P133A/P135A
	I_{CCS1}		F_{CH} = 4.00 MHz V_{CC} = 5.0 V t_{inst}*2 = 1.0 µs Main clock sleep mode	—	2	5	mA	
	I_{CCL}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V Subclock mode	—	50	100	µA	MB89131/133A/135A
				—	1	3	mA	MB89P131/P133A/P135A
	I_{CCLS}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V Subclock sleep mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz V_{CC} = 3.0 V • Watch mode • Main clock stop mode in dual-clock system	—	—	15	µA	
	I_{CCH}		T_A = +25 °C • Subclock stop mode • Main clock stop mode in single-clock system	—	—	1	µA	
	I_A	AV_{CC}	F_{CH} = 4 MHz, when A/D conversion is operating	—	1	3	mA	
	I_{AH}	AV_{CC}	F_{CH} = 4 MHz, T_A = +25 °C, when A/D conversion is not operating	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1 : The power supply current is measured at the external clock.

*2 : For information on t_{inst}, see “ (4) Instruction Cycle” in “4. AC Characteristics.”

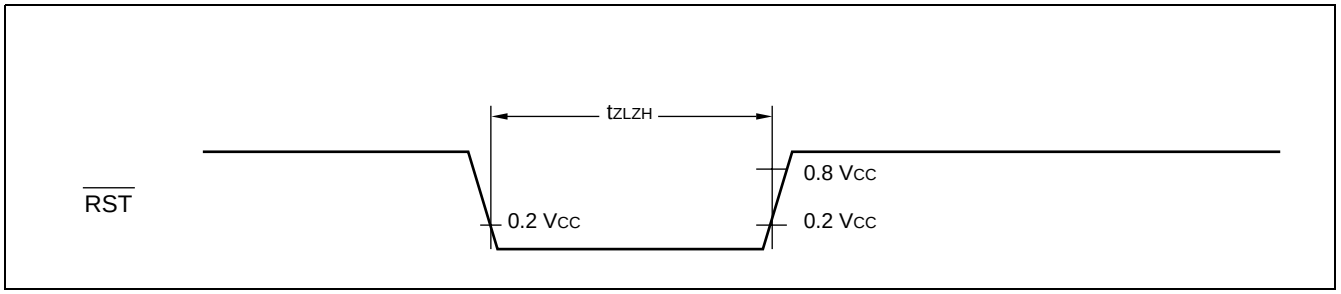
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}*	—	ns	

* : t_{HCYL} is the oscillation cycle (1/F_{CH}) to input to the X0 pin.

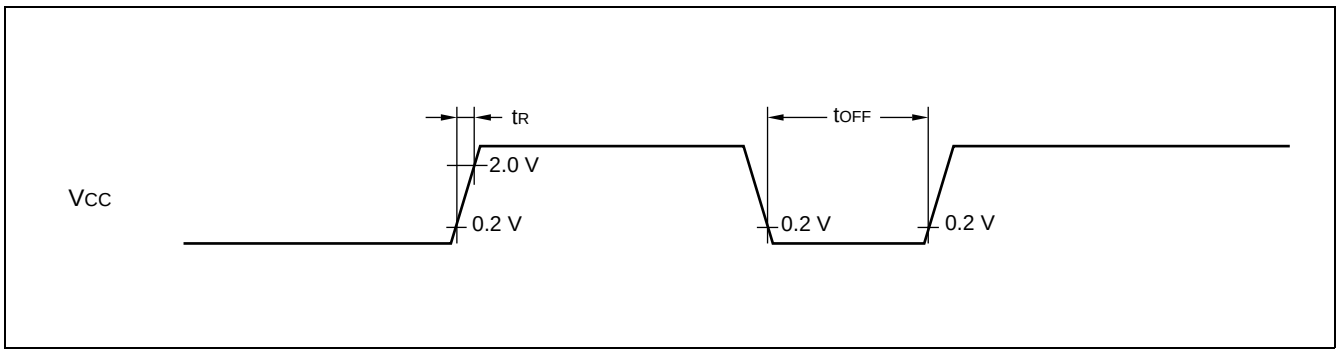


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note : Make sure that power supply rises within the oscillation stabilization time selected.
For example, when the main clock is operating at 3 MHz (F_{CH}) and the oscillation stabilization time selecting option has been set to $2^{12}/F_{CH}$, the oscillation stabilization time is 1.4 ms. Therefore, the maximum value of power supply rising time is about 1.4 ms.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

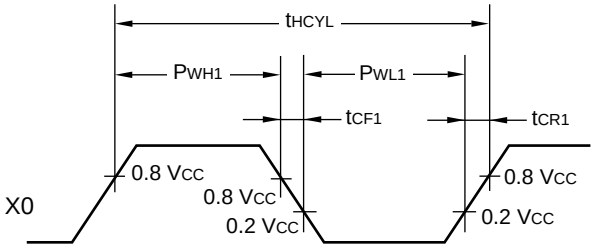


(3) Clock Timing

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

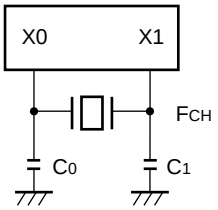
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Input clock frequency	F_{CH}	X0, X1	1	—	4.2	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	238	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH1} P_{WL1}	X0	30	—	—	ns	External clock
Input clock rising/falling time	t_{CR1} t_{CF1}	X0	—	—	24	ns	External clock

- **X0 and X1 Timing and Conditions of Applied Voltage**

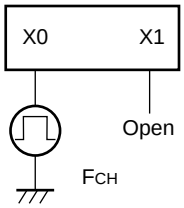


- **Main Clock Conditions**

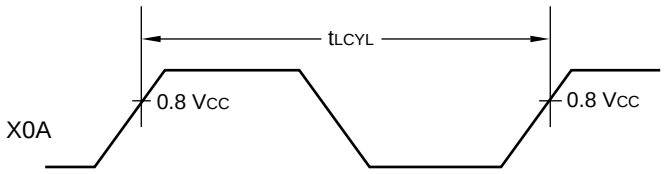
When a crystal
or
ceramic resonator is used



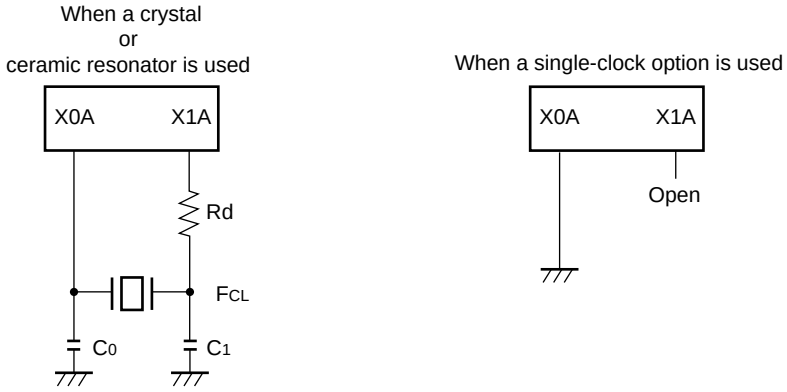
When an external clock is used



- **X0A and X1A Timing and Conditions of Applied Voltage**



- **Subclock Conditions**

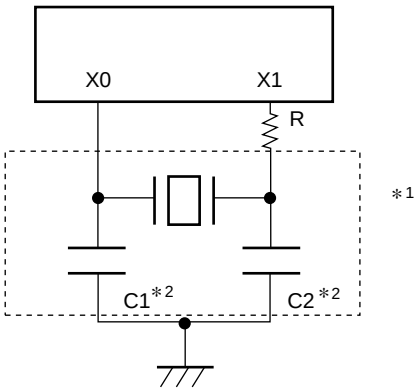


(4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 1.0 µs when operating at F_{CH} = 4 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

(5) Recommended Resonator Manufacturers

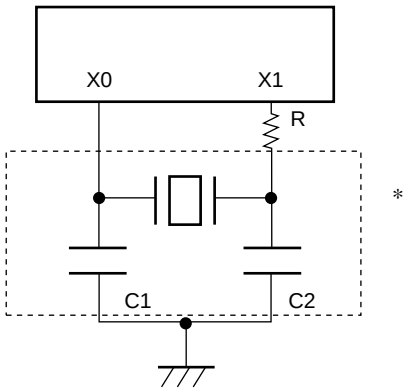
- **Sample Application of Piezoelectric Resonator (FAR Family) for Main Clock Oscillation Circuit**



FAR part number*1 (built-in capacitor type)	Frequency (MHz)	Dumping resistor	Initial deviation of FAR frequency (T_A = +25 °C)	Temperature characteristics of FAR frequency (T_A = −20 °C to +60 °C)	Loading capacitors*2
FAR-C4CC-02000-L00	2.00	1000 Ω	±0.5%	±0.5%	Built-in
		510 Ω	±0.5%	±0.5%	
FAR-C4□C-02000-□20		—	±0.5%	±0.5%	
FAR-C4□A-03000-□20	3.00	1 kΩ	±0.5%	±0.5%	
FAR-C4□A-04000-□01	4.00	750 Ω	±0.5%	±0.5%	
FAR-C4□A-04000-□21		—	±0.5%	±0.5%	
FAR-C4CB-04000-M00		—	±0.5%	±0.5%	
FAR-C4□B-04000-□00		—	±0.5%	±0.5%	
FAR-C4□B-04194-□00	4.194	—	±0.5%	±0.5%	

Inquiry : FUJITSU MEDIA DEVICES LIMITED

- **Sample Application of Ceramic Resonator for Main Clock Oscillation Circuit**



- **Mask ROM products**

Resonator manufacturer*	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Kyocera Corporation	KBR-4.0MKS	4.00	33	33	Not required
Matsushita Electronic Components Co,. Ltd.	EFOV4004B	4.00	33 (Built-in)	33 (Built-in)	1.5 kΩ
Murata Mfg. Co., Ltd.	CSBF1000J	1.00	100	100	6.8 kΩ
	CSA4.00MG	4.00	30	30	Not required
	CST4.00MGW		Built-in	Built-in	Not required
	CSA4.00MGU		30	30	Not required
	CST4.00MGWU		Built-in	Built-in	Not required
	CSA4.00MGU040		100	100	Not required
	CST4.00MGWU040		Built-in	Built-in	Not required
	CSTCS4.00MG		Built-in	Built-in	Not required
	CSTCS4.00MGWOC5		Built-in	Built-in	Not required
TDK Corporation	CCR4.0MC3	4.00	Built-in	Built-in	Not required

(Continued)

(Continued)

• **One-time PROM products**

Resonator manufacturer*	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Murata Mfg. Co., Ltd.	CSA3.00MG040	3.00	100	100	Not required
	CST3.00MGW040		Built-in	Built-in	Not required
	CSA4.00MG	4.00	30	30	Not required
	CSA4.00MGU		30	30	Not required
	CST4.00MGWU		Built-in	Built-in	Not required
	CSA4.00MGU040		100	100	Not required
	CST4.00MGWU040		Built-in	Built-in	Not required
	CSTCS4.00MG		Built-in	Built-in	Not required

Inquiry : Kyocera Corporation

- AVX Corporation
  North American Sales Headquarters : TEL 1-803-448-9411
- AVX Limited
  European Sales Headquarters : TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters : TEL 852-363-3303

Matsushita Electronic Components Co., Ltd.

- North America
  Panasonic Industrial Co. : TEL 1-201-348-7000
- Canada
  Matsushita Electric of Canada Ltd. : TEL 905-238-2436
- Europe
  Panasonic Industrial Europe (Continental) : TEL 49-40-8549-2048
  Panasonic Industrial Europe (Nlederlassung Munchen) : TEL 49-89-4800-7150
- Asia
  Panasonic Industry of Asia, Company : TEL 65-299-8400

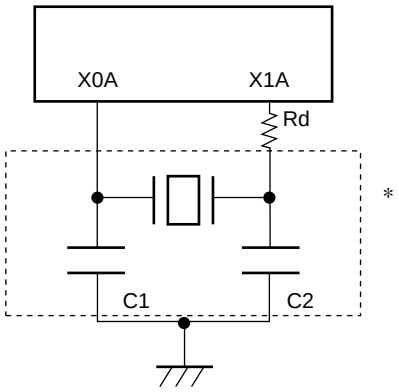
Murata Mfg. Co., Ltd.

- Murata Electronics North America, Inc. : TEL 1-404-436-1300
- Murata Europe Management GmbH : TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd. : TEL 65-758-4233

TDK Corporation

- TDK Corporation of America
  Chicago Regional Office : TEL 1-708-803-6100
- TDK Electronics Europe GmbH
  Components Division : TEL 49-2102-9450
- TDK Singapore (PTE) Ltd. : TEL 65-273-5022
- TDK Hongkong Co., Ltd. : TEL 852-736-2238
- Korea Branch, TDK Corporation : TEL 82-2-554-6633

• **Sample Application of Crystal Resonator for Subclock Oscillation Circuit**



• **Mask ROM products**

Resonator manufacturer*	Resonator	Frequency (kHz)	C1 (pF)	C2 (pF)	Rd (kΩ)
SII	DS-VT-200	32.768	24	24	680

Inquiry : SII

- Seiko Instruments Inc. (Japan) : TEL 81-43-211-1219
- Seiko Instruments U.S.A. Inc. : TEL 310-517-7770
- Seiko Instruments GmbH : TEL 49-6102-297-122

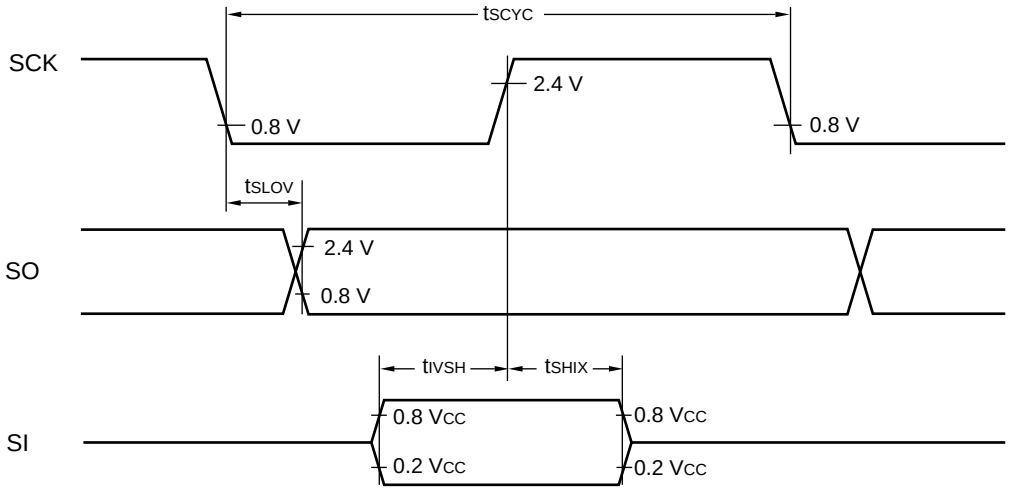
(6) Serial I/O Timing

(V_{CC} = +5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

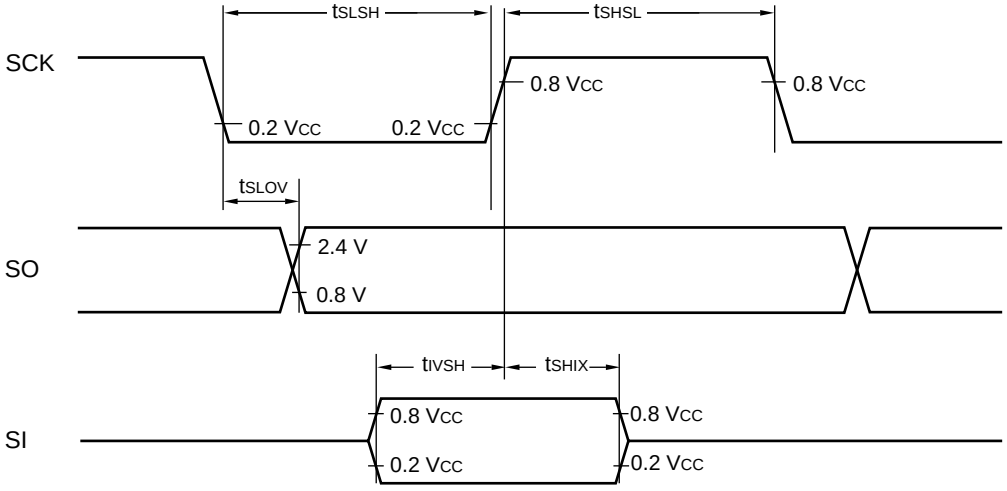
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		200	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		200	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		200	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		200	—	ns	

* : For information on t_{inst}, see “ (4) Instruction Cycle.”

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

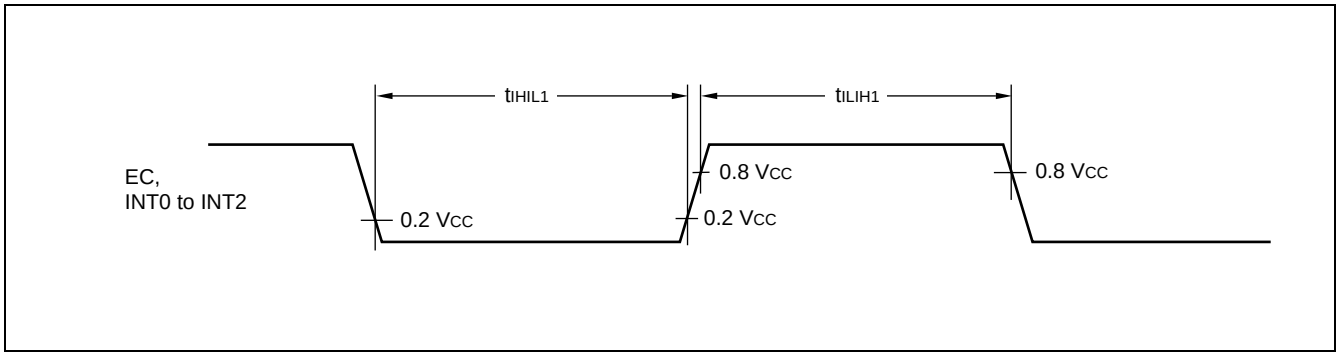


(7) Peripheral Input Timing

(V_{CC} = +5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” level pulse width 1	t_{ILIH1}	EC, INT0 to INT2	—	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 1	t_{IHIL1}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “ (4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = +3.5 V to +6.0 V, F_{CH} = 3 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

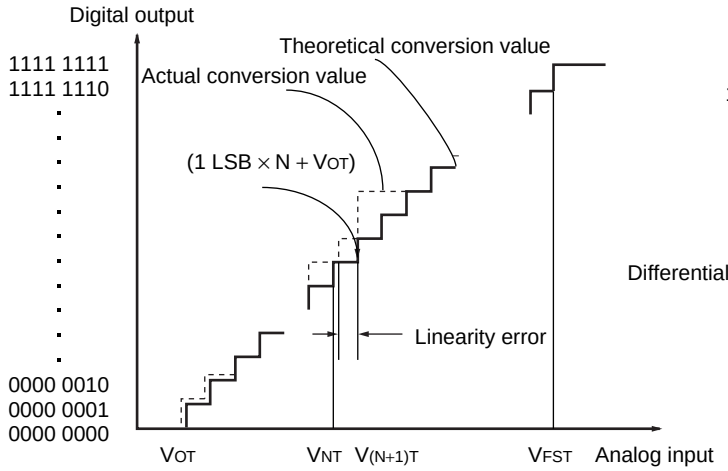
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	AVR = AV_{CC} = 5.0 V	—	—	8	bit	
Total error			AVR = AV_{CC}	—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.0 LSB	mV	1LSB = AVR/256
Full-scale transition voltage	V_{FST}			AVR – 3.0 LSB	AVR – 1.5 LSB	AVR	mV	
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time			—	—	44 t_{inst}*	—	µs	
Sense mode conversion time				—	12 t_{inst}*	—	µs	
Analog port input current	I_{AIN}	AN0 to AN3		—	—	10	µA	
Analog input voltage	—			0	—	AVR	V	
Reference voltage	—	AVR		2.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = AV_{CC} = 5.0 V, when A/D conversion is operating	—	100	300	µA	
	I_{RH}		AVR = AV_{CC} = 5.0 V, when A/D conversion is not operating	—	—	1	µA	

* : For information on t_{inst}, see “ (4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable by the A/D converter.
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.
- Linearity error (unit : LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit : LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

- Total error (unit : LSB)
  The difference between theoretical and actual conversion values



$$1\ \text{LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 1\ \text{LSB})}{1\ \text{LSB}}$$

7. Notes on Using A/D Converter

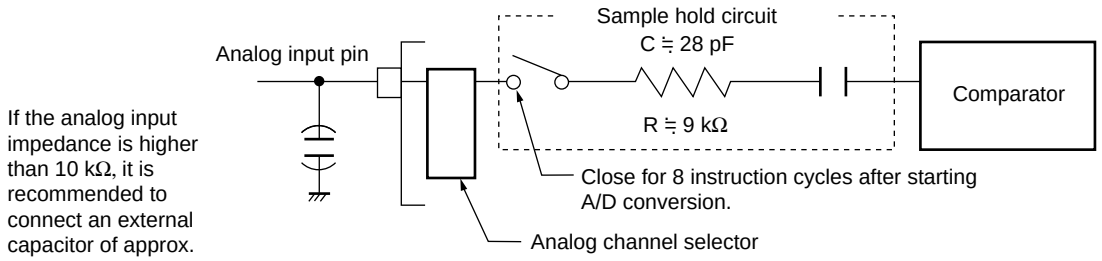
- **Input impedance of the analog input pins**

The A/D converter used for the MB89130/130A series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after starting A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ) .

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of approx. 0.1 µF for the analog input pin.

- **Analog Input Equivalent Circuit**



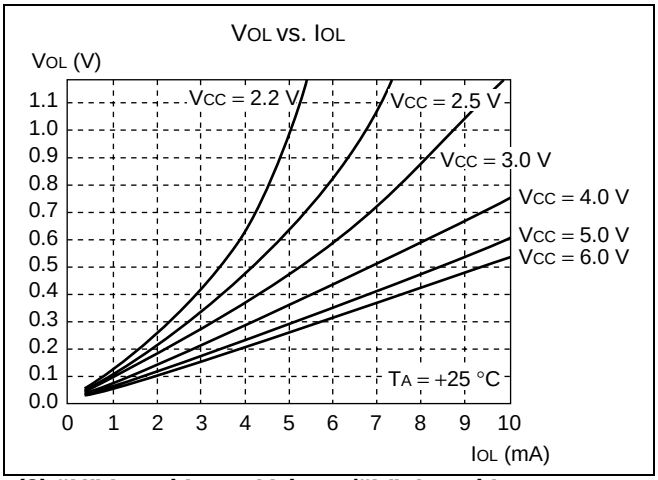
If the analog input impedance is higher than 10 kΩ, it is recommended to connect an external capacitor of approx. 0.1 µF.

- **Error**

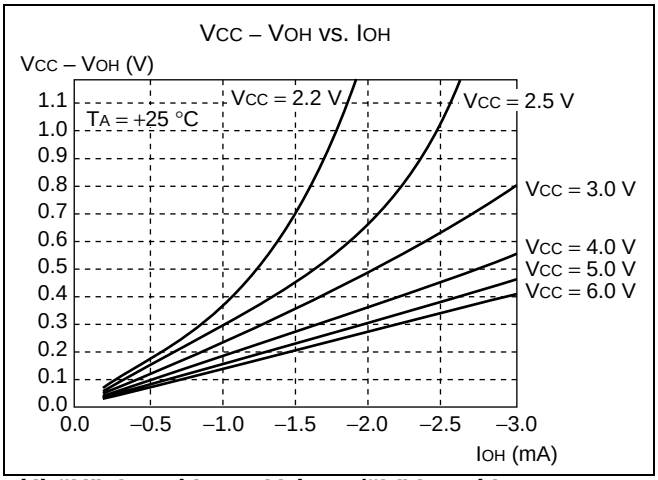
The smaller the | AVR – AV_{SS} |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

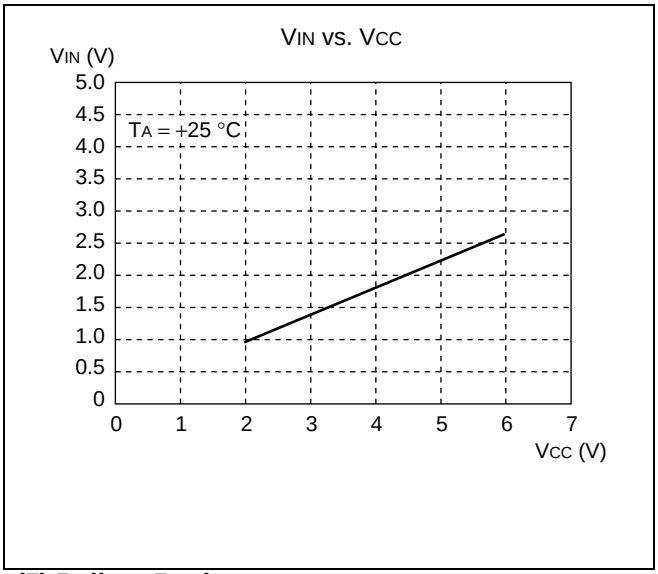
(1) “L” Level Output Voltage



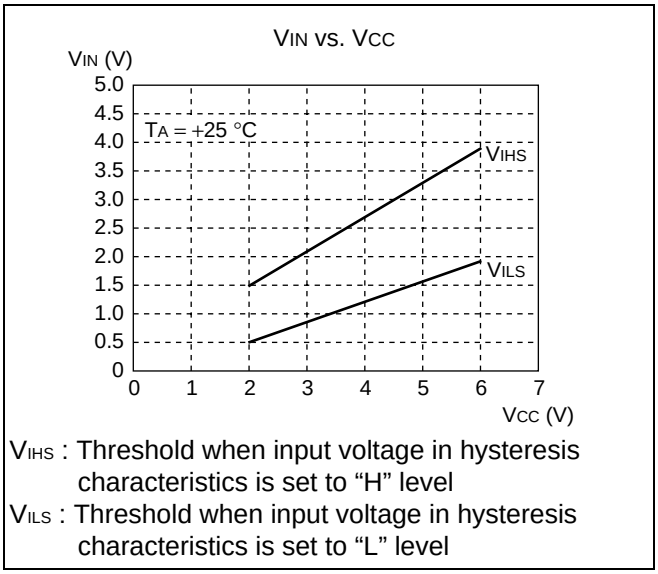
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



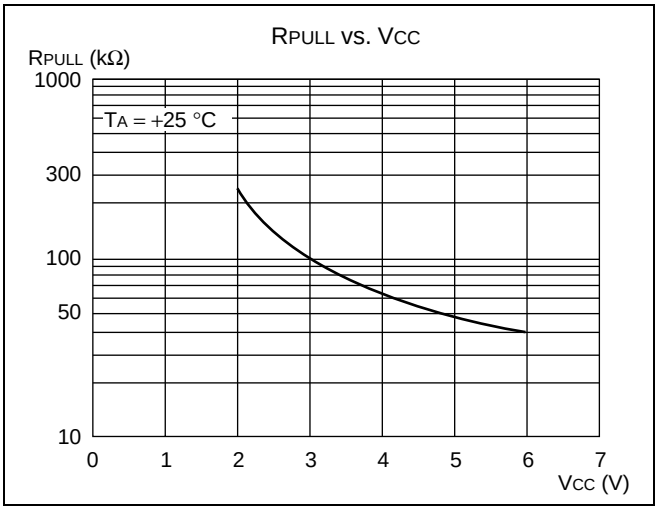
(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)



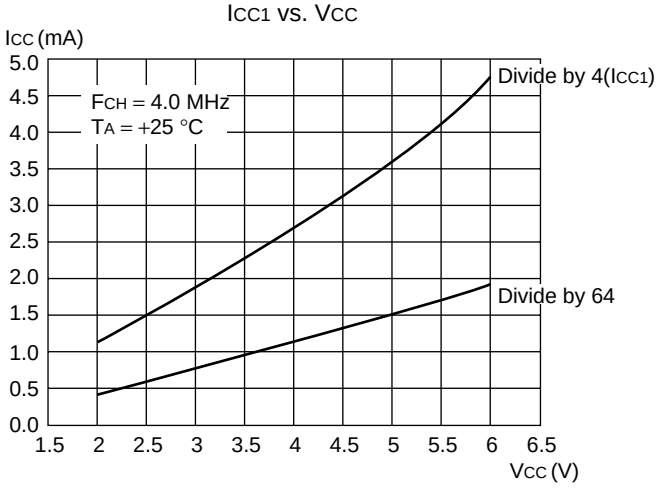
V_{IHS} : Threshold when input voltage in hysteresis characteristics is set to “H” level

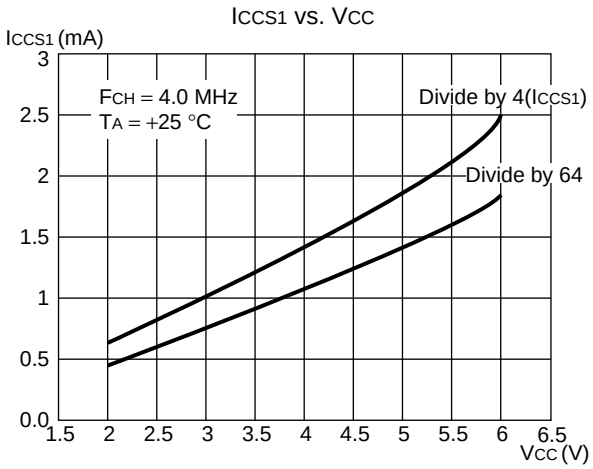
V_{ILS} : Threshold when input voltage in hysteresis characteristics is set to “L” level

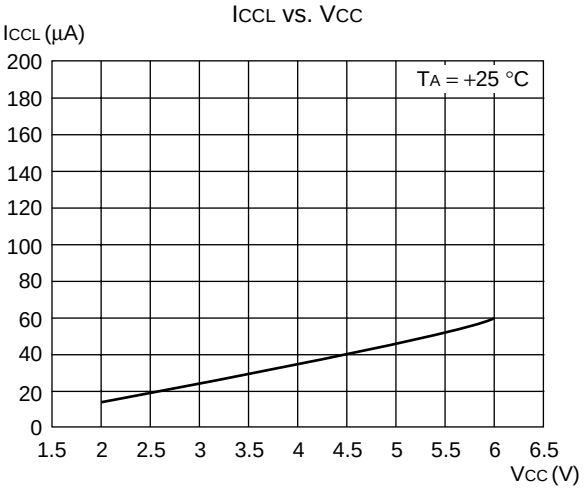
(5) Pull-up Resistance

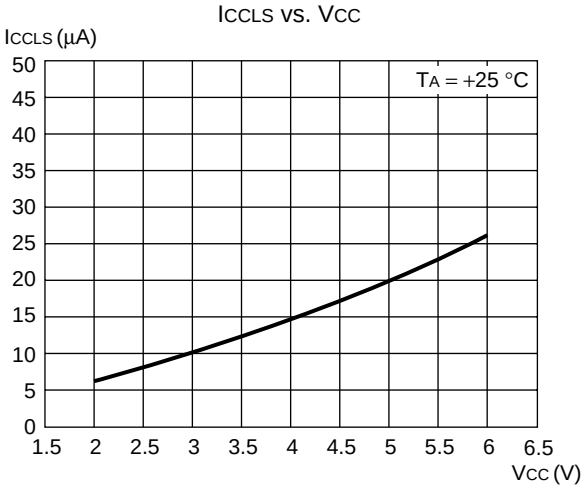


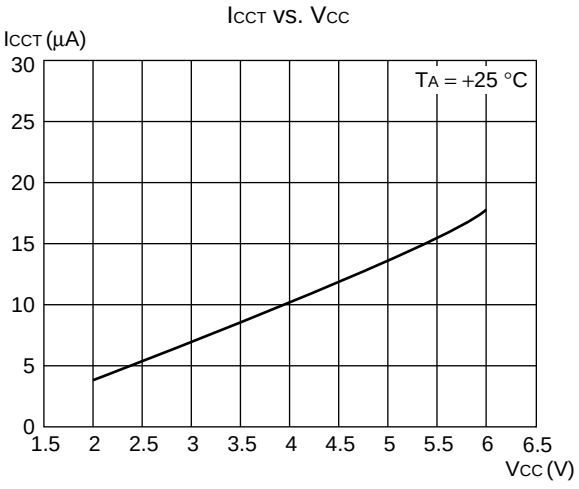
(6) Power Supply Current (External Clock)

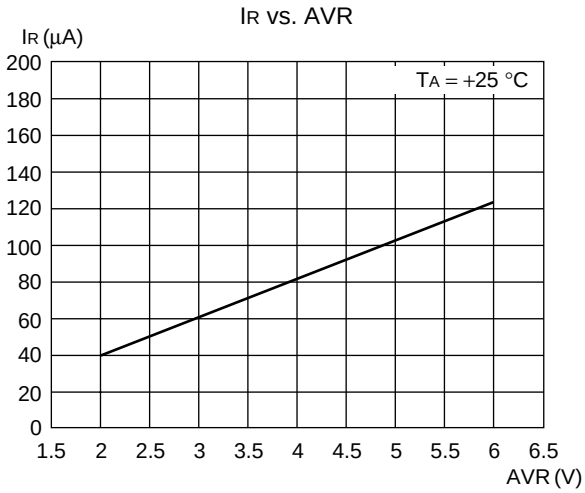












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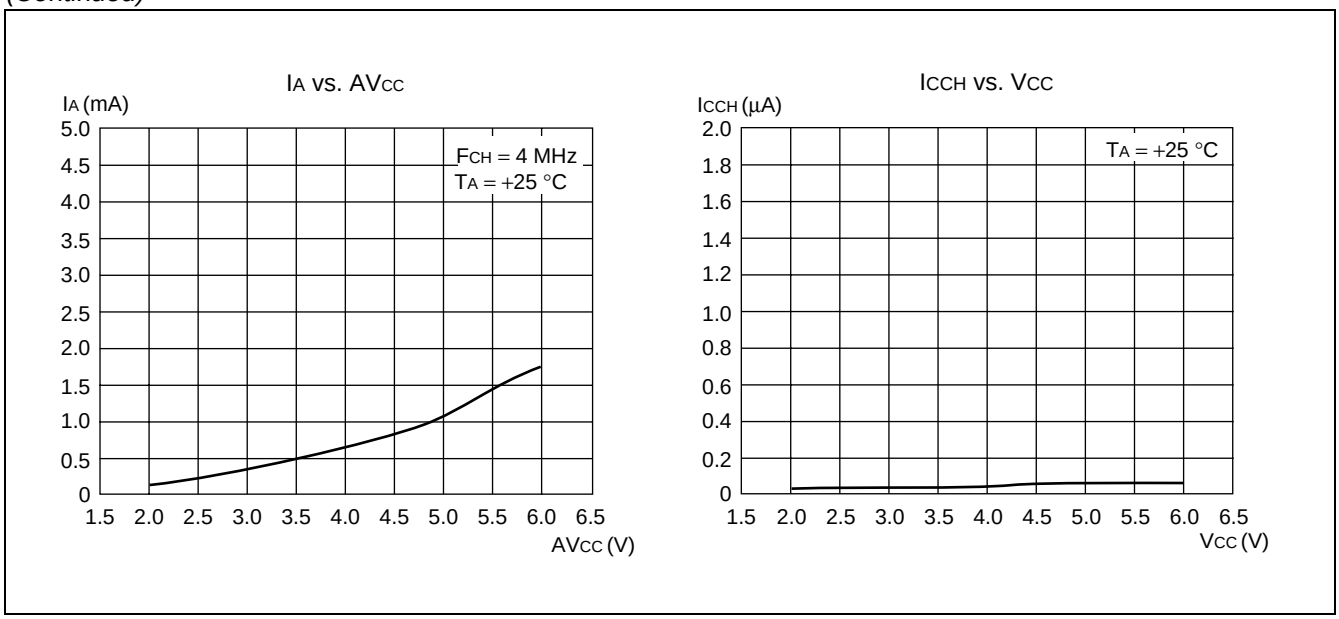

IA vs. AVCC
IA (mA)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
FCH = 4 MHz
TA = +25 °C
1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5
AVCC (V)
ICCH vs. VCC
ICCH (µA)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
TA = +25 °C
1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5
VCC (V)

■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:
- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:
- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

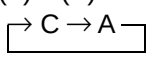
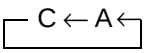
OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Note: During byte transfer to A, T ← A is restricted to low bytes.
Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89131	MB89133A MB89135A	MB89P131 MB89P133A
	Specifying procedure	**Specify when ordering masking**	**Specify when ordering masking**	**Specify when ordering masking**
1	Pull-up resistors •P00 to P07, P10 to P17, •P30 to P37, P40 to P43	Selectable by pin (P40 to P43 must be fixed to no pull-up resistor option when an A/D converter is used.)	Selectable by pin (P40 to P43 must be fixed to no pull-up resistor option when an A/D converter is used.)	Selectable by pin (P40 to P43 must be fixed to no pull-up resistor option when an A/D converter is used.)
2	Power-on reset •Power-on reset provided •No power-on reset	Selectable	Selectable	Selectable
3	Selection of oscillation stabilization time •The oscillation stabilization time initial value is selectable from 4 types given below. 0 : Oscillation stabilization $2^2/F_{CH}$ 1 : Oscillation stabilization $2^{12}/F_{CH}$ 2 : Oscillation stabilization $2^{16}/F_{CH}$ 3 : Oscillation stabilization $2^{18}/F_{CH}$	Selectable	Selectable	Selectable
4	Reset pin output •Reset output enabled •Reset output disabled	Selectable	Selectable	Selectable
5	Clock mode selection •Single-clock mode •Dual-clock mode	Selectable	Selectable	Selectable
6	Selection of oscillation circuit type •Crystal or ceramic oscillation type •External clock input type	Selectable	Selectable	Not required*1
7	Peripheral control clock output function*2 •Not used •Used	Selectable	Not required*3	Not required*3

*1 : Both external clock and oscillation resonator can be used on the OTPROM product.

*2 : “Used” must be selected when P33 (39 pin) is used as SCO for the peripheral control clock output.

*3 : The peripheral control clock output function can be used only by software.

No.	Part number	MB89P135A	MB89PV130A
	Specifying procedure	Set with EPROM programmer	Setting not possible
1	Pull-up resistors •P00 to P07, P10 to P17, •P30 to P37, P40 to P43	Selectable by pin (P40 to P43 must be fixed to no pull-up resistor option.)	All pins fixed to no pull-up resistor option
2	Power-on reset •Power-on reset provided •No power-on reset	Selectable	Power-on reset provided
3	Selection of oscillation stabilization wait time •The oscillation stabilization time initial value is selectable from 4 types given below. 0 : Oscillation stabilization $2^2/F_{CH}$ 1 : Oscillation stabilization $2^{12}/F_{CH}$ 2 : Oscillation stabilization $2^{16}/F_{CH}$ 3 : Oscillation stabilization $2^{18}/F_{CH}$	Selectable	Oscillation stabilization $2^{18}/F_{CH}$
4	Reset pin output •Reset output enabled •Reset output disabled	Selectable	Reset output enabled
5	Selection of clock mode selection •Single-clock mode •Dual-clock mode	Selectable	Dual-clock mode
6	Selection of oscillation circuit type •Crystal or ceramic oscillation type •External clock input type	Not required*1	Not required*1
7	Peripheral control clock output function*2 •Not used •Used	Not required*3	Not required*3

*1 : Both external clock and oscillation resonator can be used.

*2 : “Used” must be selected when P33 (39 pin) is used as SCO for the peripheral control clock output.

*3 : The peripheral control clock output function can be used only by software.

■ MB89P131/P133A STANDARD OPTIONS

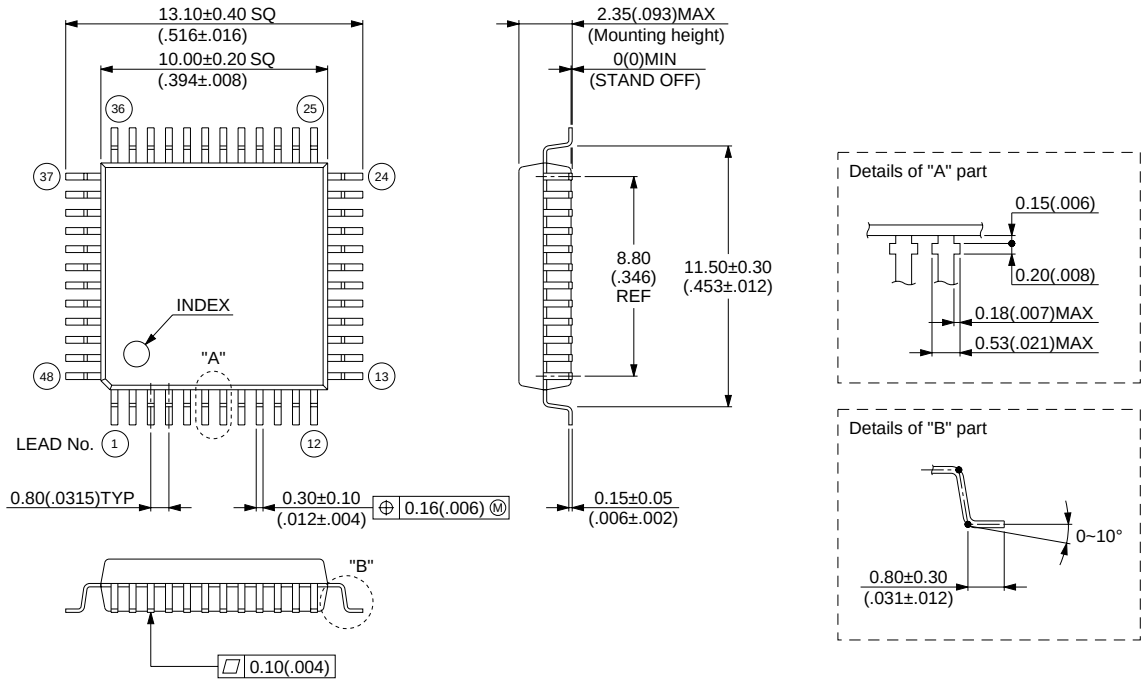
No.	Product option	MB89P131-101	MB89P133A-201
1	Pull-up resistor	Not provided for any port	Not provided for any port
2	Power-on reset	Provided	Provided
3	Selection of oscillation stabilization time	2 : Oscillation stabilization $2^{16}/F_{CH}$	2 : Oscillation stabilization $2^{16}/F_{CH}$
4	Reset pin output	Enabled	Disabled
5	Selection of clock mode	Dual-clock mode	Dual-clock mode

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89131PFM MB89133APFM MB89135APFM MB89P131PFM-101 MB89P133APFM-201 MB89P135APFM	48-pin Plastic QFP (FPT-48P-M13)	
MB89133AP MB89P133AP-201	48-pin Plastic SH-DIP (DIP-48P-M01)	
MB89PV130ACF-ES	48-pin Ceramic MQFP (MQP-48C-P01)	

■ PACKAGE DIMENSION

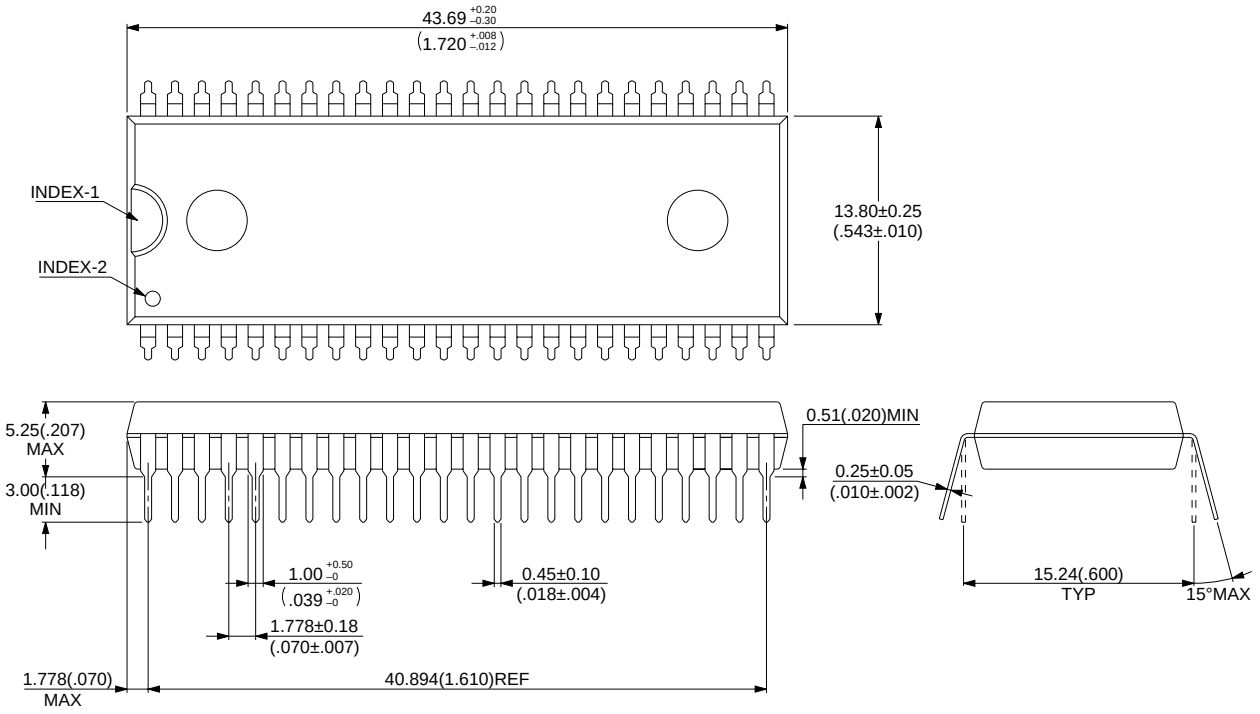
48-pin Plastic QFP
(FPT-48P-M13)



Dimensions in mm (inches)

(Continued)

48-pin Plastic SH-DIP
(DIP-48P-M01)

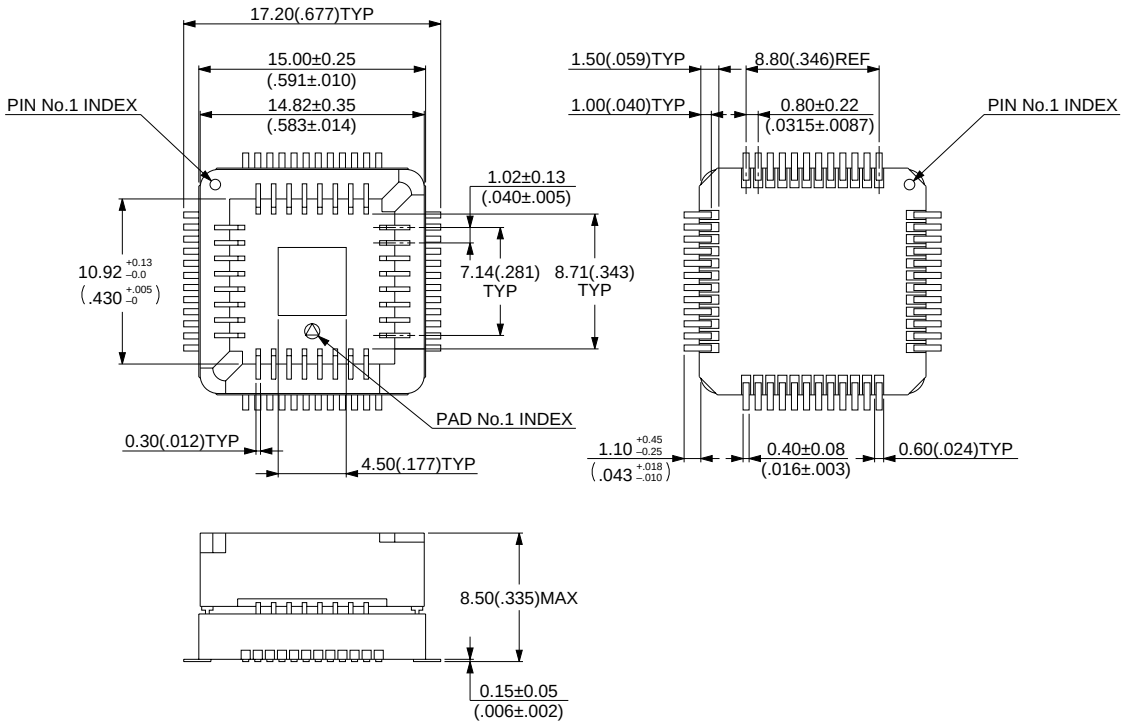


Dimensions in mm (inches)

(Continued)

(Continued)

48-pin Ceramic MQFP
(MQP-48C-P01)



Dimensions in mm (inches)

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