

## Document Title

256Kx8 bit Low Power and Low Voltage CMOS Static RAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	September 30, 1997	Preliminary

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# KM68S2000 Family

## 256Kx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology : TFT
- Organization : 256Kx8
- Power Supply Voltage  
KM68S2000 Family : 2.3~3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-TSOP1-0820F, 32-TSOP1-0813.4F

### GENERAL DESCRIPTION

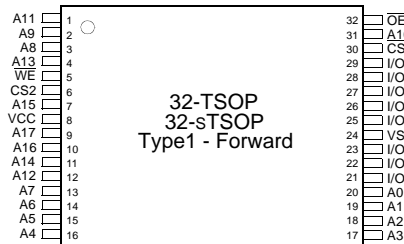
The KM68S2000 families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and wide voltage operation for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
KM68S2000L-L	Commercial(0~70°C)	2.3~2.7V	120 <sup>1)</sup> /150	10μA	25mA	32-TSOP1-F 32-sTSOP1-F
		2.7~3.3V			35mA	
KM68S2000LI-L	Industrial(-40~85°C)	2.3~2.7V		15μA	25mA	
		2.7~3.3V			35mA	

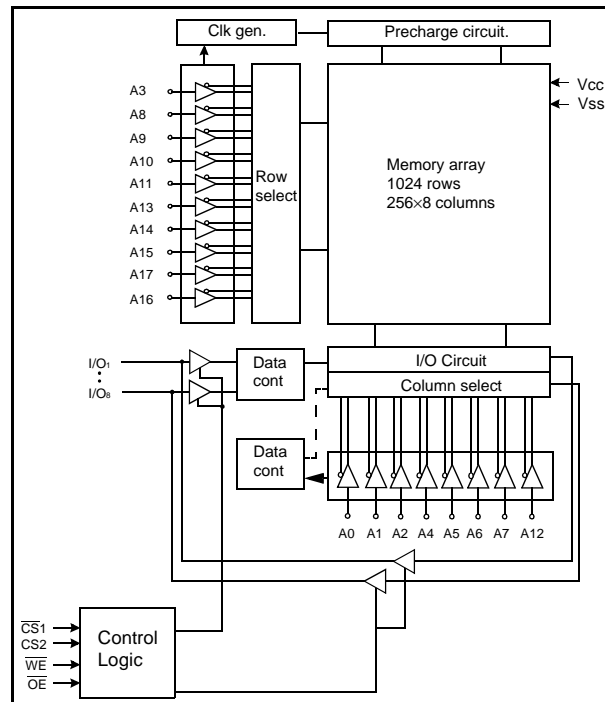
1. The parameter is measured with 30pF test load.

### PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS1}, \overline{CS2}$	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A0~A17	Address Inputs	N.C.	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM68S2000LT-12L	32-TSOP F, 120ns, 2.3~3.3V, LL	KM68S2000LTI-12L	32-TSOP F, 120ns, 2.3~3.3V, LL
KM68S2000LT-15L	32-TSOP F, 150ns, 2.3~3.3V, LL	KM68S2000LTI-15L	32-TSOP F, 150ns, 2.3~3.3V, LL
KM68S2000LTG-12L	32-sTSOP F, 120ns, 2.3~3.3V, LL	KM68S2000LTGI-12L	32-sTSOP F, 120ns, 2.3~3.3V, LL
KM68S2000LTG-15L	32-sTSOP F, 150ns, 2.3~3.3V, LL	KM68S2000LTGI-15L	32-sTSOP F, 150ns, 2.3~3.3V, LL

Note : LL - Low Low Standby Current

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	1	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM68S2000L
		-40 to 85	°C	KM68S2000LI
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	KM68S2000 Family	2.3	2.5/3.0	3.3	V
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.3~2.7V	2.0	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
		2.7~3.3V	2.2	-		
Input low voltage	V <sub>IL</sub>	KM68S2000 Family	-0.3 <sup>3)</sup>	-	0.6	

Note:

- Commercial Product : T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product : T<sub>A</sub>=-40 to 85°C, otherwise specified
- Overshoot : V<sub>CC</sub>+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

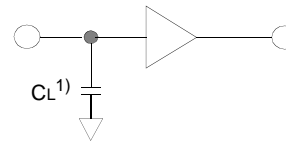
Item	Symbol	Test Conditions	Min	Typ	Max	Unit		
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA		
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA		
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read	2.3~2.7V	-	-	2	mA	
			2.7~3.3V	-	-	5	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA $\overline{CS}_1 \leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	2.3~2.7V	Read	-	-	3	mA
				Write	-	-	10	
			2.7~3.3V	Read	-	-	5	mA
				Write	-	-	15	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	2.3~2.7V	-	-	25	mA	
			2.7~3.3V	-	-	35	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =0.5mA at 2.3~2.7V I <sub>OL</sub> =2.1mA at 2.7~3.3V	-	-	0.4	V		
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.5mA at 2.3~2.7V	2.0	-	-	V		
		I <sub>OH</sub> =-1.0mA at 2.7~3.3V	2.4	-	-	V		
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.3	mA		
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CS}_1 \geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0-V <sub>CC</sub>	-	-	10 <sup>1)</sup>	μA		

- Industrial product=15μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.5V  
 Output load (See right) :  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS ( $V_{CC}=2.3\sim 3.3\text{V}$ , Commercial products: $T_A=0$ to $70^\circ\text{C}$ , Industrial products: $T_A=-40$ to $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins				Units
			120ns <sup>1)</sup>		150ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	120	-	150	-	ns
	Address access time	t <sub>AA</sub>	-	120	-	150	ns
	Chip select to output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	120	-	150	ns
	Output enable to valid output	t <sub>OE</sub>	-	60	-	75	ns
	Chip select to low-Z output	t <sub>LZ</sub>	20	-	20	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	20	-	20	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	-	35	0	40	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	-	35	0	40	ns
	Output hold from address change	t <sub>OH</sub>	15	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	120	-	150	-	ns
	Chip select to end of write	t <sub>CW1</sub> , t <sub>CW2</sub>	100	-	120	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	100	-	120	-	ns
	Write pulse width	t <sub>WP</sub>	80	-	100	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	30	0	40	ns
	Data to write time overlap	t <sub>DW</sub>	50	-	60	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns

1. The parameter is measured with 30pF test load.

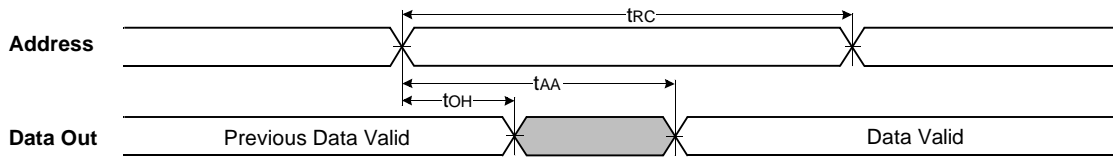
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^1)$	2.0	-	3.3	V
Data retention current	I <sub>DR</sub>	$V_{CC}=2.0\text{V}$ , $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$	-	-	10	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

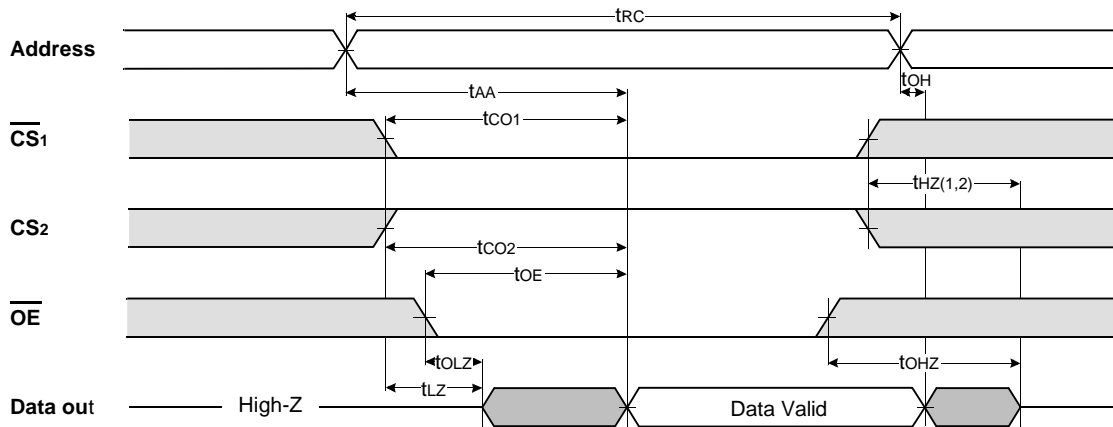
1.  $CS_1 \geq V_{CC}-0.2\text{V}$ ,  $CS_2 \geq V_{CC}-0.2\text{V}$  ( $CS_1$  Controlled) or  $CS_2 \leq 0.2\text{V}$  ( $CS_2$  Controlled)

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



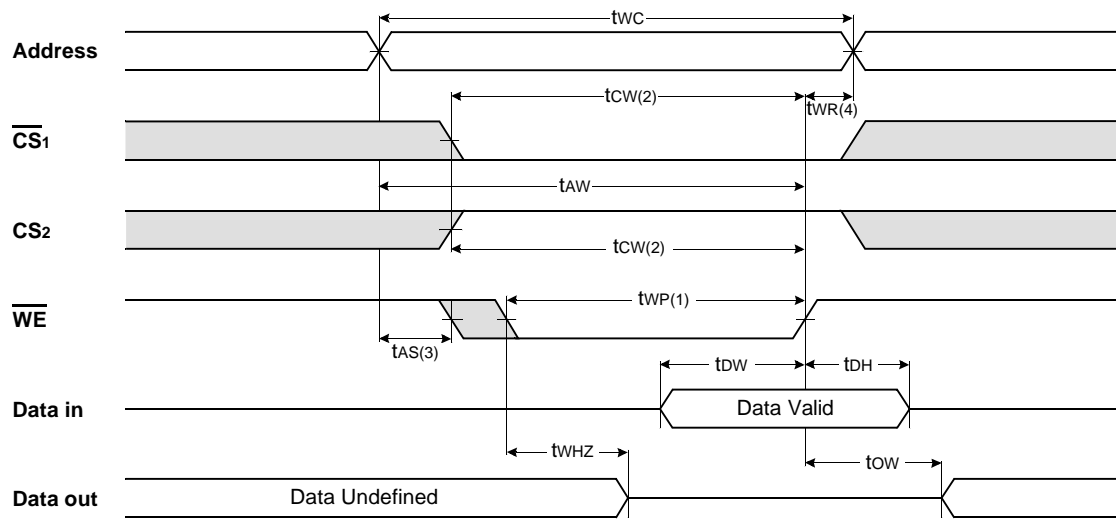
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



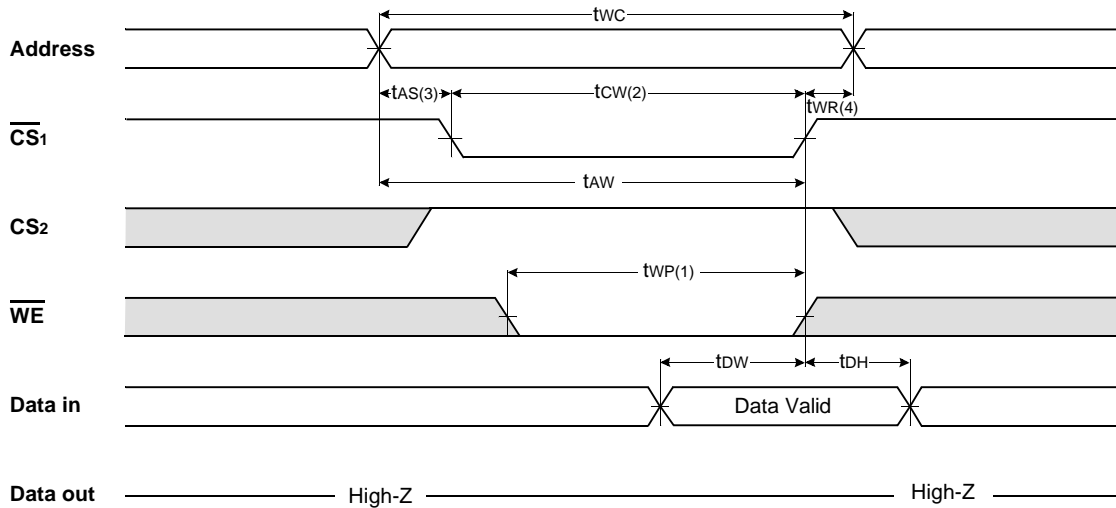
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

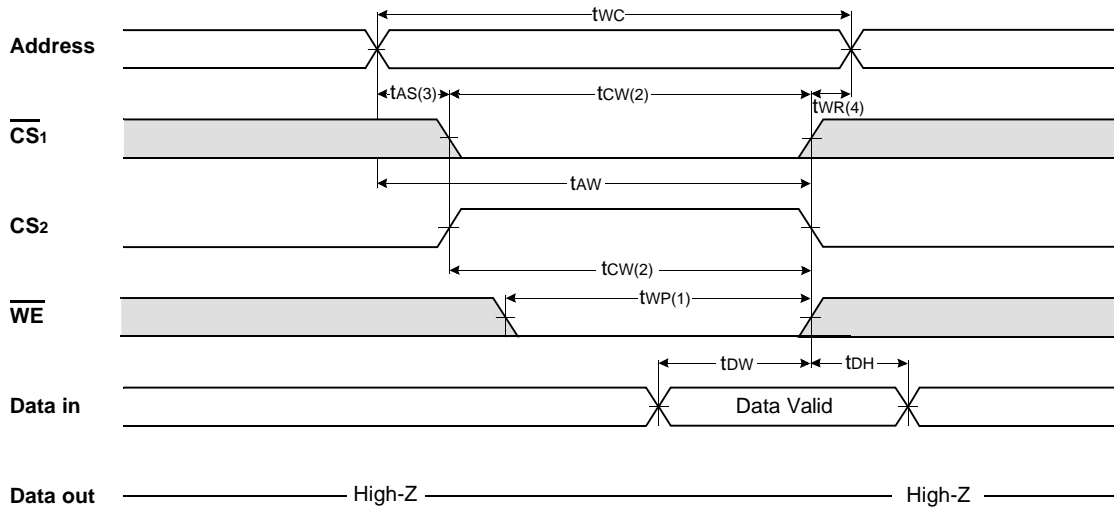
## TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}_1$ Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}_1$ Controlled)

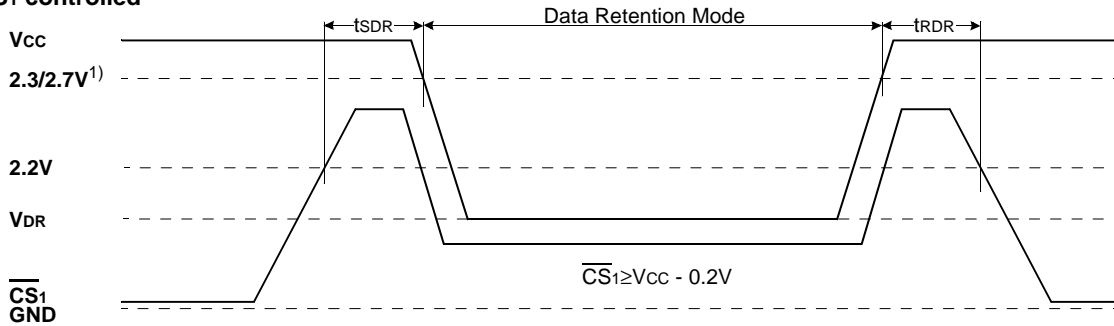


### NOTES (WRITE CYCLE)

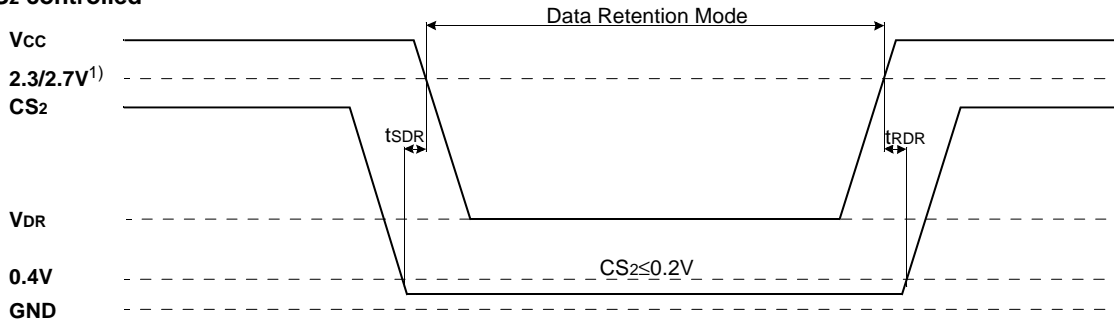
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low : A write ends at the earliest transition among  $\overline{CS}_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR(1)}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR(2)}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS}_1$ controlled



### $CS_2$ controlled



1. 2.7V for 2.7~3.3V operation, 2.3V for 2.3~2.7V operation.



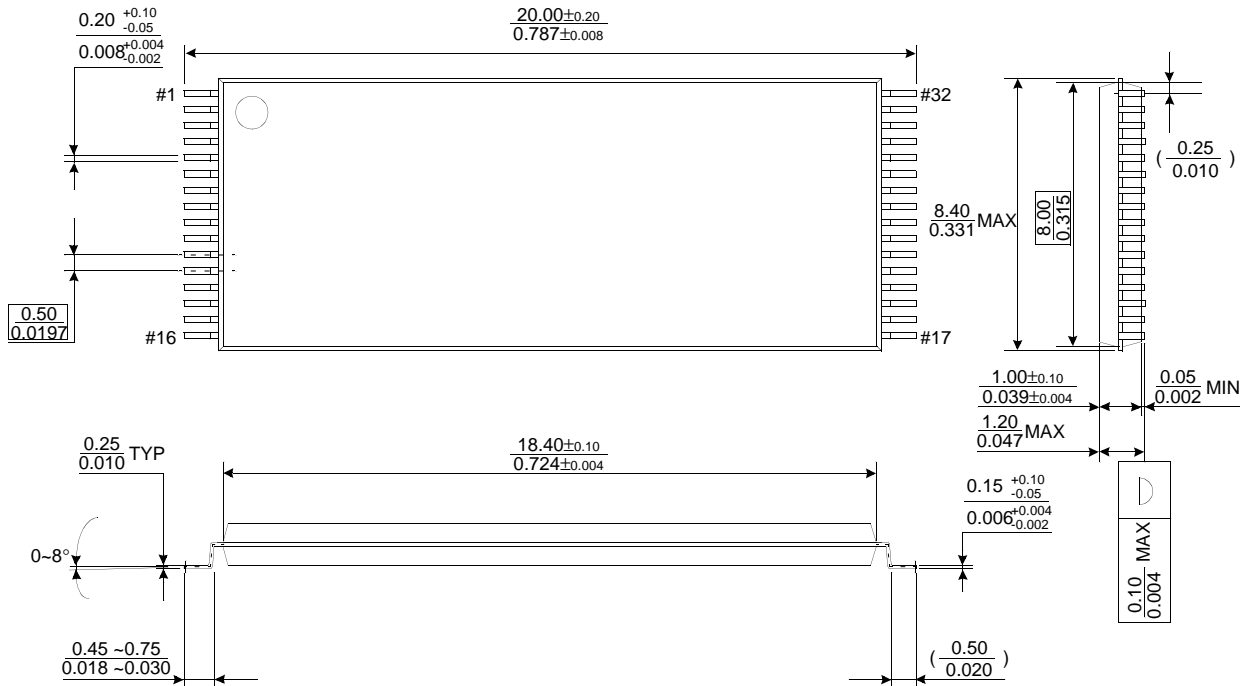
# KM68S2000 Family

**Preliminary  
CMOS SRAM**

## PACKAGE DIMENSIONS

Units : millimeter(Inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



### 32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

