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1.1 CHOOSING AN ARRAY

Four factors determine gate array size:

- gate count
- pin count and type
- package availability
- power pads and locations

All of these factors go into the process of evaluating and choosing an ASIC. Figure 1–1 shows the steps in the evaluation process.

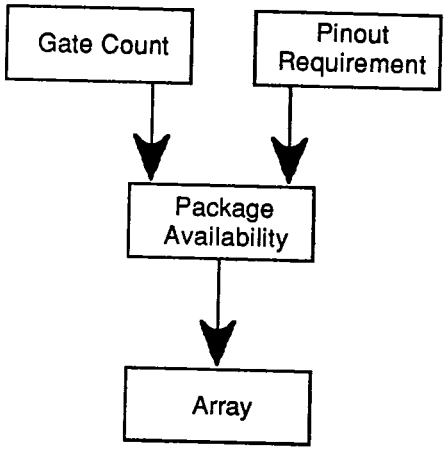


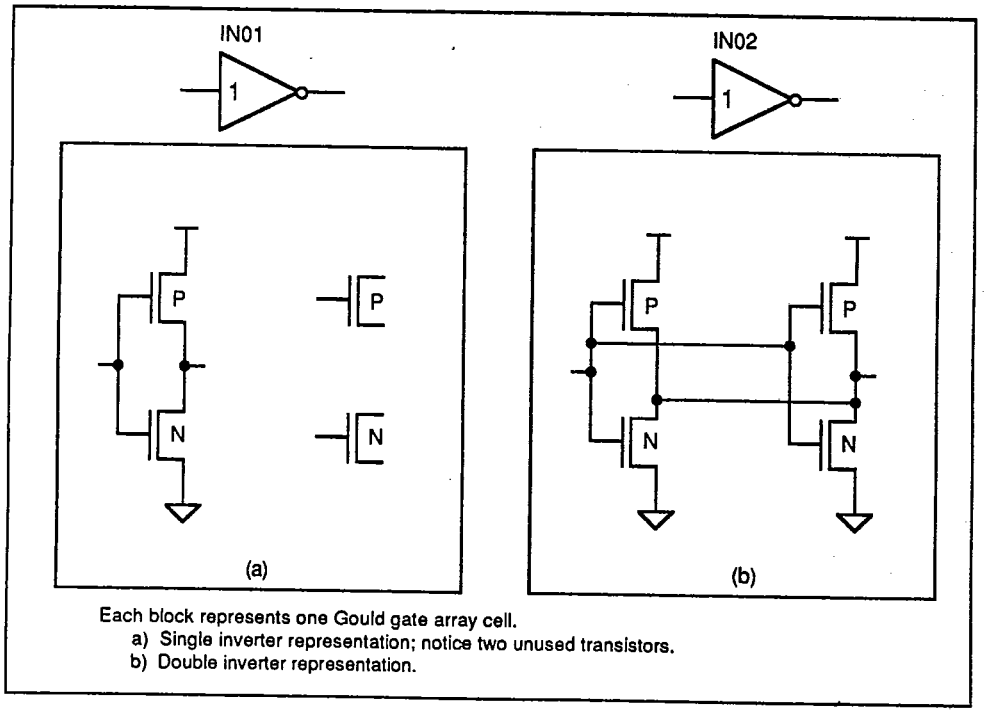
Figure 1–1. ASIC Evaluation Flowchart

1.1.1 Determining Gate Count

Gate counts are usually given in terms of equivalent gates. "Equivalent gate" refers to a 2-input NAND gate; it is comprised of two transistor pairs or four transistors. Use this definition to determine the equivalent gate count of a component and estimate the gate count of a complex circuit.

For gate arrays, the gate count is defined as the number of core cells (each core cell having four transistors) occupied by a component.

Figure 1–2 shows two inverters from the Gould library, an IN01 (inverter) and IN02 (double strength inverter). These components each use a full core cell despite the fact that the single inverter uses two transisters and the double inverter uses four. Therefore when determining the gate count for a gate array quote, refer to the Gould gate array data sheets for the component gate counts. The gate count is estimated using the gate array datasheet, a list of 7400 series and 4000 series equivalent gate counts and gate count worksheet examples found in the Application Note "Determining Gate Count for ASICs."



Each block represents one Gould gate array cell.
a) Single inverter representation; notice two unused transistors.
b) Double inverter representation.

Figure 1–2. Single and Double Strength Inverter Representation

It is a good design practice to increase the gate count by 5 percent to allow for extra drive buffers often needed in CMOS gate array implementations.

1.1.2 Pin Requirements

Next determine the number of pins required. The total pinout is the sum of the pins for

- inputs
- outputs
- bi-directional (I/Os)
- power
- ground

Because the power-bus sizes are fixed for gate arrays, additional Vdd and Vss pins may be required to reduce the noise associated with multiple outputs switching. Table 1–1 contains a summary of the number of signal and fixed power pins available in the GC series family.

Table 1–1
GC CMOS GATE ARRAY FAMILY

GC Series Gate Array

ARRAY NAME	TOTAL GATES	USEABLE GATES	SOG USEABLE GATES	Programmable TAB PADS*	Programmable WIRE BOND PADS	POWER TABS
GC40K	38976	13735	23386	268	152	12
GC30K	30000	11760	18000	234	140	12
GC25K	25344	10348	15206	212	130	12
GC20K	19840	7721	11904	196	116	12
GC15K	15000	5790	9000	168	100	12
GC10K	10320	3963	6192	136	84	12
GC7K	7488	3283	4493	116	68	12
GC5K	5280	2083	3168	98	56	12
GC3K	3128	994	1877	76	38	12

*Router technology under development for sea of gate (SOG) architecture will increase the number of useable gates to the value noted here. Please contact your Gould Semicondutor Division representative for current availability.

Once the gate count and pinout is known, a proper array can be chosen using the information provided in Table 1–1. Table 1–1 also lists the actual number of gates and the total number of pads available on each Gould array. Also listed are the actual numbers useable for each array. This is important, because gate arrays come in fixed gate counts (3963, 5790 etc.), and the presence of only a few extra gates can mean that a larger array must be used.

Any pad that is not a preassigned power pad is a programmable pad. A programmable pad can be one of the following: input buffer, output buffer, bidirectional buffer, Vdd pad, Vss pad, or a crystal oscillator. When assigning Vdd and Vss power pads, the option of using a fixed pad location is always taken first. Only if all fixed power pad locations are used up should the programmable pads listed in Table 1–1 be used for additional Vdd and Vss pads.

The GC series Arrays have a flexible bond-pad structure around the periphery that can accommodate either wire bonding or high pin count tape-automated bonding (TAB). TAB increases the I/O count without increasing chip size.

Changing a circuit to eliminate a few gates can mean a smaller array and a substantial savings. For example, when implementing a circuit on a board using standard 7400 parts, unused functions such as set, reset, or load are typically handled by tying the appropriate control pin high or low. These redundant functions should be removed in the gate array logic, thus reducing gate count.

1.1.3 Package Availability

Next step find a package for the chosen array. Each array has a different die size; each package type has a cavity that fits a range of die sizes. Hence not all arrays will fit all packages. After you have determined gate and pin count, select a package type from Table 1–2.

Table 1–2
Package Availability

A. Plastic Packages

LEADS	ARRAY SIZE								
	GC3K	GC5K	GC7.5K	GC10K	GC15K	GC20K	GC25K	GC30K	GC40K
DIPS									
8	√								
14	√								
16	√								
18	√								
20	√								
22	√	√	√	√					
24	√	√	√	√	√	√			
28	√	√	√	√	√	√	√		
40	√	√	√	√	√	√	√		
48		√	√	√	√	√	√		
SOIC									
16	√								
28	√	√	√						
Chip Carriers									
28	√	√	√	√	√				
44	√	√	√	√	√	√	√	√	√
68			√	√	√	√	√	√	√
84					√	√	√	√	√
PPGA									
68	√	√	√	√	√	√	√	√	
84	√	√	√	√	√	√	√	√	
100			√	√	√	√	√	√	
108				√	√	√	√	√	√
120					√	√	√	√	√
132						√	√	√	√
144								√	√

Consult factory for package types not shown

Table 1–2
Package Availability
(continued)

B. Ceramic Packages

	ARRAY SIZE								
LEADS	GC3K	GC5K	GC7.5K	GC10K	GC15K	GC20K	GC25K	GC30K	GC40K
DIPS									
14	X								
16	X								
18	X								
22	√	√	√	√					
24	√	√	√	√	√	√	√	√	
28	√	√	√	√	√	√	√	√	
40	√	√	√	√	√	√	√	√	
48	√	√	√	√	√	√	√	√	
Chip Carriers									
24	√	√	√						
28	√	√	√	√					
40			√	√	√				
44			√	√	√				
48			√	√	√	√	√	√	
52			√	√	√				
68					√	√	√	√	√
84							√	√	√
CPGA									
68					√	√	√	√	
84						√	√	√	√
100					√	√	√	√	
120								√	√

Consult factory for package types not shown
X = prototyping use only

1.1.4 Power Pads and Locations

Every Gate Array integrated circuit has a different operating frequency, a different number of input and output buffers, and a different number of transistors being used. The power pad rules described on this section are intended to protect a Gate Array circuit from logic failure caused by insufficient power distribution or excessive switching noise. The number and placement positions of power pads can be determined by three steps:

1. Determine the minimum number of power pads.
2. Determine the power pad locations.
3. Place input, output and I/O buffers.

Power pads are defined as:

Vdd	positive supply power pad
Vssp	ground supply for output buffers on the perimeter of the die
Vssc	ground supply for the input buffers and internal core cells

1.1.4.1 Determining the Minimum Number of Power Pads

Three considerations must be taken into account when determining the number of power pads needed.

Output Buffer Consideration.

Output buffers can create significant current spikes (up to 10 times the rated DC current of the buffer) while switching. To ensure that these current spikes do not impair the operation of the input level translators and internal logic, follow the equivalent output equation given below to determine the total equivalent output in your circuit. Use equations (1) and (2) to determine the number of power pads required for output buffers.

Equivalent output = EO

$$EO = (0.16 * N0) + (0.25 * N1) + (0.5 * N2) + N4 + (3 * N8) + (2 * N8SR)$$

where

N0 = # of 0.65 mA outputs,	(OBxx0 and IOxx0 macros)
N1 = # of 1.0 mA outputs,	(OBxx1 and IOxx1 macros)
N2 = # of 2.0 mA outputs,	(OBxx2 and IOxx2 macros)
N4 = # of 4.0 mA outputs,	(OBxx3 and IOxx3 macros)
N8 = # of 8.0 mA outputs,	(OBxx5 and IOxx5 macros)
N8SR = # of 8.0 mA outputs, (controlled slew rate outputs)	(OBxx5 and IOxx5 macros)

(1) Vdd required $= \frac{EO}{16}$

(2) Vssp required $= \frac{EO}{16}$

The controlled slew rate output buffer has been designed to reduce AC transients at switching time and be able to supply 8.0mA current at DC condition. The equivalent output equation weights output buffers based on their magnitude of switching current.

Input Buffer Consideration

Input buffers such as Schmitt trigger and TTL draw DC current. They also generate current spikes when switching. The voltage level of internal power buses will rise or drop due to these DC and AC currents. Equations (3) and (4) determine the number of power pads required for input buffers.

$$(3) \quad \text{Vdd required} = \frac{\#\text{ of IB}}{20}$$

$$(4) \quad \text{Vssp required} = \frac{\#\text{ of IB}}{20}$$

I/O buffers need to be treated in *both* output buffer consideration and input buffer consideration.

Core Transistors Consideration

Power dissipation in the core of an array depends on the number of gates being used and their operating frequency. Equations (5) and (6) determine the number of power pads needed for core dynamic current.

$$(5) \quad \text{Vdd required} = \frac{\text{Vdd} * f * \#\text{gate} * \text{FO} * 0.11 * 1.73}{20}$$

$$(6) \quad \text{Vssc required} = \frac{\text{Vdd} * f * \#\text{gate} * \text{FO} * 0.11 * 1.73}{20}$$

FO = average fanout
Vdd = maximum supply voltage
f = maximum operating frequency in MHz
#gate = maximum # of gates switching at a given time in thousand.
Interconnect factor = 1.73

Example

FO = 1.5pF Vdd 5.5V f = 10MHz # gate = 4K

$$\text{Vdd required} = \text{Vssc required} = \frac{5.5 * 10 * 4 * 1.5 * 0.11 * 1.73}{20} = 3.13 \cong 4$$

Calculate the Number of Pads Needed

Use the following equation to calculate the number of power pads needed in your circuit.

# of Vdd = maximum of result [(1), (3), (5)]
# of Vssp = result of (2)
# of Vssc = maximum of result [(4), (6)]

The GC series Gate Array family uses a split bus structure to distribute power from pads to input buffers, output buffers and core transistors. This is why there are different types of power pads to consider. This structure provides isolation of output switching noise from internal core circuitry.

Also, every Vss package pin can be double bonded to a Vssp pad and an adjacent Vssc pad. Thus the required Vss package pin can be substantially reduced. The following example illustrates the concept discussed in this section.

Example

Considerations:

Output Buffer	Input Buffer	Core Transistors
Vdd required = 4 Vssp required = 4	Vdd required = 3 Vssc required = 3	Vdd required = 1 Vssc required = 1

# of Vdd = Maximum [4, 3, 1] = 4
# of Vssp = 4
# of Vssc = max [3, 1] = 3

If Vssc pads are selected to locate next to Vssp pads, then only four Vss package pins are needed for three Vssc and four Vssp pads. Each Vdd pad will bond to a Vdd package pin, so four Vdd package pins are needed.

1.1.4.2 Determining the Power Pad Locations

Once you have determined the minimum number of Vdd and Vss pads, you must decide the placement of the power pads. Use the corner preassigned fixed pads of the die first for power pad location. When two power pads are required, use the diagonal corner pin pairs (either top left and bottom right or top right and bottom left).For additional power pads when all fixed power pads are used, use the programmable pads in the center of any side of the die.

1.1.4.3 Placing Input, Output and I/O Buffers

The rules to place I/O buffers between power pins are as follow:

First, place the output buffers while not exceeding the maximum of 16 EO between two Vssp pads and two Vdd pads. Table 1–3 shows each type of output buffer and its corresponding EO.

Second, place no more than 20 input buffers between two Vdd pads and two Vssc pads.

Third, keep the following suggestions in mind when placing I/O buffers:

- Place all faster switching and higher current output buffers as close to power pins as possible.
- Place all TTL input buffers away from fast switching and high current output buffers. This will isolate noise sensitive TTL input buffers from switching noise generated by these output buffers.

- Place all additional Vssc and Vssp power pads adjacent to each other. This allows these two power pads to be bonded to the same post of the package. Only one Vss package pin is required to supply power to two Vss pads (Vssc and Vssp). All preassigned, fixed Vss pads are arranged in this nature to achieve this bonding option.

Table 1–3
EO vs Output Drive

Nominal Sink/Source Current	Equivalent output
8mA	3
8mA slew rate controlled OB	2
4mA	1
2mA	0.5
1mA	0.25
.65mA	0.16

Example

Assume a GC10000 circuit with the following outputs:

4	OB015	(conventional 8mA OB)
18	OB815	(slew rate controlled 8mA OB)
8	IO0E3	(4mA IO)
4	OB011	(1mA OB)
33	IB075	(TTL input buffer)

Operating conditions:
max Vdd = 5.5V
frequency = 8MHz
average fanout FO = 3
maximum # of gate switching at a given time = 2K

1. Calculate the number of power pins:

   a. Output buffer considerations:

4	OB015	N8 = 4
18	OB815	N8SR = 18
8	IO0E3	N4 = 8
4	OB011	N1 = 4

   The equivalent output is:

   EO = (0.16 * N0) + (0.25 * N1) + (0.5 * N2) + (3 * N8) +(2 * N8SR)
   EO = (0.16 * 0) + (0.25 * 4) + (0.5 * 0) + 8 + (3 * 4) +(2 * 18)
   EO = 49

   Vdd required $\frac{EO}{16} = \frac{49}{16} = 3.10 \cong 4$

   Vssp required $\frac{EO}{16} = \frac{49}{16} = 3.10 \cong 4$

   b. Input buffer considerations:

33	IB075
8	IO0E3

   Vdd required $\frac{\#\text{ of IB}}{20} = \frac{41}{20} = 2.05 \cong 3$

   Vssc required $\frac{\#\text{ of IB}}{20} = \frac{41}{20} = 2.05 \cong 3$

   c. Core transistor considerations:

   $$Vssc = Vdd = \frac{Vdd * f * \#gate * FO * 0.11 * 1.73}{20}$$

   $$Vdd = \frac{5.5 * 10 * 3 * 0.11 * 1.73}{20} = 1.60 \cong 2$$

   $$Vssc = \frac{5.5 * 10 * 3 * 0.11 * 1.73}{20} = 1.60 \cong 2$$

   d. Calculate the number of power pins:

   # of Vdd = max [4, 3, 2] = 4
   # of Vssp = 4
   # of Vssc = max [3, 2] = 3

2. Determining the power pin locations:

   Use all 4 corner preassigned fixed power pins.

3. Placing the I/O buffers:

   Although only 3 Vssc pins are required, all 4 preassigned fixed Vssc pins can be used without adding any extra package pin count. It is always a good habit to keep as many power pads as possible to keep the effects of noise to a minimum.

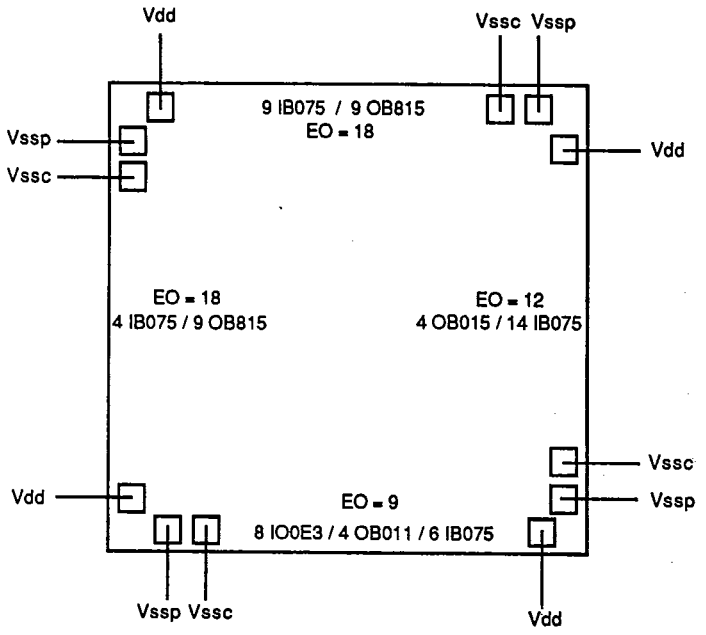


Figure 1–3. Input, Output I/O and Power Pad Location

Example

Assume a GC20000 circuit with the following outputs:

12	OB035	(conventional 8mA OB)
18	OB835	(slew rate controlled 8mA OB)
4	OB013	(4mA OB)
4	OB012	(2mA OB)
20	IB015	(CMOS IB)
20	IB075	(TTL IB)

Operating conditions:
max Vdd = 5.5V
frequency = 7MHz
average fanout FO = 2.5
maximum # of gates switching at a given time = 3.5K

1. Calculate the number of power pins:

   a. Output buffer considerations:

12	OB035	N8 = 12
18	OB835	N8SR = 18
4	OB013	N4 = 4
4	OB012	N2 = 4

The equivalent output is:

$$EO = (0.16 * N0) + (0.25 * N1) + (0.5 * N2) + N4 + (3 * N8) + (2 * N8SR)$$
$$EO = (0.16 * 0) + (0.25 * 0) + (0.5 * 4) + 4 + (3 * 12) + (2 * 18)$$
$$EO = 78$$

Vdd required $\frac{EO}{16} = \frac{78}{16} = 4.90 \cong 5$

Vssp required $\frac{EO}{16} = \frac{78}{16} = 4.90 \cong 5$

   b. Input buffer considerations:

20	IB015
20	IB075

Vdd required $\frac{\#\text{ of IB}}{20} = \frac{40}{20} = 2$

Vssc required $\frac{\#\text{ of IB}}{20} = \frac{40}{20} = 2.$

c. Core transistor considerations:

$$Vssc = Vdd = \frac{Cl * Vdd * f * \#gate}{20}$$

$$Vdd = \frac{5.5 * 8 * 3.5 * 2.5 * 0.11 * 1.73}{20} = 3.7 \cong 4$$

$$Vssc = \frac{5.5 * 8 * 3.5 * 2.5 * 0.11 * 1.73}{20} = 3.7 \cong 4$$

d. Calculate the number of power pins:

# of Vdd = max [5, 2,.4,] = 5
# of Vssp = 5
# of Vssc = max [2, 4] = 4

2. Determining the power pin locations:

Use all 4 corner preassigned fixed power pins and one additional Vdd and Vssp pin on the center of the right side of the die.

3. Placing the I/O buffers:

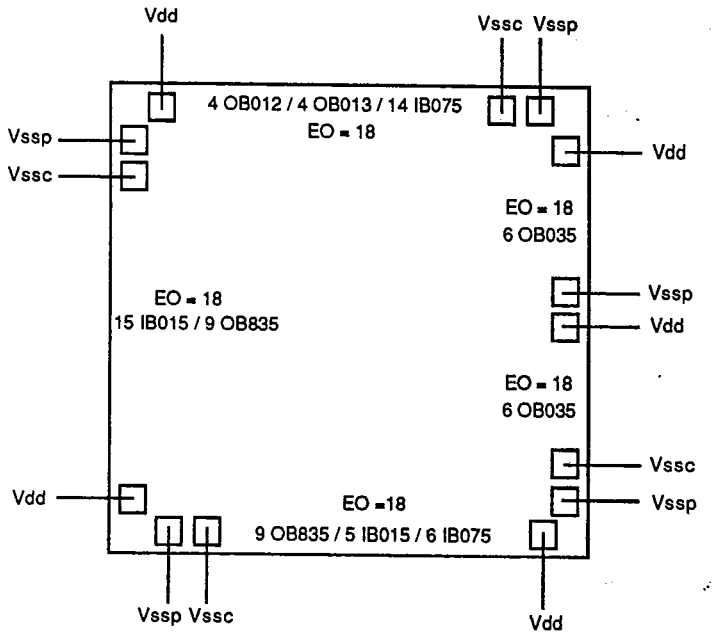


Figure 1–4. Input, Output I/O and Power Pad Location

1.2 CHOOSING AN INTERFACE

1.2.1 The Design Flow

Before defining the interface points, it is useful to review the ASIC design flow from schematic capture through back annotation. Figure 2–1 illustrates the steps necessary to develop an ASIC circuit on a workstation.

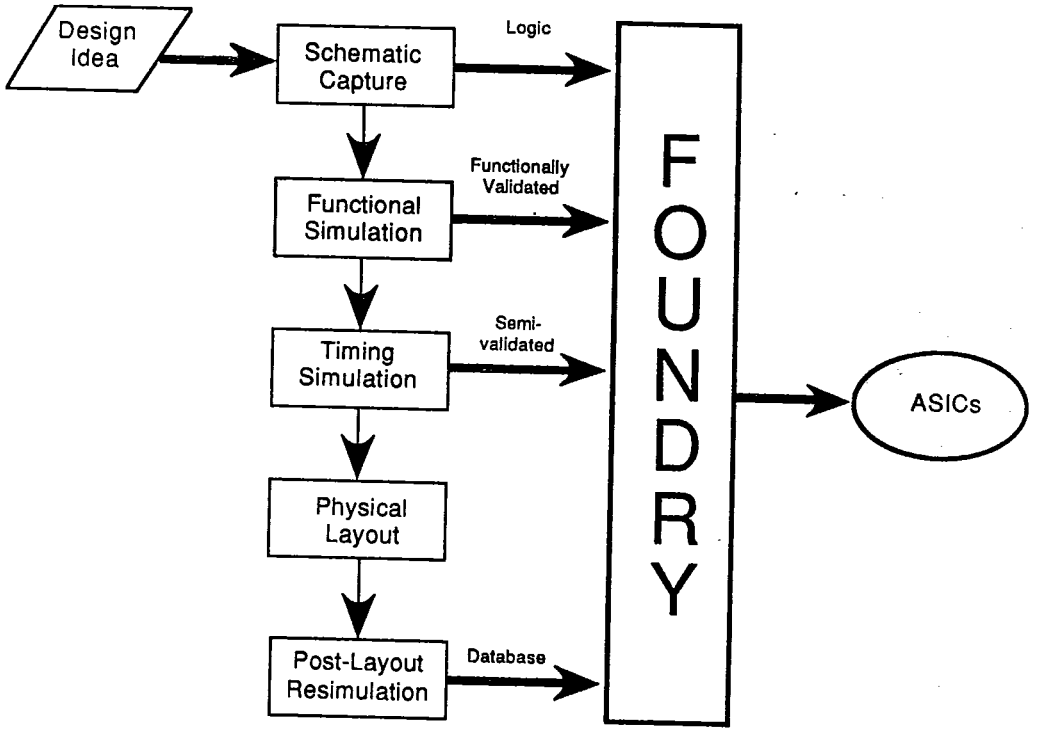


Figure 2–1. ASIC Design Flow

1.2.1.1 Schematic Capture

Schematic capture is the process of drawing a logic diagram on a workstation using a Gould approved library.

1.2.1.2 Functional Simulation

After the logic diagram has been drawn, the circuit is tested for correct operation when stimulated by the customers input vectors. During this simulation, each logic element has a typical delay. On some workstations you may skip this step and go directly to an estimated timing simulation.

1.2.1.3 Estimated Timing Simulation

The estimated timing simulation is performed before layout with statistically calculated wire lengths and the actual output loading caused by input capacitance of the gates being driven. Because Gould has made many ASICs, the statistical database is large and accurate. Today, less than 5 percent of our circuits are recycled through place and route because of wire length requirements.

1.2.1.4 Physical Layout

After the estimated timing simulation is completed, the physical layout is done on the workstation. This process is called place and route. During this step, the individual cells or macros are placed using an algorithm that minimizes wire lengths.

1.2.1.5 Post-Layout Resimulation

Post-layout resimulation is the last step in the ASIC design cycle before circuit tooling is generated. During this process, the actual capacitance loading on each node of the circuit is extracted from the final physical layout . These capacitance values replace the estimated values in the timing simulation. The simulation is rerun and the results are compared against estimated timing data. If the performance does not meet pre-layout results, the slow logic paths are identified and the circuit is modified such that it can be successfully placed and routed.

1.2.2 Standard Interface Points

There are four standard interface points between the customer and Gould for a gate array or standard cell project.

- Logic Drawing
- Functionally Validated Netlist (FVNL)
- Semivalidated Netlist (SVNL)
- Database (DBASE)

Other interface points are possible; check with your Gould sales representative. Figure 2–5, at the end of this chapter, illustrates the balance of effort between the customer and Gould for the different interface options.

With any interface, the customer must provide test vectors*. These will be formatted by Gould and must conform to test vector criteria. The function of the circuit is defined by test vectors. It is the customer's responsibility to provide a set of vectors that fully exercise the device. See Chapter 5 for a discussion of testing.

* Option for Gould generated vectors at extra cost.

1.2.2.1 Logic Drawing

The customer creates a logic drawing showing the functional behavior of the circuit and sends the drawing to Gould for implementation. This is the most costly and time-consuming interface; it has given way , in many cases, to the interface points described below.

1.2.2.2 Functionally Validated Netlist (FVNL)

The functional circuit is supplied as a netlist which has been functionally validated by customer simulation. Functionality is defined by the test vectors, which the customer supplies in the Gould format. No timing analysis has been performed. Gould performs parametric timing simulation with estimated interconnect capacitance to compare with the customer's simulations. Gould then performs a back-annotated simulation after layout with the customer's defined input vectors (for comparison with previous Gould simulations). The customer is responsible for schedule and NRE expenses due to any race and hazard conditions detected by the Gould timing simulation.

1.2.2.3 Semivalidated Netlist (SVNL)

The circuit is supplied as a netlist, which has been validated by the customer via prelayout-parametric simulation. Device capability, temperature, voltage, loads (including statistically estimated interconnect loads) and process variations are taken into account. Tester, package, and pin loads are 50 pF. The maximum temperature is assumed to be 10°C above the maximum ambient temperature defined in the Standard Test Specification.

1.2.2.4 Database (DBASE)

Gould supports physical design on Mentor workstations. The customer supplies a netlist, vectors in Gould format, the interconnect capacitance table, and geometrical data for circuit macro placement.

1.2.3 Gould Design Services

In addition to the standard interface points, Gould clients can choose to use one or more design services to reduce the workload. NETRANS ™ and GATE GOBBLER ™ are services currently available which allow data entry in non-Gould netlist formats and optimize designs for area efficiency, respectively. Figure 2–2 shows how a system designer might choose among the different paths available depending on the goal and existing specification.

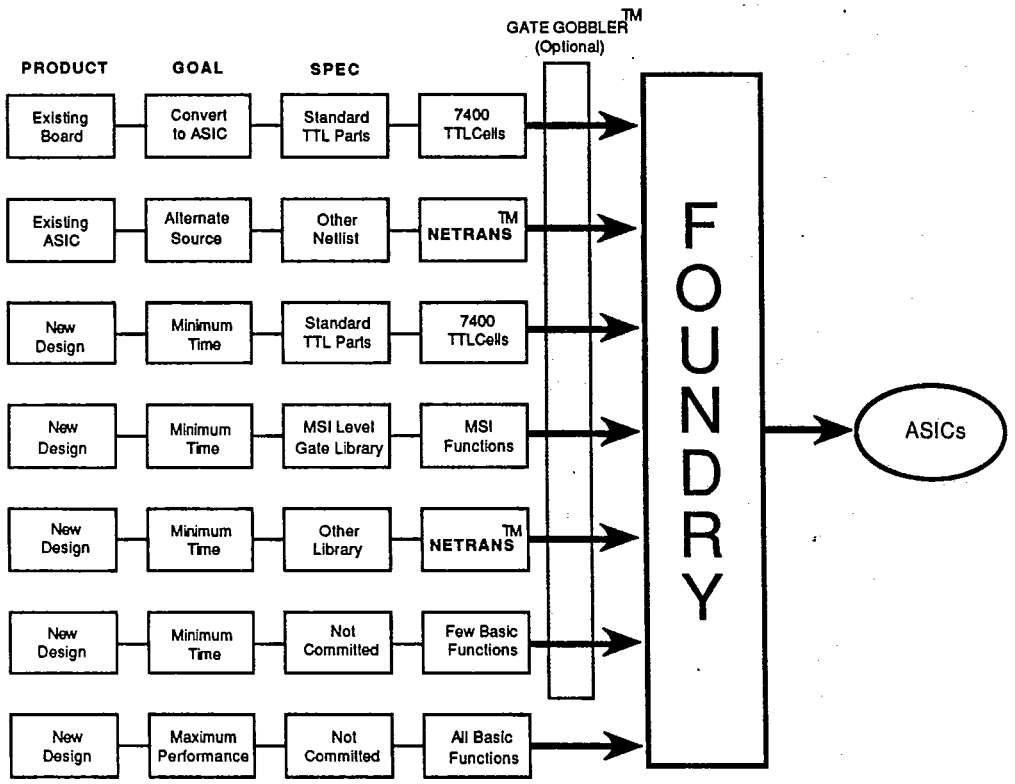


Figure 2–2. Optional Design Services

1.2.3.1 NETRANS ™

NETRANS is a software tool developed around artificial intelligence techniques which enables Gould to accept a design in any application specific IC format and translate it into a Gould-compatible (BOLT) netlist. It can also translate any test vector format (LTX, Teradyne and Sentry) into Gould-compatible test vectors. The NETRANS service frees the designer of single library/vendor constraints when an alternate source or conversion from Gate Array to Standard Cell is needed. Using NETRANS saves many weeks of design time since there is no need to re-create an existing proven design from scratch onto a new library.

The translation is performed by initially converting the netlist into BOLT format. This is followed by one-to-one mapping of macro cells into Gould macro cells. The test vectors are next converted into Gould's format. Accuracy of the conversion is finally verified by simulating the design. After NETRANS operation the design is ready for layout and fabrication in the normal development cycle. Figure 2–3 illustrates the NETRANS functions.

The design format preferred for input is any ASCII, IBM PC AT/XT, MS DOS format or compatible, 5 1/4" floppy disk. Other formats are UNIX 9 track tape, VAX/VMS tape, Mentor cartridge, or an unlabeled 9 track tape with 80 characters record and 20 record blocks.

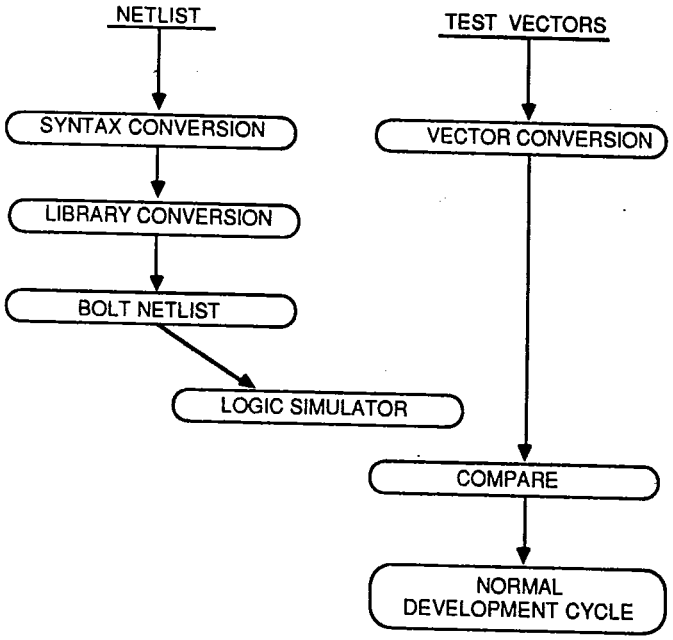


Figure 2–3. Netrans Functions

1.2.3.2 GATE GOBBLER ™

Gate Gobbler is one of Gould's EXPERT ASIC ™ design tools for CAE. It is a rule based artificial intelligence expert system that reduces the gate count of standard cell and gate array circuits without affecting performance. Gate count reductions translate directly into area, cost, package, and room for additional functionality benefits to the system designer.The gate count reduction depends on the rules invoked and the optimization of the original circuit design. Reductions of over 10% have been observed, typical reductions are 7%. These savings are accomplished by substituting more optimal gate selections and eliminating unused functions in the original netlist. Performance is not affected and further, the more efficient netlist is always rechecked to insure that it still runs the original test vectors.

Gate Gobbler gives the designer several important new choices in design methodology. First, the design does not need to be manually optimized for production since Gate Gobbler does that automatically. This reduces development time, which is almost always a valuable resource.

Second, the designer is no longer required to learn and work with a large number of library elements. This also reduces development time and it allows the designer to focus attention on the higher level design functions rather than expending this same energy on the fine details of small differences within the library. The designer can work comfortably with a small, familiar set of library elements of his or her own choice, knowing that Gate Gobbler will optimize the circuit later.

Third, by automatically reducing the gate count of designs made from any choice of library elements, Gate Gobbler helps make vendor-independent designs practical. An example of this is the use of the 7400 functions. The 7400 standard parts often have features which remain unused on an ASIC design, but the functions are familiar to most designers and several foundries offer 7400's as macros or cells. Until Gate Gobbler eliminated the gate count penalty, it was not economical to choose the 7400's for a design that some day might reach high production volumes. Now the designer can choose to capture his logic in 7400 functions and rely on the fact there will be an efficient alternative as well as multiple vendors when the circuit is ready for silicon. Figure 2–4 illustrates the Gate Gobbler functions.

The Gate Gobbler expert system is run by a Gould ASIC design center as a service for designs submitted to Gould Semiconductor. All that is required is a netlist and set of test vectors. The Gate Gobbler is a service run as a courtesy to all system designers. If the gate reduction is not significant or if the new netlist fails to run the original test vectors, the design verification and circuit fabrication may still proceed with the original netlist. When the above two conditions are met,the system designer examines all the information and makes the decision as to which netlist should proceed into fabrication.

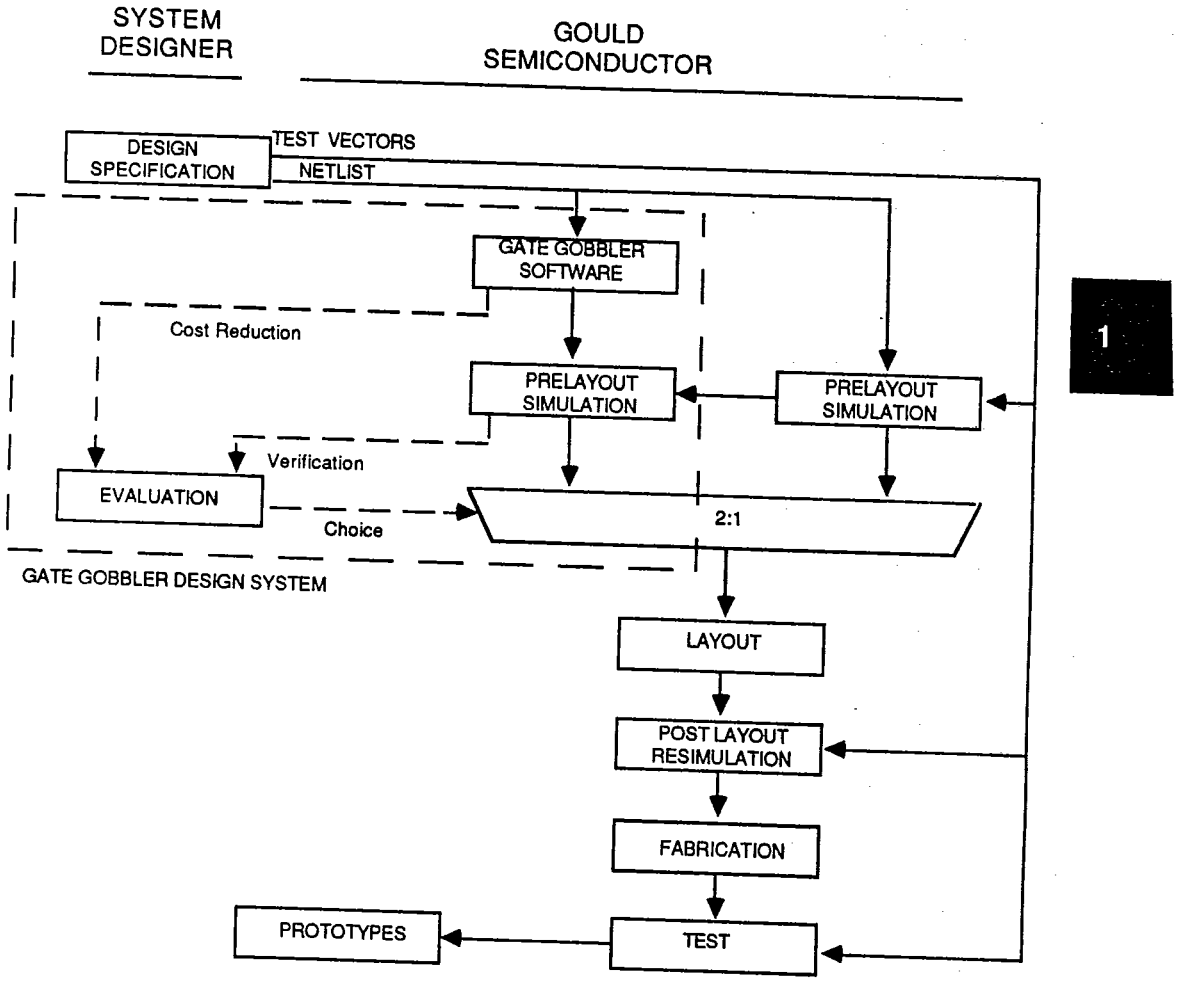


Figure 2–4. Gate Gobbler Functions

Option	Logic Drawing	Functionally Validated Netlist	Semi-Validated Netlist	Database**
Task Summary	Logic Schematic Electrical Spec	plus Functional Logic Simulation (no timing analysis)	plus Parametric Logic Simulation (with estimated timing)	plus Place and Route
Function Specification Logic Drawing or Circuit Schematic Timing Diagrams Standard Test Specification (AC/DC)	Customer	Customer	Customer	Customer
Logic Conversion (to Gould cells) Schematic Entry Logic Stimulus/ Response Patterns	GOULD			
* Pre-Layout Functional Simulation				
* Pre-Layout Timing Simulation (with estimated loading)		GOULD		
Automatic Place-and-Route (Physical Layout) * Post-Layout Re-simulation (with actual loading data) Formal Vectors (for use with a Sentry 21 tester)			GOULD	
Standard Test Program Photo Tape Stepper Tooling Prototype Wafer Fab Functionally-tested Ceramic Samples (25 units) Fully-Tested Prototypes (25 units)				GOULD
Primary Input Medium	Logic Schematic	Floppy Disc	Tape or Floppy Disc	Tape or Floppy Disc

* Requires customer approval when performed by Gould
**Database availability is limited depending on workstation and customer requirements.

Figure 2–5. ASIC Design Interface Points

1.3 INTERPRETING THE DATA SHEETS

The data sheets in this manual give the important information about the GC series Gate Array devices. This chapter explains how to use them, and provides curves with design information that relate to all gate array devices.

1.3.1 Determining DC Characteristics

Through examples, this section illustrates how to determine the DC characteristics for output drivers and input pull-up/pull-down resistances. The characteristic curves are characterized at Vdd = 5.0V, with a junction temperature of 25°C and with typical processing.

The N-Channel curves (Figures 3–1 and 3–3) represent the properties of the pull-down resistor on the input buffers and the N-Channel driver on the output and IO buffers. The P-Channel curves (Figures 3–2 and 3–4) represent the pull-up resistor on the input buffers and the pull-up device on the output and IO buffers.

1.3.1.1 Output Driver Currents

The output driver sink and source current can be estimated using the equation

$$Isink = Ids * Kpvdc * Kt$$

where

Ids = sink current for the corresponding Vout value (Figure 3–1 and Table 3–1)
or Ids = source current for the corresponding Vout value (Figure 3–2 and Table 3–1)
Kpvdc = process/voltage DC derating factor (Table 3–4)
Kt = temperature DC derating factor (Figure 3–5 and Table 3–3)
Junction temperature (T_j) = Ambient temp. (T_a) + 10°C

Example

The output current through an OB015 buffer, under the following conditions, can be estimated as:

- Vdd = 4.5V
- Worst-case process
- Ambient temperature = 70°C
- Vout = Vol = 0.4V

Can be obtained as shown below:

1. For Vout = 0.4V, Ids = 15.45mA, from Figure 3–1
2. For worst-case process, Vdd = 4.5V, Kpvdc = 0.67, from Table 3–4
3. For T_a = 70°C, T_j = 80°C
4. For T_j = 80°C, Kt = 0.78, (Table 3–3 or Figure 3–5)

Using the Isink equation and the derating factors we find the DC current for the specified conditions:

Isink = Ids * Kpvdc * Ktdc

Iol = Isink = 15.5mA * 0.67 * 0.78

Iol = 8.10mA

Example

The output current through an OB015 buffer, under the following conditions, can be estimated as:

- Vdd = 4.5V
- Worst-case process
- Ambient temperature = 70°C
- Vout = Voh = 2.4V

Can be obtained as shown below:

1. For Vout = 2.4V, Ids = 19.5mA, from Figure 3–2
2. For worst-case process, Vdd = 4.5V, Kpvdc = 0.53, from Table 3–4
3. For T_a = 70°C, T_j = 80°C
4. For T_j = 80°C, Kt = 0.78, (Table 3–3 or Figure 3–5)

Isource = Ids * Kpvdc * Kt
Ioh = Isource = 19.5mA * 0.53 * 0.78
Ioh = Isource = 8.01mA

1.3.1.2 Pull-Up/Pull-Down Current

The pull-up (Ipu) and pull-down current (Ipd) can be estimated using the following equation:

Ipd = Ids * Kpvdc * Kt

where

Ids = current through pull-up transistor for the corresponding Vin (Figure 3–4 and Table 3–2)
or Ids = current through pull-down transistor for the corresponding Vin (Figure 3–3 and Table 3–2)
Kpvd = process/voltage DC derating factor (Table 3–4)
Kt = temperature DC derating factor (Figure 3–5 and Table 3–3)
Junction temperature (T_j) = Ambient temp. (T_a) + 10°C

Example

The DC current through the pull-up transistor of the IB095 input buffer, under the following conditions:

- Vdd = 4.5V
- Worst-case process
- Ambient temperature = 70° C
- Vin = 2.4V

Can be obtained as shown below:

1. For Vin = 2.4V, Vds = Vin - Vdd = 2.4V - 5.0V = -2.6V
   (always assume Vdd = 5.0V, the equation will derate Vdd to 4.5V later)
2. For Vds = -2.6V, Ids = -117.0µA, from Table 3–2
3. For worst-case process, Vdd = 4.5V, Kpvdc = 0.53, from Table 3–4
4. For T_a = 70°C, T_j = 80°C
5. For T_j = 80°C, Kt = 0.78, (Table 3–3 or Figure 3–5)

Using the Ipu equation and the derating factors we find the DC current for the specified conditions:

Ipu = -117.0µA * 0.53 * 0.78
Ipu = -48.4µA

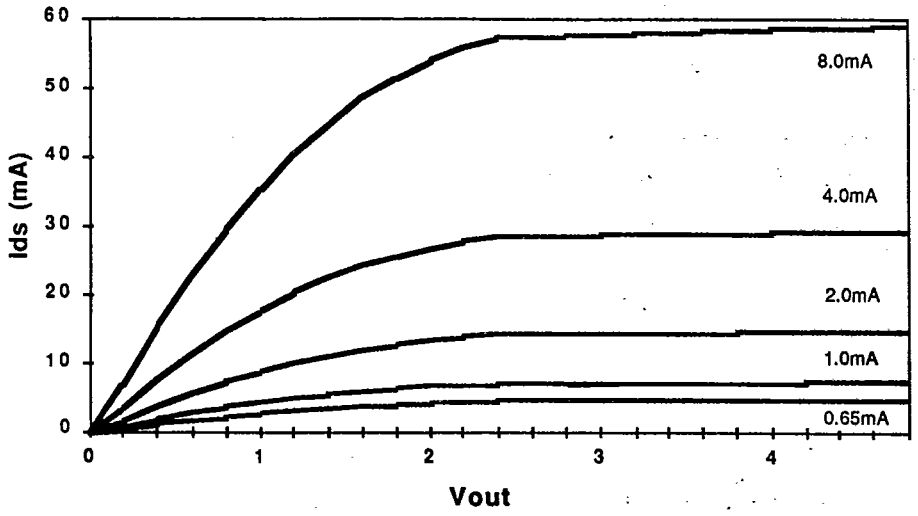


Figure 3–1. Typical N-Channel Driver DC Characteristics

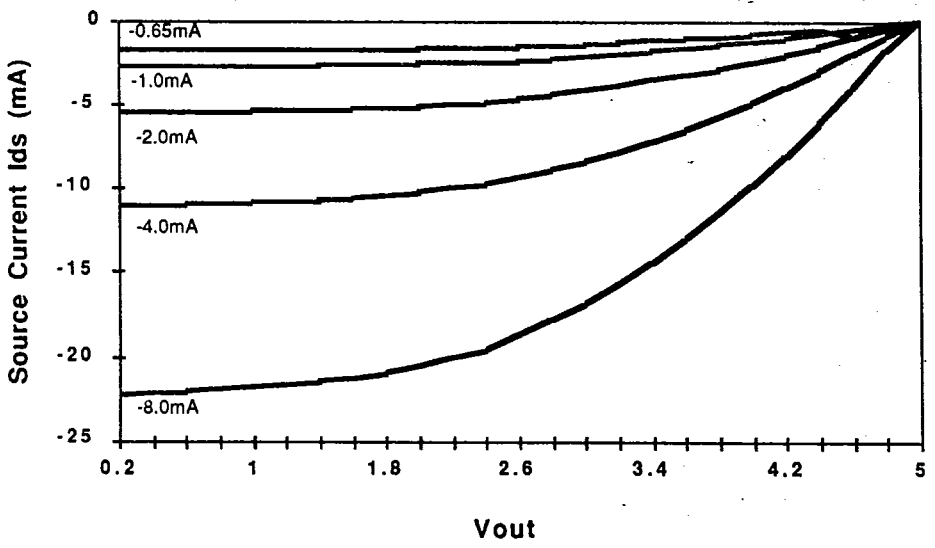


Figure 3–2. Typical P-Channel Driver DC Characteristics

Table 3–1
IV CHARACTERISTICS, 1.25µ DM GA OUTPUT BUFFERS

Typical case process, Vdd = 5.0V, T_j = 25°C

N- Channel

Vout	Ids (mA) 8.0mA	Ids (mA) 4.0mA	Ids (mA) 2.0mA	Ids (mA) 1.0mA	Ids (mA) 0.65mA
0.4V	15.45	7.70	3.85	1.92	1.26

P- Channel

Vout	Ids (mA) 8.0mA	Ids (mA) 4.0mA	Ids (mA) 2.0mA	Ids (mA) 1.0mA	Ids (mA) 0.65mA
2.4V	19.50	9.70	4.83	2.41	1.57

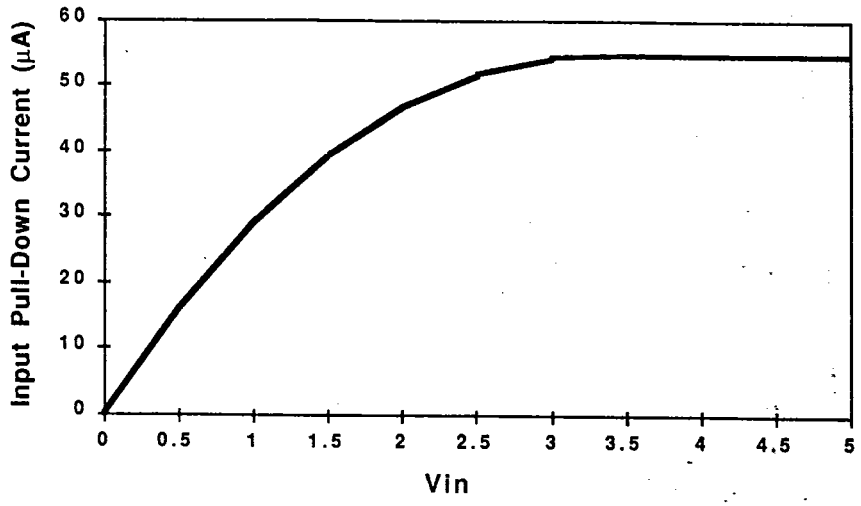


Figure 3–3. Typical N-Channel Input Pull-Down DC Characteristics

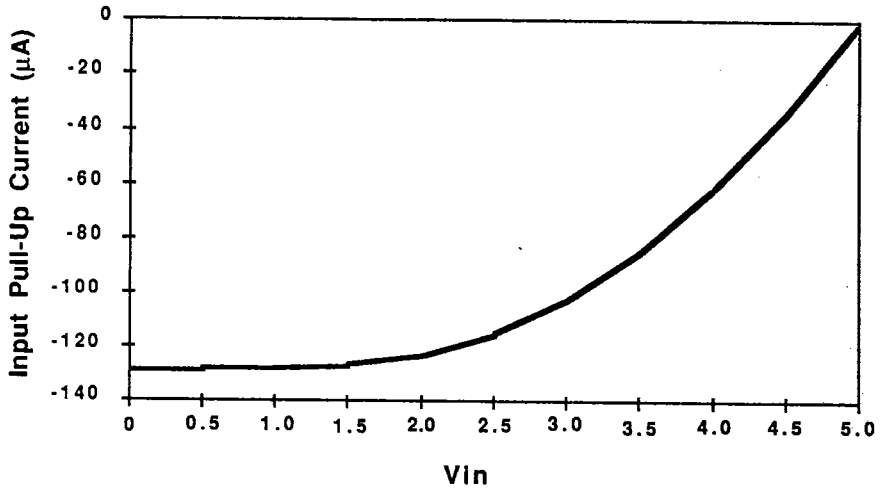


Figure 3–4. Typical P-Channel Input Pull-Up DC Characteristics

Table 3–2
INPUT PULL-UP AND PULL-DOWN CURRENT VALUES

Typical case process, Vdd = 5.OV, T_j = 25°C

Vinput (V)	Pull-Down Current (μ A)
0.0	0.0
0.5	16.0
1.0	29.1
1.5	39.3
2.0	46.9
2.5	51.9
3.0	54.4
3.5	54.8
4.0	54.8
4.5	54.9
5.0	54.9

Vinput (V)	Pull-Up Current (μ A)
5.0	0.0
4.5	-33.7
4.0	-61.9
3.5	-84.9
3.0	-102.7
2.5	-115.6
2.0	-123.6
1.5	-127.0
1.0	-127.8
0.5	-128.3
0.0	-128.8

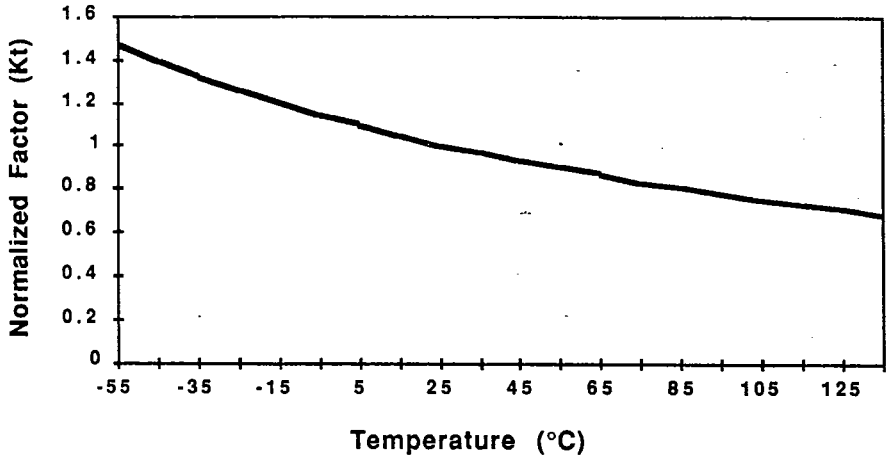


Figure 3–5. DC and AC Variations with Temperature

Table 3–3
TEMPERATURE DERATING FACTORS FOR AC and DC CHARACTERISTICS (K_t VS. TEMP)

Junction Temperature °C	Temperature Derating Factor K_t
-55	1.47
-45	1.39
-35	1.32
-25	1.26
-15	1.20
-5	1.14
5	1.10
15	1.05
25	1.00
35	0.97
45	0.93
55	0.90
65	0.87
75	0.83
85	0.81
95	0.78
105	0.75
115	0.73
125	0.71
135	0.68

1

Table 3–4
PROCESS, VOLTAGE DC DERATING FACTORS
(K_{pvdc})

N-Channel (Vout = 0.4V)		
Vdd=4.5V	Vdd=5.0V	Vdd=5.5V
Worst Case	Typical Case	Best Case
0.67	1.00	1.45

P-Channel (Vout = 2.4V)		
Vdd=4.5V	Vdd=5.0V	Vdd=5.5V
Worst Case	Typical Case	Best Case
0.53	1.00	1.88

1.3.2 AC Characteristics

In addition to the DC characteristics discussed above, the AC characteristics must also be considered. This section discusses flip-flops, propagation delays, and I/O buffer timing.

1.3.2.1 Flip-Flops

Set-up and Hold Times

The setup and hold times of every flip-flop in the Macro Cell Library are specified in the data sheets. Setup time is the minimum length of time for which the input data to be clocked must be stable *before* the leading or trailing edge of the clock. Hold time is the minimum length of time for which the data to be clocked should be stable *after* the active edge of the clock.

Figure 3–6 illustrates setup and hold time for a typical flip-flop.

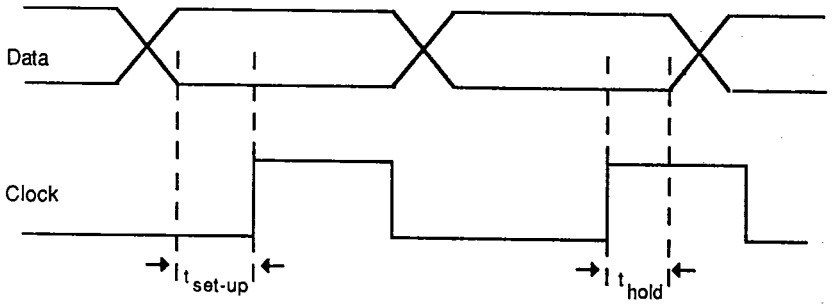


Figure 3–6. Flip-Flop Setup and Hold Timing

To ensure reliable operation of flip-flops, the setup and hold time requirements must be met.

Synchronous Reset and Set

Some flip-flops in the Macro Cell Library have synchronous set and reset signals. A synchronous set or reset is active *only* when Clock is high. The timing diagram for the macro cell DF16 in Figure 3–7 illustrates the synchronous reset operation.

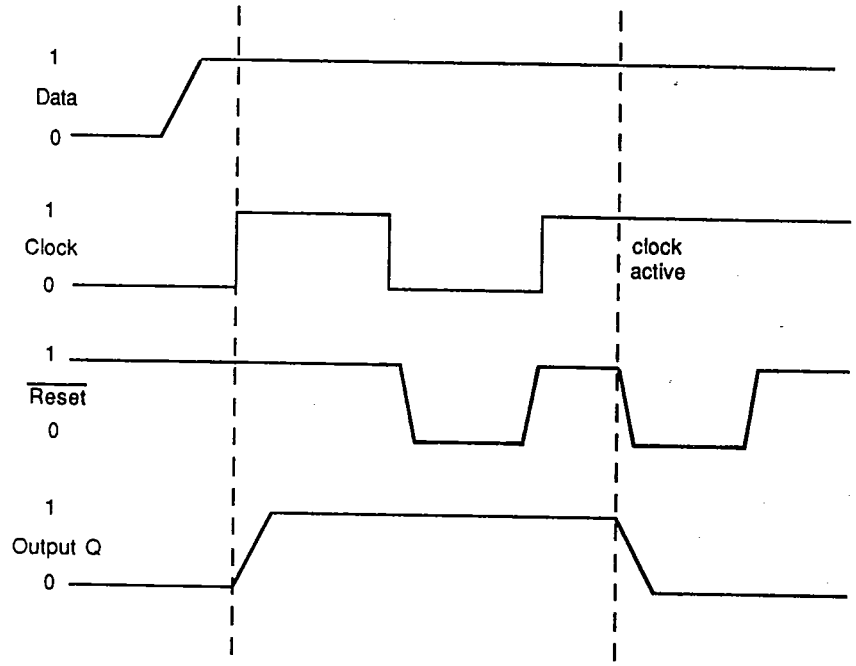


Figure 3–7. Flip-Flop Synchronous Reset Timing

1.3.2.2 Propagation Delay Estimation

The data sheets for each macro cell in the library have specific information for propagation delay estimation. Use this information to estimate the propagation delay of a critical path in a design. The total propagation delay of a path is defined as the summation of the delay of each macro in the path modified by the process, voltage and temperature derating factors.

$$tpd = \sum_{n=1}^{N} (tpdn) * (Kpv) / (Kt) = (Kpv) / (Kt) \sum_{n=1}^{N} (tpdn)$$

where

tpdn = propagation delay of macro Mn in the path, estimated from the data sheets
Kpv = AC process/supply voltage derating factor (Table 3–5 or Figure 3–11)
Kt = temperature derating factor (Table 3–3 or Figure 3–5)

The propagation delay for a macro Mn is defined as

tpdn = tdxn + Kn * Fn for all input buffer macros and core macros
tpdn = tdxn + Ktdxn * Cn for all the output and I/O buffer macros

where

tdxn, Kn and Ktdxn = intrinsic parameters from the data sheets
Fn = total number of unit loads that are driven by the core macro Mn
Cn = total capacitance on the output/IO pin driven by the pad macro Mn

For an I/O macro, both equations above are used.

Note that the fanout (Fn) is the total number of equivalent unit loads driven by the macro Mn, including its own output load, if any. The internal tristatable macros should have a fanout not only their own output loads but also any other output loads that are driven along with all input loads. Figures 3–8 and 3–9 illustrate the calculation of fanout (F) and propagation delay (tpd).

The propagation delay calculations for flip-flops and latches are slightly different than logic gates. The data sheets show input-to-output as well as output-to-output delays. The output loading on both Q and QN must be considered. The reasons for these specifications become obvious if you look at the logic schematic for a DF09 macro cell, for example. Here the propagation delay from C to QN depends on the loads on both QN and Q. It is determined by adding QN-to-Q delay to C-to-QN delay.

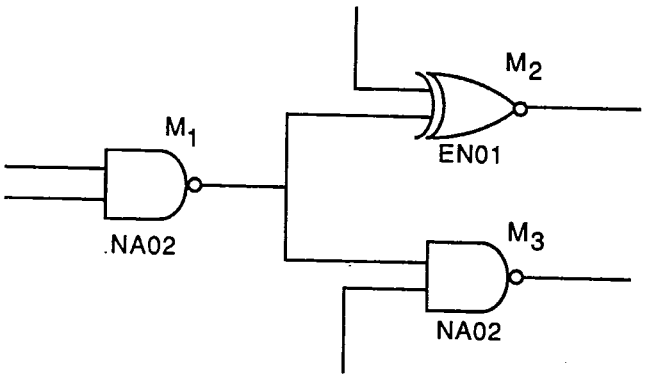
SN-to-Q delay is dependent upon the fanout on node Q. Because the QN output goes low *after* Q goes high, the SN-to-QN delay is dependent on the fanout on the output Q.

Note that the setup and hold time requirements must be met *before* the propagation delay estimation is made.

Figure 3–10 illustrates propagation delay estimation of a critical path in a design.

The estimated tpd path is from the data sheets and, therefore, for Vdd = 5.0V, junction temperature = 25°C and typical-case process.

Example 1



Loads driven by M_1 in Example 1 is:

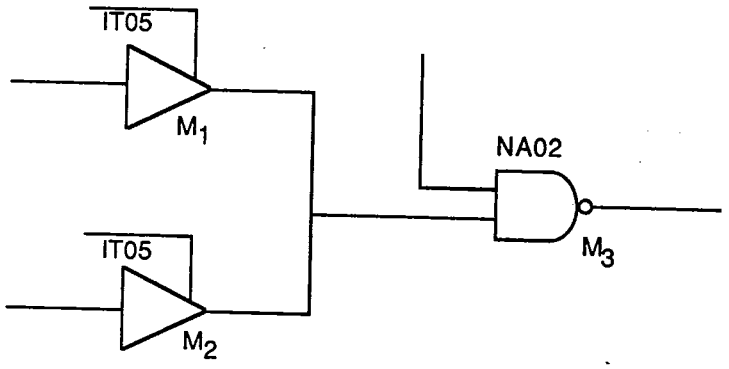
$F_1 = M_2$ input + M_3 Input
$= 2 + 1$
$= 3$

From the datasheet for the Macro Cell NA02,
tdr = 0.23ns Kr = 0.15ns/load
tdf = 0.19ns Kf = 0.14ns/load

tpd_1 t_{PLH} $M_1 = 0.23 + 0.15 * 3 = 0.68$ns
t_{PHL} $M_1 = 0.19 + 0.14 * 3 = 0.61$ns

Figure 3–8: Fanout and Propagation Delay Examples

Example 2



In Example 2, the fanout on the output of M_1 would be:

$F_1 = M_1$ output + M_2 output + M_3 input

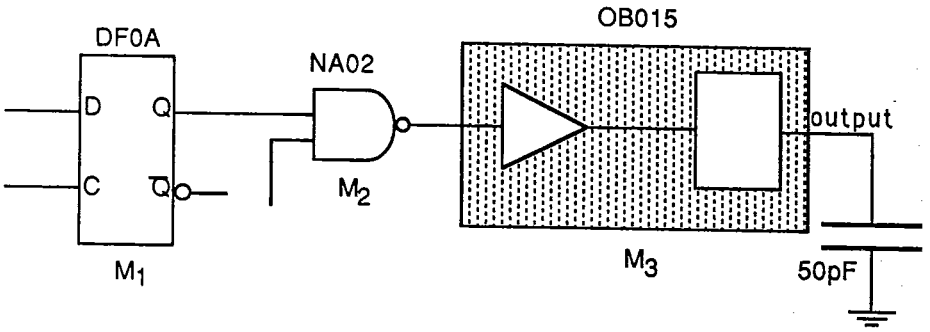
$=1.2 + 1.2 + 1.0 = 3.4$

From the datasheet for IT01, A-Q,
tdr = 0.510 Kr = 0.120
tdf = 0.560 Kf = 0.100

tpd_1 tPLH $M_1 = 0.510 + 0.120 * 3.40 = 0.920$ns
tPHL $M_1 = 0.560 + 0.100 * .3.40 = 0.900$ns

Figure 3–9: Fanout and Propagation Delay Examples

Example 3



Macro	M1		M2	M3	
Fan out (F or CL)	0	1	4	50 pf	
Delay	C - $\overline{Q}$	$\overline{Q}$ - Q	A - Q	A - Q	Tpd Path
tPLH (ns) output switches from L to H	0.63	.32+.15*1=.47	.23+4*.15=.83	.92+.07*50=4.4	6.3
tPHL (ns) output switches from H to L	0.8	.26+.11*1=.37	.19+4*.14=.75	1.08+.08*50=5.1	7.1

(ADD IN DIRECTION OF ARROWS)

Figure 3–10. Critical Path Propagation Delay Example

If Vdd = 4.5V and ambient temperature = 70° C (Junction temp = 80°), for worst-case process the delay for the path would become:

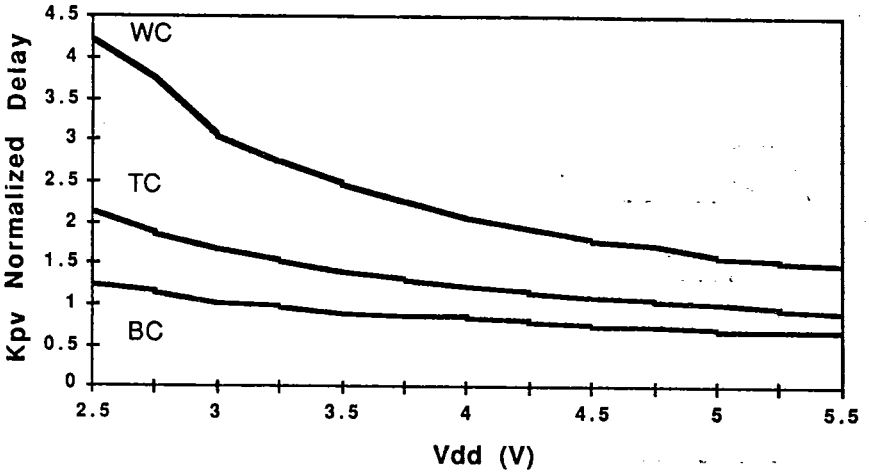
tdp = (tpd path) * (Kpv) * (Kt)
Kpv = 1.78 From AC characteristics (Figure 3–11 or Table 3–5)
Kt = 0.78 (Table 3–3 or Figure 3–5)

$$tpd = \frac{(6.3) * (1.78)}{(0.78)}$$

= 13.7ns for tplh

$$= \frac{(7.10) * (1.78)}{(0.78)}$$

= 16.4ns for tphl



T = 25°C Normalized to 5.0V at Typical Process

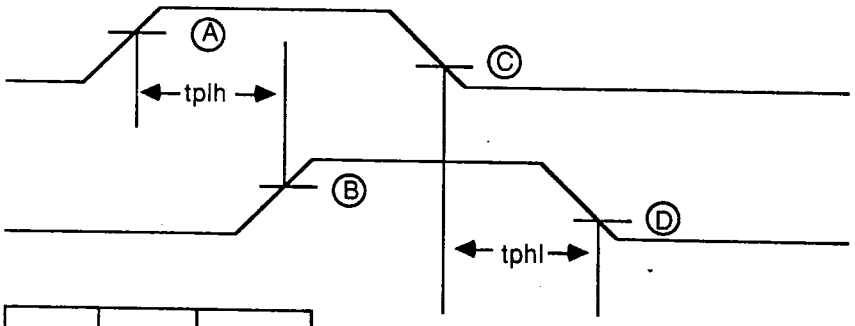
Figure 3–11. Delay Derating (Kpv).

Vdd	(Kpv) Worst Case Speed	(Kpv) Typical	(Kpv) Best Case Speed
2.50	4.22	2.13	1.25
2.75	3.57	1.86	1.15
3.0	3.05	1.67	1.01
3.25	2.73	1.52	0.97
3.50	2.47	1.39	0.89
3.75	2.26	1.30	0.85
4.0	2.05	1.21	0.83
4.25	1.92	1.14	0.78
4.50	1.78	1.08	0.73
4.75	1.72	1.03	0.72
5.0	1.60	1.00	0.68
5.25	1.53	0.94	0.67
5.50	1.49	0.90	0.65

Table 3–5
ACProcess and Operating Voltage (Kpv).

1.3.2.3 I/O Voltage and Timing Characterization

The simple timing waveforms in Figure 3–12 describe how the propagation delays of input, output, and input/output buffers were characterized (with respect to voltage levels) for data presented in the data sheets.



Level	TTL	CMOS
VA	2.0	0.7 Vdd
VB	2.0	0.7 Vdd
VC	0.8	0.3 Vdd
VD	0.8	0.3 Vdd

Figure 3–12. I/O Buffer Timing

1.3.3 Vdd/Vss Strapping Limits

In typical logic designs , there are occasionally unused input and output pins to macros. Unused outputs (such as the Q output in an SR latch) must be left floating. However, unused inputs must be strapped to Vdd or to Vss to prevent reliability problems caused by floating inputs. Do this in the logic drawing by calling up either the core Vdd (CVdd) or core Vss (CVss) macros and attaching the Q output of the CVdd (or CVss) macro to the unused macro input pin. CVdd and CVss are connections to the core Vdd and Vss buses, respectively. These take up no area set aside for logic macros, but the signal lines do take up routing tracks.

When using the CVss (or CVdd) macro in a design, you should realize that you can have any number of macro inputs tied-down (tied-up) for a given CVss (CVdd) macro. However, there is a physical limit to the number of different CVss (CVdd) macros available per gate array type. Table 3–6 defines these limits. Gould recommends using only one CVdd and one CVss to avoid routing congestion.

Table 3–6
NUMBER OF CVDD/CVSS MACROS AVAILABLE

	Number of Macros Available	
Gate Array Name	CVdd	CVss
GC40K	-	-
GC30K	-	-
GC25K	-	-
GC20K	150	150
GC15K	100	100
GC10K	86	86
GC7.5K	36	36
GC5K	4	4
GC3K	-	-

1.3.4 Input Thresholds

CMOS logic thresholds (Vt) are specified at 30 percent and 70 percent of the supply voltage for maximum Vil and minimum Vih, respectively. That is, for a device operating at 5 V, a maximum "0" level would be 1.5 V, whereas the minimum "1" level would be 3.5 V.

The specified input levels for TTL logic families are 0.8 V and 2.0 V for maximum zero and minimum one, respectively. Level-translation buffers are used when interfacing gate array with TTL or LSTTL components.

These TTL-to -CMOS level translators dissipate a significant amount of power, especially when the input voltage at the pin is held at the minimum TTL high level of 2.0 V. For this reason, Gould recommends that a pull-up be connected to the gate input to turn off the P-Channel half of the TTL-level translator, by using either the TTL input buffer macro that has a pull-up transistor or a pull-up device at the board level.

Table 3–5 lists the static current for selected input values of input voltage for a TTL buffer. The data assumes a typical process at a junction temperature of 25° C. Approximate values

of power dissipation in other process and junction-temperature scenarios can be estimated using the process and junction-temperature factors, Tables 3–3 and 3–4.

Table 3–7
CURRENT THROUGH TTL INPUT BUFFER

Vin (V)	Idc (mA)
0.00	0.00
0.60	0.00
0.70	0.01
0.80	0.06
0.90	0.16
1.00	0.29
1.05	0.37
1.10	0.48
1.15	0.64
1.20	0.88
1.25	1.27
1.30	2.11
1.35	0.89
1.40	0.87
1.45	0.85
1.50	0.83
1.55	0.81
1.60	0.79
1.65	0.77
1.70	0.75
1.75	0.72
1.80	0.70
1.85	0.68

Vin (V)	Idc (mA)
1.90	0.66
1.95	0.64
2.00	0.62
2.05	0.60
2.10	0.58
2.15	0.56
2.20	0.54
2.25	0.52
2.30	0.50
2.35	0.48
2.40	0.46
2.45	0.44
2.50	0.43
2.55	0.41
2.60	0.39
2.65	0.37
2.70	0.35
3.00	0.26
3.25	0.18
3.50	0.12
3.75	0.07
5.00	0.00

1.3.5 Dynamic Power

The basis behind calculating average dynamic power is summing together all the pieces that make up that power. The equation for calculating average power is:

$P = V^2 * C * f$
or $P = V^2 * Cl * IF * (\sum_K FO_K * f_K)$ where
P = average power
V = operating power
Cl = unit load $\frac{(pF)}{gate}$
IF = interconnect factor
FO_K = fanout of the kth node (average = 2)
f_K = switching frequency of the kth node

Dynamic power may be calculated in different ways. We recommend using this equation for both quick conservative estimations and the more involved analysis.

For a quick conservative estimation of the average power we suggest considering the core capacitance and the pad capacitance separately. That is:

Core Capacitance:

(# of utilized gates in the array) * (% of gates switching per cycle) * 2 * $\frac{(0.11pF)}{gate}$ * (1.73 interconnect factor) = core capacitance.

The number of simultaneously switching gates depends on the circuit, but a good estimate would be 25%.

Pad Capacitance:

(# of utilized output of IO pads) * (% of outputs switching per cycle) * $\frac{(output\ cap\ load)}{output}$ = pad capacitance.

Again the number of switching outputs is circuit dependent, as is the number of switching core circuits. A rule of thumb for switching outputs would be 15%.

Example:

An example of this method follows:

Suppose that one is doing a 6K array at 90% utilization, 5.5V supply maximum and running frequency is 25 MHz. Then the calculations of the core capacitance would be:

(5880 gates) * (90% utilized) * (25% switching) * 2 * $\frac{(0.11pF)}{gate}$ * (1.73 interconnect factor) = core capacitance.

Core capacitance = 504 pF.

The pad capacitance would be:

$$(132 \text{ possible IO pads}) * (.15 \text{ outputs switching per cycle}) * \frac{(50 \text{ pF})}{\text{IO}} = \text{pad capacitance.}$$

Pad capacitance = 990 pF.

Therefore, dynamic power is:

$(5.5 \text{ V})^2$ * (504pF core capacitance + 990 pF pad capacitance) * (25 MHz) = dynamic power.

Dynamic power = 1130mW.

If the dynamic power is under the system requirements then you're done.

Suppose after doing the previous calculation the dynamic power exceeded the system limits. The detailed analysis can be used to get a more accurate representation for the dynamic power.

Assume the same givens as in the previous example, i.e., 6k array, 90% utilization, 5.5 V supply maximum, 25 MHz. The equation for average power still holds, but now the individual capacitances are broken down and multiplied by their switching frequencies. The same is done for the outputs.

Places to look for groups of logic driving large capacitive loads includes master clocks for the chip, logic banks,decoders, and data buses. Keep in mind that it is the capacitance load being driven, not the actual gates switching that contribute the most to dynamic power.

Suppose after reviewing the circuit you discover the following information:

1. 100 gates switch at the 25 MHz rate.
2. 1000 additional gates switch at a 5 MHz rate.
3. 2 outputs switch per cycle at the 25 MHz rate.
4. 20 outputs switch per cycle at a 5 MHz rate.
5. The remainder of the gates switch somewhere below 1 MHz.
6. The remainder of the IO switch somewhere below 500 kHz.

The detailed method requires one to calculate the dynamic power individually and then sum them up.

For this example:

100 gates running at 25 MHz

(100 gates) * 2 * $\frac{(0.11pF)}{gate}$ * (1.73 interconnect factor) * (25 MHz) = sum #1.

Sum #1 = 952pF-MHz.

For the 1000 gates

(1000 gates) * 2 * $\frac{(0.11pF)}{gate}$ * (1.73 interconnect factor) * (5 MHz) = sum #2.

Sum #2 = 1904pF MHz.

For 2 outputs running at 25 MHz

(2 IO pads) * $\frac{(50pF)}{IO}$ * (5 MHz) = sum #3.

Sum #3 = 2500pF-MHz.

For 20 outputs switching at 5 MHz

(20 IO pads) * $\frac{(50pF)}{IO}$ * (5 MHz) = sum #4.

Sum #4 = 5000pF-MHz.

For the remainder of the gates

(5880 - 100 - 1000 gates) * 2 * $\frac{(0.11pF)}{gate}$ * (1.73 interconnect factor) * (1 MHz) = sum #5.

Sum #5 = 1820pF-MHz.

For the remainder of the IO

(132 - 2 - 20 IO) * $\frac{(50pF)}{IO}$ * (.5 MHz) = sum #6.

Sum #6 = 2750pF-MHz.

Adding the sums and multiplying the square of the operating voltage gives:

$(5.5\ V)^2$ * (952pF-MHz + 1904pF-MHz + 2500 pF-MHz +
5000 pF-MHz + 1820pF-MHz + 2750pF-MHz) = total dynamic power
Total dynamic power = 451mW.

Dynamic Power can be calculated either as a quick conservative calculation, or a more accurate computation, depending on ones particular needs.

1.4

AVOIDING DESIGN PROBLEMS

This chapter presents some suggestions for logic designers who are creating designs that will be implemented as a Gould gate array. Knowing some of the tricks-of-the-trade helps ensure that a design will be successful.

Synchronous logic is the key to reliable gate array implementations. Because numerous texts cover this subject, this section highlights only those considerations which are of greatest significance in the design of gate arrays.

1.4.1 Problems with Gated Direct-Action Signals

Direct action signals are input signals (to a flip-flop) that can independently (either with an edge or a level) cause the flip-flop to change state. The most common direct-action signals are CLK, SET, RESET and asynchronous LOAD. A gated direct-action signal is one that is fed by combinational logic (see Figure 4–1A). While there are several circumstances under which this circuit will work, it is important to note its disadvantages.

First, if CLK is high when CONTROL is asserted, the flip-flop will clock immediately. In this case the designer must ensure that the setup times on the flip-flop being clocked as well as any of the components downstream from the flip-flop have not been violated.

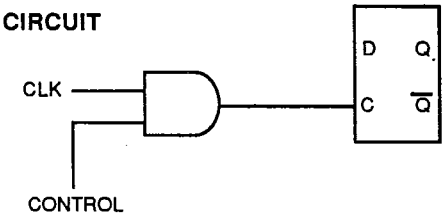
Second, if CONTROL were asserted just prior to CLK going low, a very narrow pulse could be generated at C (see Figure 4–1B). Simulators usually cannot handle narrow pulses (or glitches) accurately; that is, if a pulse is shorter than the minimum pulse width of the flip-flop, it will be ignored in simulation but such a pulse *might* clock the flip-flop on silicon, and cause the circuit to fail in the system.

The best way to avoid this problem is to use synchronous logic. Figure 4–2 shows a synchronous clock-and-hold circuit and a synchronized reset circuit, as an idea for dealing with this situation.

JK Flip-Flops versus Set-Reset Latches

Gated direct action signals most often appear in designs for register or counter decoders. Occasionally, there is a need to decode counter or register outputs to SET or RESET a flip-flop. If you use the direct-action SET or RESET inputs of a master-slave flip-flop (or a cross-coupled NAND or NOR structure), the circuit is not protected against the illegal decodes that flash across the counter or register as it changes states. A JK flip-flop provides one form of synchronous SET or RESET.

A: CIRCUIT



B: WAVEFORMS

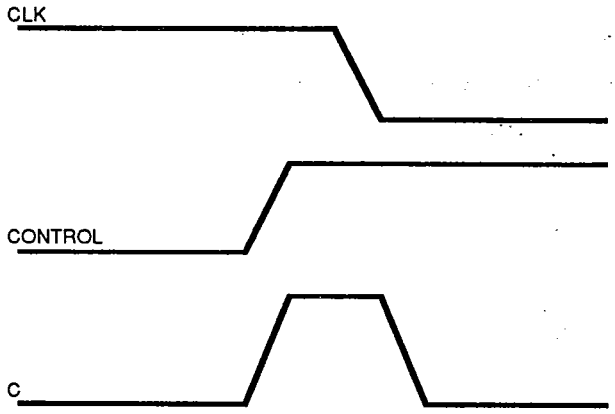
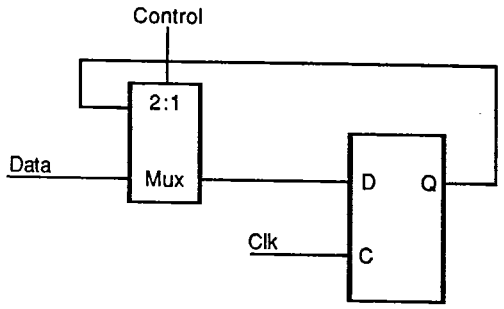
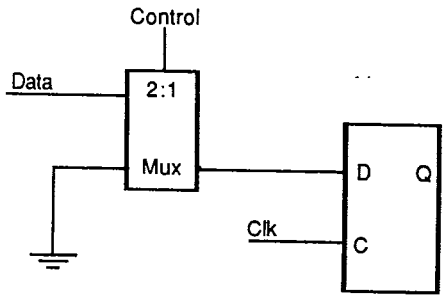


Figure 4–1. Gated Direct Action Signal Example



SYNCHRONOUS SHIFT AND HOLD



SYNCHRONOUS RESET

Figure 4–2. Synchronous Gating Circuit Examples

1.4.2 Clock Considerations

This section presents a collection of design considerations relating to clocked circuits. An ideal synchronous design has one system clock; that is, all clocked elements on the circuit should be clocked by the same signal. As the number of clocked elements increases, the number of clock drivers must increase too (see Figure 4–3).

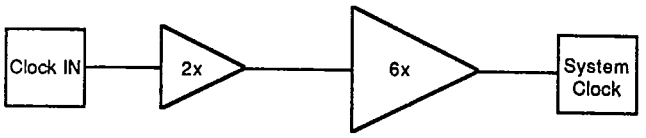


Figure 4–3. Typical Clock Driver

The main problem with this approach is the hold time specification for the data the clock is expected to capture due to the delay through the clock driver. Should such a problem arise, we recommend the solution illustrated in Figure 4–4. If the latch is transparent while CLK is low, when CLK asserts itself the latch will capture the input data and the hold-time requirement will be satisfied.

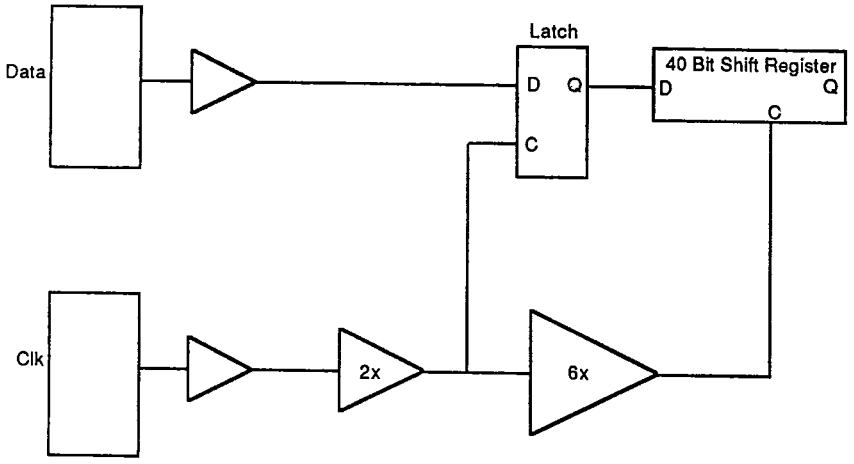


Figure 4–4. Typical Clock Driver with Latch

Clock pulse-width and duty-cycle are also important considerations. A low-frequency, low duty-cycle clock has many of the same design problems as does a high-frequency even duty-cycle clock. Gould recommends a 45 to 55 percent duty cycle.

If a flip-flop is exposed to a very slowly changing clock waveform, both the master and the slave sections of the flip-flop might be on simultaneously. To avoid this problem, maintain a maximum ratio of 12 loads per single clock driver (e.g., IN01).

The load on a flip-flop can affect the minimum pulse width of its clock. As the load increases, the required pulse-width increases. If a flip-flop is driving a load where C to Q delay is equal to or greater than the minimum clock pulse width it should be buffered (see Figure 4–5).

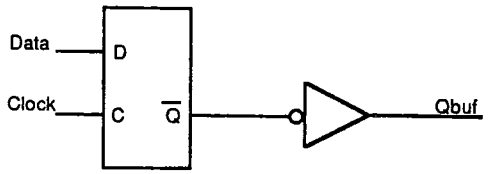


Figure 4–5. Buffered Flip-Flop Output Circuit

1.4.3 Avoid Analog Delays

Avoid using analog delays to "match" paths across a circuit. Analog delay is very hard to predict. Variations on the order of eight to one (with process, temperature and voltage variations) are not uncommon. "Pipelining" (inserting clocked flip-flops) is an effective way to balance long paths; that is, the design can usually accommodate additional levels of delay (in increments of the system clock period) to keep various control and data signals synchronized.

1.5 SIMULATION AND THE STANDARD TEST

Before the discussion of test and simulation for testing begins there are a couple of points that need to be understood.

Gould SCD uses Sentry VII and Sentry 21 series testers to test its gate array products. While this equipment effectively and efficiently evaluates the product, it can be a different environment than the parts will be exposed to in the application. Handlers, long cables and pin electronics loading are unique to the test environment. To appreciate the rigor of the production test scenario, contrast this with the printed circuit board where ground planes, local capacitive decoupling and very short distances minimize the noise environment the part is exposed to in its application .

Remember a test simulation is not a system simulation. A system simulation demonstrates that the gate array behaves as required in the kinds of situations it will encounter in its application, A test simulation demonstrates that all of the devices on the gate array are in place and operational and the array meets the Standard Test Specification. The better the design and test patterns the more efficiently this can be done.

1.5.1 The Standard Test

Gould uses the Standard Test on finished parts to verify certain basic parameters of the manufacturing process. The Standard Test is the means by which Gould can determine whether the manufactured product meets the Standard Test Specification. Figure 5–1 outlines the items in the Standard Test. The Gould Standard Test is much like standard test for discrete components. Off the shelf TTL components are tested to a set of specifications that are unrelated to the application. For example, VIHmin in TTL parts is tested at 2.0V, even though the targeted application may use a different value. Using a single value as this is a compromise; since the part can't be tested for all values, a representative value is chosen and used consistently in the Standard Test. The Standard Test is designed to assure the customer that the gate array is functionally correct and that all of the electrical parameters (DC and AC) are correct.

As an example, the Gould gate array output buffers can be specified in an almost continuous range of currents and voltages. These gate arrays are expected to be used in a variety of applications, all requiring slightly different output performance specifications. However, the Standard Test approach specifies that all output buffers are tested to the same requirements (VOL/IOL, VOH/IOH). Hence the Standard Test proves the manufacturing process rather than the application.

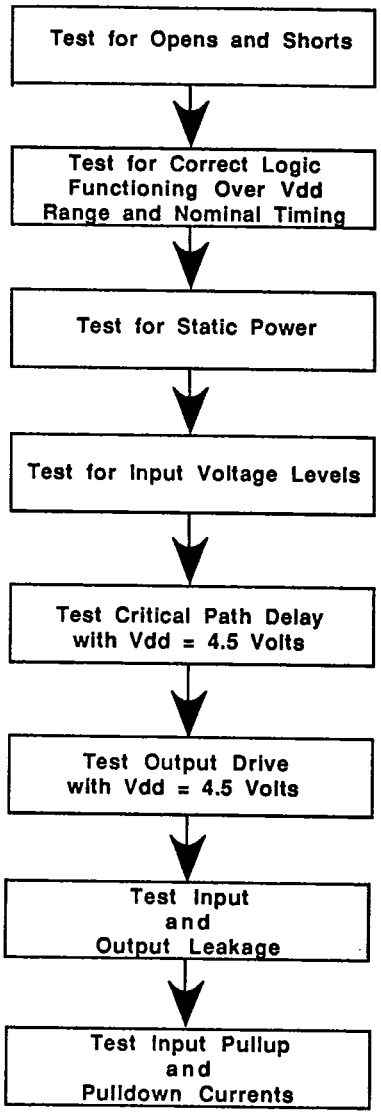


Figure 5–1. Definition of Standard Test

1.5.1.1. The Standard Test Specification

The Standard Test Specification contains important information for customers and about the part itself. The customer also has input to the Spec.

- screening requirements
- revision page/customer approval
- applicable documents
- marking and package information
- circuit description/block diagram
- operating specifications
- package pin definitions
- input and output parametrics
- timing requirements
- standard electrical test method
- any nonstandard testing requirements (e.g., burn-in)

This document is signed and approved by the customer and Gould prior to the start of the project. A tutorial that describes the Standard Test Specification is provided in Chapter 6.

1.5.1.2. The Test Program

A test program is a collection of input and output patterns supported by control statements. Four types of patterns are required to create a test program:

- *Functional Pattern* - Input vectors (i.e., truth table) used to verify that the device logic is correct.
- *Static Idd Pattern* - Input vectors used to setup the device for Idd measurement
- *Input Parametric Pattern* - Input vectors used to setup the device for input voltage testing and tristate leakage test.
- *Output Parametric Pattern* - Input vectors used to setup the device for output voltage testing.

The Static Idd, Input Parametric and Output Parametric Patterns must be less than 200 vectors.

1.5.2 The Functional Test

The functional test is specific to the application. The customer supplies a set of input waveforms in the form of test patterns or vectors. Usually these are the same waveforms used in the simulation of the part during the design process. Gould uses these patterns and the expected outputs to verify the correct functioning of the finished gate array parts. The function of the circuit is defined by the functional patterns.

1.5.2.1. Creating a Functional Test

Many engineers find it useful to create a formal flowchart of the functional test. Such a flowchart should describe the sections of logic to be tested and the order of the test. The test tactic for each section should be summarized. Testing the logic in sections makes it easier to design a thorough test.

Testing all possible input combinations is usually impractical. A better strategy is to find a set of input vectors that exercises all the logic without going through all possible inputs. The examples in Table 5–1 show two sets of test vectors for a 4-input NAND gate.

When creating a test program, limit the number of test vectors to 3 sets of 4,000 clock cycles. Each set must include an initialization sequence of 100 vectors or less to put the part into a known state.

The design process is inherently top-down; in contrast, developing test patterns is bottom-up. The lowest levels in the design hierarchy are simulated first. Once the operation of these modules has been verified, the test moves to the next level in the hierarchy, continuing this way until the highest level in the design is reached.

A complete simulation of the final design is done using timing and three device conditions worst case, nominal, and best case. The output of these simulations is compared for any differences. Different outputs should be reviewed for marginal or incorrect logic design. See Chapter 4, "Avoiding Design Problems." Worst case is defined as 80°C, 4.5 V, and Kp = 1.4. Best case is 0° C, 5.5 V, and Kp = 0.5.

Table 5–1
EXAMPLES OF TESTS
FOR 4–INPUT NAND GATE

Excessive Test		Good Test
0000	1000	1111
0001	1001	0111
0010	1010	1011
0011	1011	1101
0100	1100	1110
0101	1101	
0111	1111	

1.5.2.2. Inputs and Outputs

There are five basic input types allowed. The input types are:

Type 1:	NRZ
Type 2:	Delayed NRZ
Type 3:	Return-to-Zero (RZ)
Type 4:	Return-to-One (RTO)
Type 5:	Exclusive-NOR (XNOR)

Note that all the input types are specified relative to T0, the time base established for the test program. The delay (d) and the width (w) parameters are fixed for a given input. However, they may be different for different inputs. See figure 5–2 below for signal waveforms, which also appears in the Standard Test Specification.

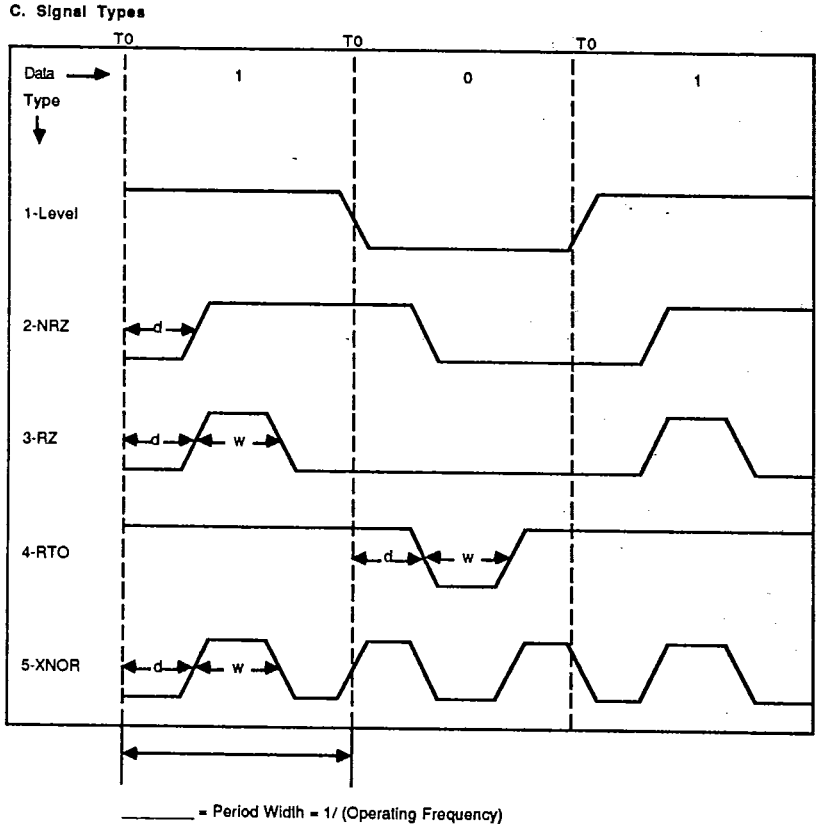


Figure 5–2. Allowable Input Types

Input vectors are signals that are applied to the input pins of the part for test. During each cycle, the input pins are updated to the current value and the outputs are strobed. For each input pin, the Standard Test Specification file defines where in the cycle transitions can occur.

Output transitions are determined by the network and by input timing. A maximum of one transition per T0 per output should be observed. The tester strobes the output once relative to T0, at the end of the cycle. If there are multiple transitions per T0 on an output, only the last transition is recorded; all others are ignored. All outputs are tested with a 50 pF capacitive load. System simulations requiring capacitive loads is discussed in the appropriate workstation Users Guide.

1.5.2.3. Requirements of All Patterns

The following requirements are to ensure compatibility between the customer's submitted vectors and the testers used at Gould. Because of noise considerations, the tester tests the device at a speed that is 10 times slower than the operating frequency. In the following requirements, all period, delay, width, and strobe values are with respect to the operating frequency.

General requirements are as follows:

1. The periods, widths and delays must all fit within *one* of the following ranges:

Range	Period	Width of Delay or Strobe
A	10ns - 4.095µs	1ns - 1.023µs
B	100ns - 40.95µs	10ns - 10.23µs
C	1µs - 409.5µs	100ns - 102.3µs
D	10µs - 4.095ms	1µs - 1.023ms

2. IO signals must follow the input signal requirements when in input mode and the output signal requirements when in output mode.

Requirements for input signals are as follows: (Refer to figure 5–2)

1. Delay (d) must be at least 1ns.
2. Delay (d) plus width (w) plus 1ns must be less than the period.
3. Input signals must be 0 or 1.
4. Level signals must only have transitions on period boundaries.
5. NRZ input transitions may only occur at the period boundary plus delay (d).
6. RZ input transitions to 1 may occur at the period boundary plus delay (d).
7. RZ input transitions to 0 may only occur at the period boundary plus delay (d) plus width (w).

8. RTO input transitions to 0 may only occur at the period boundary plus delay (d).
9. RTO input transitions to 1 may only occur at the period boundary plus delay (d) plus width (w).
10. There must be six or fewer input types. A type is a combination of the signal type and associated timing. For example: Two inputs, both NRZ, one having a delay (d) of 30ns and the other having a delay (d) of 40ns, would be two input types.
11. Width (w) must be at least 2ns.
12. XNOR inputs must only transition at every period boundary plus delay (d) or at every period boundary plus delay (d) plus width (w).
13. XNOR inputs may only transition at the period boundary.

Requirements for output signals are as follows:

1. Output signals may only transition once per period.
2. The same strobe point must be used on all outputs.
3. The strobe must start at least 1ns into the period and at least 3.0ns away from the end of the period.
4. TSO (tristate outputs) must have a control signal.
5. TSO may only be 0, 1, or Z when disabled. (Check at strobe time.)
6. TSO may only be 0, 1 or X when enabled. (Check at strobe time.)

1.5.2.4. I/O Control Signals

The signals that control the reading and driving of a device's bidirectional I/O pins (IO Control Node Name, page 7 of the Standard Test Specification, Appendix A) must be included in all patterns. To generate these control signals it is normally sufficient to capture the control nodes when the simulations for the various required patterns are run. The name and polarity of the IO Control Node must be identified in the Standard Test Specification.

1.5.2.5. Similar Conventions

Gould accepts test patterns from a variety of workstations. To ensure a usable set of patterns, the following conventions must be followed.

1. Submit Input Functional Patterns in a Print On Charge, time value format.
2. Submit Output Functional Patterns in a strobed, clock-value format (set strobe 3.0ns before end of clock cycle).

3. Provide consistent input definition of patterns:

   - One [d,w] per input per pattern
   - One output transition per T0

The workstation user's guide details the actual files needed for these patterns. Gould converts the patterns to cycle-based format during the resimulation of the circuit at the factory. The utility that converts the patterns also checks them for consistent input definition and multiple output transitions.

1.5.2.6. Specific Functional Pattern Requirements

In addition to the general requirements discussed above, the following requirements and constraints must be included in the Functional Test Pattern:

1. It must be possible to initialize timing chains, long counters that have no intermediate outputs and all memory elements. To illustrate this, consider the flip-flop that is inserted to generate a system clock. If it cannot be reset, a special test program routine must be written to test this circuit. Since the routine is not a feature of the Gould automatic test program development software, it becomes an effort that increases test development time and cost.

2. Gould prefers to use input vectors that toggle each node in the circuit at least once. We define toggling of the node to mean starting at zero or one and changing to the opposite state and back again.

3. The simulation is done using nominal conditions and operating at the system frequency.

1.5.3 Patterns for Parametric Measurements

The Static Idd Pattern, the Input Parametric Pattern and the Output Parametric Pattern are used to setup the part for various measurements. Each of these patterns is limited to 200 vectors.

1.5.3.1. Static Idd Pattern

The static Idd Pattern must insure that there are no floating nodes in the device when Idd/standby current is measured. All inputs are driven high (Vdd) or low (Vss) to place the device in a quiescent state for measurement of leakage and power consumption. Pins with pull-up inputs should be left floating. Pins with pull-downs should be driven low. Tristate output pins should be tristated. An internal tristate node should be driven by only one device. Bidirectional pins should be defined as inputs and driven high or low.

This pattern is also used to test the tristate and bidirectional output buffer leakage currents. The pattern must put the part in a state that allows for the measurement of these currents.

1.5.3.2. Input Parametric Pattern

The Input Parametric Pattern (VIL/VIH) measures input levels. For each input transition it is possible to directly observe the results at an output. A test circuit like that shown in either Figure 5–3, Figure 5–4, or Figure 5–5 makes the development of this pattern straight forward.

1.5.3.3. Output Parametric Pattern

The Output Parametric Pattern (VOL/VOH) measures output voltage and current levels. All outputs must transition to both logic states. A separate pattern is not needed if the first functional pattern places each output in both a "1" and "0" state.

1.5.3.4. Propagation Delay Path Selection

Gould tests the AC performance of its gate arrays by testing a single output against expected performance rather than against a customer's system or component requirement. If the network has been validated after layout with a logic simulation that takes into account actual loading and path delays, verifying one path is sufficient to ensure that all paths have the correct propagation delay.

The quality of the AC measurement is virtually independent of the output pin selected. Some applications have paths that are critical and many customers prefer to name these pins as the ones tested during the AC test.

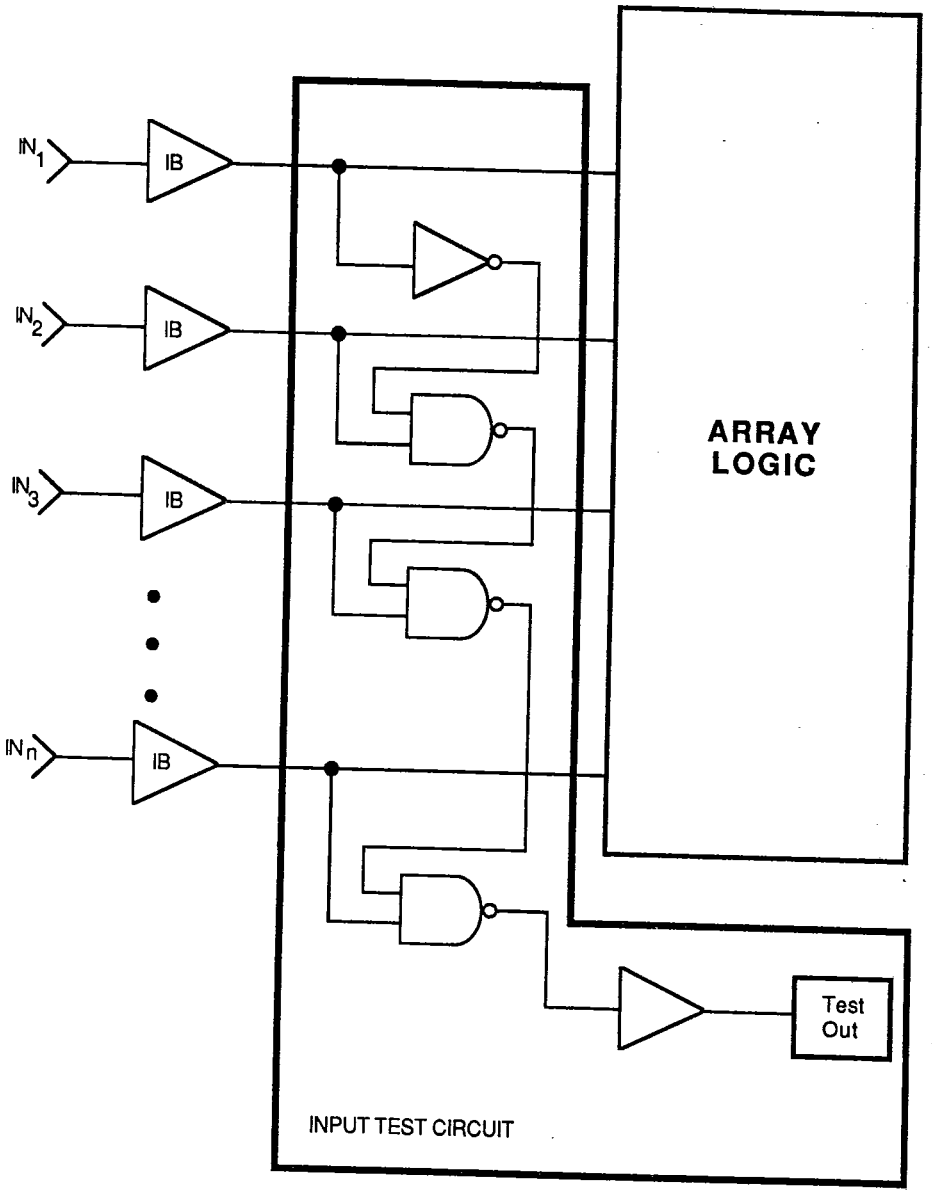


Figure 5–3 VIH and VIL Test Circuit

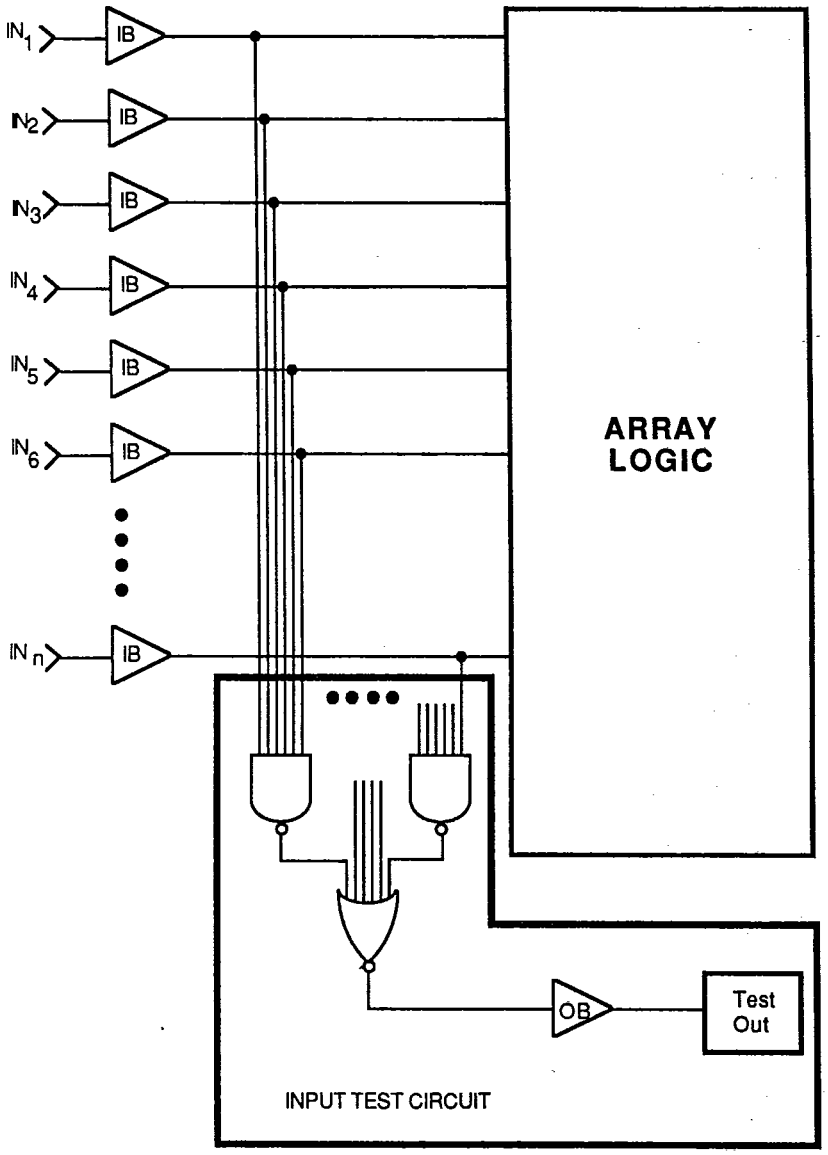


Figure 5-4 VIH and VIL Test Circuit

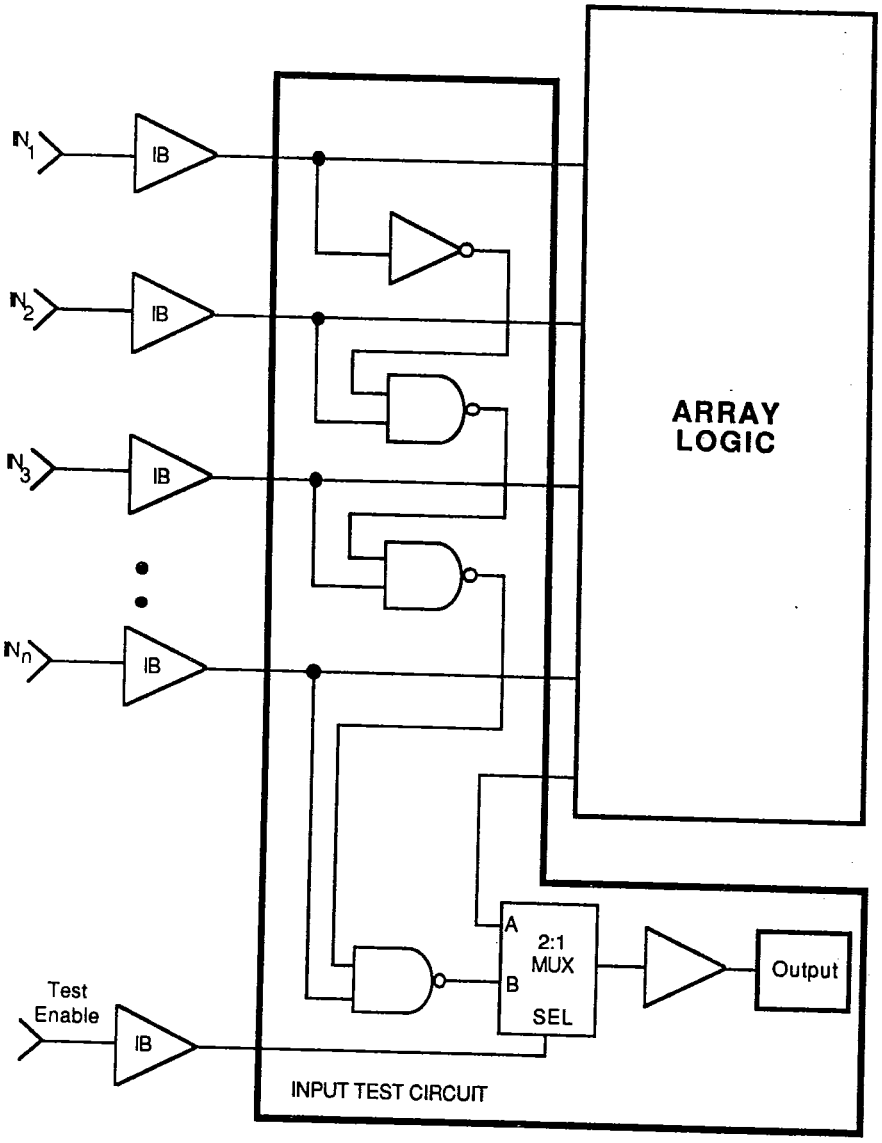


Figure 5-5 VIH and VIL Test Circuit With no Unused PKG Pins

1.6 TUTORIALS

The test specification is the primary communication link between a customer and Gould. To enhance this communication, Gould has established a format for the specification (Chapter 7).

In addition Gould has developed the Start Package Checklist to insure that your development begins on time. This checklist defines the deliverables for a given interface.

The next two sections introduce the Standard Test Specification Form and the Start Package Checklists.

1.6.1 Using the Gould Standard Test Specification

This form represents the format for the data required for a standard design workflow. Any departure from this format usually involves a nonstandard workflow and-consequently-extra cost. The following is a section-by-section explanation of items in the format:

Cover Sheet

The cover sheet contains the fundamental project identification information. It also has spaces for approval signatures of authorized individuals in both the customer's and vendor's organizations. The cover sheet also contains space for revision control of the specification.

I. PURPOSE

This section is self-explanatory.

II. APPLICABLE DOCUMENTS

All documents that are included in the specification (by reference) must be listed here. Applicable documents include logic diagram, netlist, test vector files, etc. All referenced documents must accompany the specification (unless previously on file with Gould Semiconductors) and are subject to acceptance by Gould. Inclusion of general, military or other specification constitutes a nonstandard workflow and will need to be quoted by Gould engineering.

III. SCREENING REQUIREMENTS

The screening described in this section represents the normal screening of devices manufactured by Gould. Any departure from this screening (burn-in, etc.) constitutes a nonstandard workflow and will need to be quoted by Gould engineering.

IV. PHYSICAL CHARACTERISTICS

This section will contain information about package type(s) and leadcounts, as well as marking, for the device. Normally, only one package type and leadcount will be specified; however, provision is made for additional packaging options where necessary.

V. CIRCUIT DESCRIPTION

A. Functional Description

This space is intended for the customer's description of the functional performance of the device. This description should be brief and in somewhat general terms.

B. Block Diagram

This space is provided for the inclusion of a block diagram of the circuit. When this block diagram exists as another document (for example, the top level of a hierarchical logic diagram) it may be included here by reference.

VI. OPERATIONAL SPECIFICATION

A. Absolute Maximum Ratings

This section represents the absolute maximum conditions for the environment of a Gould device. No changes or additions by the customer are allowed.

B. Operating Conditions

In this chart, the customer is to present the operating conditions under which the device will be expected to perform. As with Absolute Maximum Ratings many of the conditions are predefined.

VII. ELECTRICAL SPECIFICATIONS

A. Package Pin Definition

The notes make this section reasonably self-explanatory. Note that Gould prefers that the customer specify pinout, and it is helpful if the pin-number sequence is in numerical order.

B. Parametric Voltage and Current Levels.

The charts in this section (one each for inputs,outputs and bidirectionals) define parameters of the interface circuits of various types that can be used in the design of the circuit. The values *are not* subject to negotiation or change.

C. Signal Types as defined in section VII part C of the specification.

VIII. STANDARD ELECTRICAL TEST

This section describes the standard electrical test in abbreviated form and provides the means by which functional test ground rules are incorporated into the specification.

IX. FUNCTIONAL TEST DESCRIPTION

In this space, the customer provides a description of the functional test patterns listed in section II of the Standard Test Specification.

1.6.2 Using the Gould Start Package Checklists

When sending your design and Standard Test Specification to Gould, be sure to include the appropriate start package checklist, (Chapter 8). There are checklists available for the various interfaces for Gould gate array and cell based circuits. These will enable Gould to start your development and deliver your prototypes on time.

Your deliverables are checked and validated by Gould before any development work begins. A schedule for the shipment of prototypes is made after successful completion of the validation process. *The checklist is as important as the test specification and simulation files for getting your circuit developed on time.*

In using the checklist, only fill out the front side. The reverse side is for Gould internal use only. Some of the following explanation may not be applicable to all checklists.

General Information

Fill in your company name and the feature size defining a technology. The customer device number is your own internal number or name which you have assigned to the part.

Customer Supplied Data

Each item requested in this section must be supplied. Please list the file names and revisions (if revision is not applicable list the date last updated). You may have up to 3 functional patterns, each individually initialized and less than 4000 clock cycles. The Static Idd, Input Parametric and Output Parametric patterns must be included and consist of less than 200 vectors each.

Data Medium

Please check the appropriate box for the medium you are using to transfer your data to Gould. If you are using magnetic tape, it must be 1600 BPI and you need to record the record length and blocking factor.

Authorized Customer Representative(s)

Fill in the names and addresses of the technical and administrative contacts.

The completed checklist and associated data should be delivered to a Gould representative.

1.7

STANDARD TEST SPECIFICATION FORM

1

Standard Test Specification for a Gould 1.25µ Double Metal Gate Array Device

REVISIONS			Customer
Revision	Description of Change(s)	Date	Approval

Gould Approval		Customer Approval		
Signature	Des Engr	Signature	Des Engr.	Date
Signature	Test Engr	Signature	Buyer	Date
Signature	Dept Mngr	Signature	Other	Date
Project Name (If Applicable)		Customer		
Gould Device #		Customer Document #	(Customer	

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1.25µ Double-Metal HCMOS Gate Arrays

I. PURPOSE

The purpose of this specification is to define the mechanical, environmental and electrical characteristics for integrated circuits supplied by Gould Electronics. All parts which comply with this specification shall be considered to meet the customer's requirements. Any parameter left undefined will be processed according to Gould Electronics' normal quality control standards.

This document is intended to take precedence over applicable customer documents. Once signed by the customer and Gould Electronics, no changes may be made without written consent by the customer and Gould Electronics.

1

II. APPLICABLE DOCUMENTS

Applicable documents shall include test patterns which are in Gould Electronics format (see design manual), all other documents are subject to approval by Gould Electronics.

	Name	Revision
Functional pattern(s)		
	_____	_____
	_____	_____
	_____	_____
Static Idd pattern	_____	_____
Input parametric pattern	_____	_____
Output parametric pattern	_____	_____
Netlist	_____	_____

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III. SCREENING REQUIREMENTS

Screening is done in accordance with the applicable product flow which typically includes the following:

A. Perform standard electrical test on wafers.

B. Precap visual inspection.

C. Temperature cycle, -65°C ± 2°C to 150°C ± 2°C, 5 cycles.

(PPGA -40°C ± 2°C to 90°C ± 2°C,)

D. Seal, gross leak (cavity packages only).

E. External visual.

F. Perform standard electrical test (see section VIII) on packaged assemblies.

G. QA lot acceptance sampling

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IV. PHYSICAL CHARACTERISTICS

A. Package type(s):

_____

B. Package lead count(s):

_____

C. Package marking will be the following:

***M* AMI XXXXYZZ**
Cnnnnnn

_____
_____

1

Where:

M is the mask works and will appear as shown, or as a letter M with a circle around it, AMI is the Gould Semiconductor (American Microsystems Inc) Logo, XXXXYZZ is the date and traceability code, Cnnnnnn is the Gould Electronics Marketing number (manufacture's option), and the blank lines left are for optional customer marking. Refer to the table below for maximum lines and letters/line available.

PLASTIC			CERAMIC		
Lead Count	Maximum # of Lines	Maximum Letters/Line	Lead Count	Maximum # of Lines	Maximum Letters/Line
DIP			DIP		
22	1	16	22-24	1	9
24-48	2	16	28-68	1	11
PCC			PCC		
28-44	2	8	22-24	1	9
68-84	5	16	28-84	1	11
PGA			PGA		
ALL	2	13	68-144	1	11

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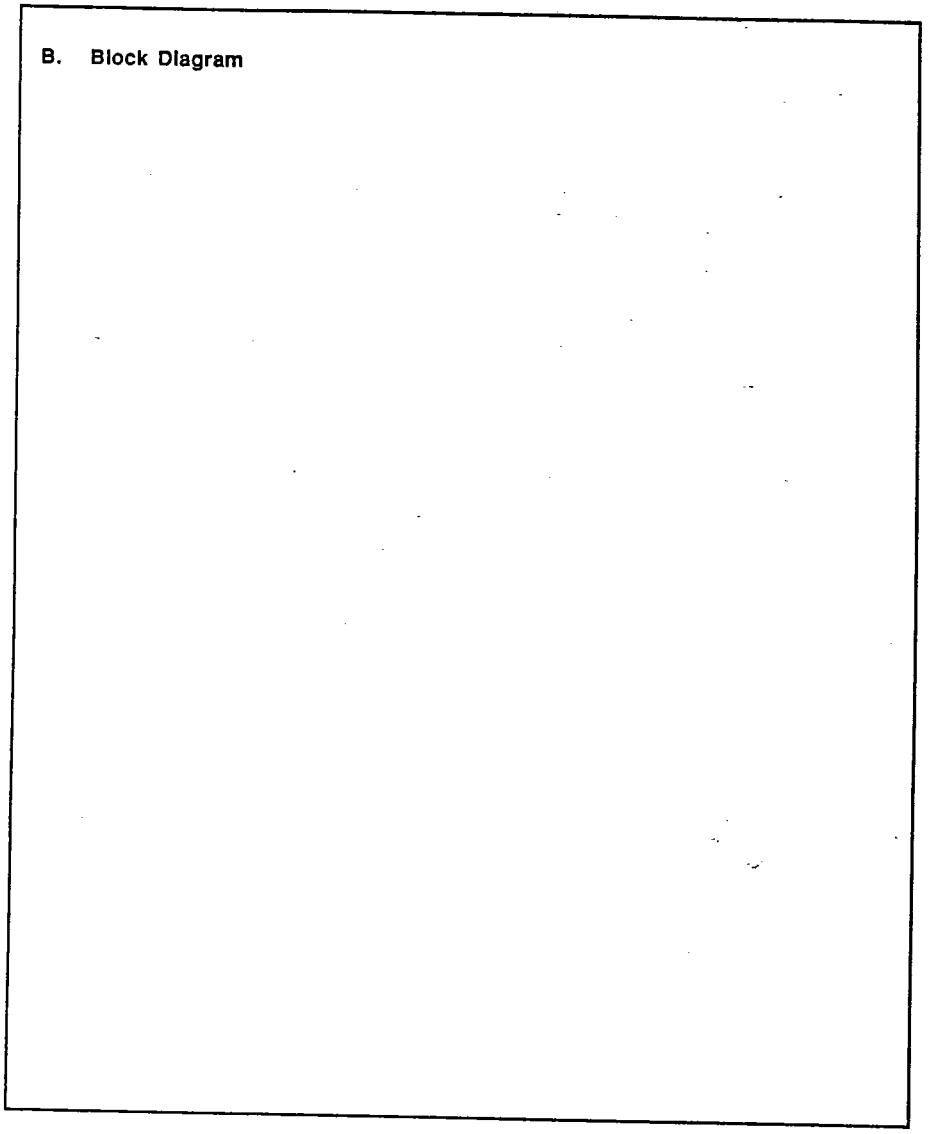
V. CIRCUIT DESCRIPTION

A. Functional Description

B. Block Diagram



VI. OPERATIONAL SPECIFICATIONS

A. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
Vdd	DC Supply Voltage	-0.3	7.0	V	
Vin	Input Pin Voltage	-0.3	Vdd+0.3	V	
Iin	Input Pin Current	-10.0	10.0	mA	25°C
Tstrg	Storage Temp (DIP/PCC)	-55	150	°C	
Tstrg	StorageTemp (PGA)	-40	90	°C	
Tlead	Lead Temperature		300	°C	10 Sec

B. Operating Conditions

Symbol	Parameter	Max	Min	Units	Notes
Vdd	DC Supply Voltage	5.5	4.5	V	(2)
Idd	Static Supply Current				(1)
Vss	Circuit Ground	0.0	0.0	V	
Ta	Ambient Temperature	70.0	0.0	°C	(2)

(1) Static Idd current is exclusive of input/output drive requirements and is measured with the clocks stopped and all inputs tied to Vdd or Vss, configured to draw minimum current, refer to section VIII.

(2) The input and output parametric values in section VII B, parts 1,2 and 3, are directly related to ambient temperature and DC supply voltage. A temperature range other than 0 to 70 °C or a supply voltage range other than 4.5 to 5.5 volts will affect these values and must be evaluated by Gould Electronics.

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VII. ELECTRICAL SPECIFICATIONS

A. Pin Definitions

Pin #	Name	I/O	Parametric Type	Signal Type	d (ns)	w (ns)	IO Control Node Name	Pol	Note
1									
2									
3									
4									
5									
6									
7									
8									
9									
10									
11									
12									
13									
14									

(3) Pin names should be alphanumeric and not exceed 8 characters.
(4) Pin designation: I = Input, O = Output, IO = Bidirectional, P = Power Pad.
(5) See part B of this section.
(6) See part C of this section. The columns SIGNAL TYPE, d, and w are for input pins or the input portion of IO pins only.
(7) IO Control is a node which controls the tester as an Input or Output for the IO pin. NA for non-IO pins. The IO Control node is externally generated and is of level signal type, see section VII-C.
(8) IO Control node Polarity. A '+' indicates when IO Control is a 1 the pin will be driven as an input and when IO Control is a 0 the pin will be treated as an output. A '-' is the opposite.

(Pin Definitions Continued)

Pin #	Name	I/O	Parametric Type	Signal Type	d (ns)	w (ns)	IO Control Node Name	Pol	Note
15									
16									
17									
18									
19									
20									
21									
22									
23									
24									
25									
26									
27									
28									
29									
30									
31									
32									
33									
34									
35									
36									

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(Pin Definitions Continued)

Pin #	Name	I/O	Parametric Type	Signal Type	d (ns)	w (ns)	IO Control Node Name	Pol	Note
37									
38									
39									
40									
41									
42									
43									
44									
45									
46									
47									
48									
49									
50									
51									
52									
53									
54									
55									
56									
57									
58									

1

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(Pin Definitions Continued)

Pin #	Name	I/O	Parametric Type	Signal Type	d (ns)	w (ns)	IO Control Node Name	Pol	Note
59									
60									
61									
62									
63									
64									
65									
66									
67									
68									
69									
70									
71									
72									
73									
74									
75									
76									
77									
78									
79									
80									

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B. Parametric Voltage and Current Levels

(1.25µm Gate Array, Parametric revision 1.00)

Ambient Temperature = 0-70° C

1. INPUTS:

Type	Vil	Vih	Iil(9) Min	Iil(9) Max	Iih(10) Min	Iih(10) Max	Note
IBA	0.3Vdd	0.7Vdd	NA	-1.0µA	NA	1.0µA	CMOS (10a)
IBB	0.3Vdd	0.7Vdd	-60µA	-300µA	NA	NA	CMOS with pullup
IBC	0.3Vdd	0.7Vdd	NA	NA	30µA	130µA	CMOS with pulldown
IBD	0.8V	2.0V	NA	-1.0µA	NA	1.0µA	TTL (10a)
IBE	0.8V	2.0V	-60µA	-300µA	NA	NA	TTL with pullup
IBF	0.8V	2.0V	NA	NA	30µA	130µA	TTL with pulldown
IBG	See Data Below		NA	-1.0µA	NA	1.0µA	CMOS Schmitt Trigger (10a)
IBH	See Data Below		NA	-1.0µA	NA	1.0µA	TTL Schmitt Trigger (10a)

(9) Iil is tested at Vdd = 5.5 Volts and Vin = 0 Volts.
(10) Iih is tested at Vdd = 5.5 Volts and Vin = 5.5 Volts.
(10a) Input leakage is not tested at temperatures below room ambient.

		CMOS Schmitt Trigger Input Data	
Type	Characteristic	Minimum	Maximum
IBG	Negative-Going Threshold Vt-	1.2V	
	Positive-Going Threshold Vt+		4.2V
	Hysteresis	1.0V	

		TTL Schmitt Trigger Input Data	
Type	Characteristic	Minimum	Maximum
IBH	Negative-Going Threshold Vt-	0.7V	
	Positive-Going Threshold Vt+		2.1V
	Hysteresis	0.3V	

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(Parametric Voltage and Current Levels Continued)

(1.25µm Gate Array, Parametric revision 1.00)

Ambient Temperature = 0-70° C

2. OUTPUTS:

Type	Vol	Voh	Iol (12)	Ioh (13)	Ioz (14)	Note
OBZ	0.4V	2.4V	4mA	-4.0mA	NA	Single Power (SP)
OBY	0.4V	2.4V	8mA	-8.0mA	NA	Double Power (DP)
OBX	0.4V	2.4V	4mA	-4.0mA	±10µA	SP, Tristate
OBW	0.4V	2.4V	8mA	-8.0mA	±10µA	DP, Tristate
OBV	NA	2.4V	NA	-4.0mA	-10µA	SP, Open Drain P (11)
OBU	NA	2.4V	NA	-8.0mA	-10µA	DP, Open Drain P (11)
OBT	0.4V	NA	4mA	NA	+10µA	SP, Open Drain N (11)
OBS	0.4V	NA	8mA	NA	+10µA	DP, Open Drain N (11)
OBR	0.4V	2.4V	2.0mA	-2.0mA	NA	Half Power
OBQ	0.4V	2.4V	1.0mA	-1.0mA	NA	Quarter Power
OBP	0.4V	2.4V	0.65mA	-.65mA	NA	Seventh Power
OBN	0.4V	2.4V	2.0mA	-2.0mA	±10µA	Half Power , Tristate
OBM	0.4V	2.4V	1.0mA	-1.0mA	±10µA	Quarter Power, Tristate
OBL	0.4V	2.4V	0.65mA	-.65mA	±10µA	Seventh Power, Tristate

(11) At test time a 1.5k ohm resistor is tied to Vdd or Vss on open drain devices to force a signal level when the device is in a high-impedance state.
(12) Vol, Iol are tested at Vdd = 4.5 Volts.
(13) Voh, Ioh are tested at Vdd = 4.5 Volts.
(14) Ioz is tested with Vdd = 5.5 Volts.

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(Parametric Voltage and Current Levels Continued)

(1.25µm Gate Array, Parametric revision 1.00)

Ambient Temperature = 0-70° C

3. BIDIRECTIONALS:

Type	Vil	Vih	Vol	Voh	Iol (15)	Ioh (16)	Ioz min (17)	Ioz max (17)	Note
BAL	0.3Vdd	0.7Vdd	0.4V	2.4V	0.65mA	-0.65mA	-10µA	10µA	.65mA CMOS IO
BAM	0.3Vdd	0.7Vdd	0.4V	2.4V	1.0mA	-1.0mA	-10µA	10µA	1mA CMOS IO
BAN	0.3Vdd	0.7Vdd	0.4V	2.4V	2.0mA	-2.0mA	-10µA	10µA	2mA CMOS IO
BAW	0.3Vdd	0.7Vdd	0.4V	2.4V	8.0mA	-8.0mA	-10µA	10µA	8mA CMOS IO
BAX	0.3Vdd	0.7Vdd	0.4V	2.4V	4.0mA	-4.0mA	-10µA	10µA	4mA CMOS IO
BBX	0.3Vdd	0.7Vdd	0.4V	2.4V	4.0mA	-4.0mA	-60µA	-310µA	4mA CMOS w/pu IO
BBW	0.3Vdd	0.7Vdd	0.4V	2.4V	8.0mA	-8.0mA	-60µA	-310µA	8mA CMOS w/pu IO
BCX	0.3Vdd	0.7Vdd	0.4V	2.4V	4.0mA	-4.0mA	30µA	140µA	4mA CMOS w/pd IO
BDL	0.8V	2.0V	0.4V	2.4V	0.65mA	-0.65mA	-10µA	10µA	.65mA TTL IO
BDM	0.8V	2.0V	0.4V	2.4V	1.0mA	-1.0mA	-10µA	10µA	1mA TTL IO
BDN	0.8V	2.0V	0.4V	2.4V	2.0mA	-2.0mA	-10µA	10µA	2mA TTL IO
BDW	0.8V	2.0V	0.4V	2.4V	8.0mA	-8.0mA	-10µA	10µA	8mA TTL IO
BDX	0.8V	2.0V	0.4V	2.4V	4.0mA	-4.0mA	-10µA	10µA	4mA TTL IO
BEW	0.8V	2.0V	0.4V	2.4V	8.0mA	-8.0mA	-60µA	-310µA	8mA TTL w/pu IO
BEX	0.8V	2.0V	0.4V	2.4V	4.0mA	-4.0mA	-60µA	-310µA	4mA TTL w/pu IO

(15) Vol, Iol are tested at Vdd = 4.5 Volts
(16) Voh, Ioh are tested at Vdd = 4.5 Volts.
(17) Ioz is tested with Vdd = 5.5 Volts.

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(Parametric Voltage and Current Levels Continued)

(1.25µm Gate Array, Parametric revision 1.00)

Ambient Temperature = 0-70° C

3. BIDIRECTIONALS (continued):

Type	Vil	Vih	Vol	Voh	Iol (15)	Ioh (16)	Ioz min (17)	Ioz max (17)	Note
BGL	See Type IBG		0.4V	2.4V	0.65mA	-0.65mA	-10µA	10µA	.65mA Schmitt IO
BGM	See Type IBG		0.4V	2.4V	1.0mA	-1.0mA	-10µA	10µA	1mA Schmitt IO
BGN	See Type IBG		0.4V	2.4V	2.0mA	-2.0mA	-10µA	10µA	2mA Schmitt IO
BGW	See Type IBG		0.4V	2.4V	8.0mA	-8.0mA	-10µA	10µA	8mA Schmitt IO
BGX	See Type IBG		0.4V	2.4V	4.0mA	-4.0mA	-10µA	10µA	4mA Schmitt IO
BG1	See Type IBG		0.4V	2.4V	4.0mA	-4.0mA	-60µA	-310µA	4mA Schmitt w/pu
BG2	See Type IBG		0.4V	2.4V	8.0mA	-8.0mA	-60µA	-310µA	8mA Schmitt w/pu
BG3	See Type IBG		0.4V	2.4V	4.0mA	-4.0mA	30µA	140µA	4mASchmitt w/pd

(15) Vol, Iol are tested at Vdd = 4.5 Volts
(16) Voh, Ioh are tested at Vdd = 4.5 Volts.
(17) Ioz is tested with Vdd = 5.5 Volts.

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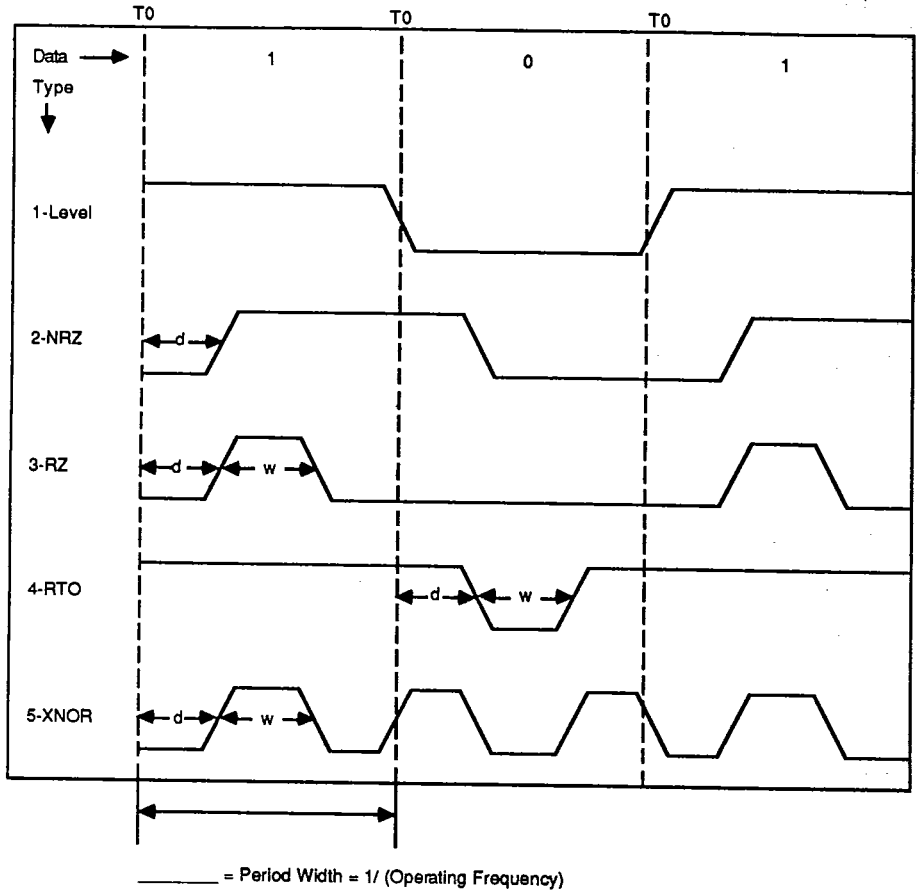
C. Signal Types



The period is selected in increments of 5ns with a minimum period of 50ns, up to 1µs.

VIII. STANDARD ELECTRICAL TEST

Functional Patterns: The functional test will be a maximum of three patterns containing less than 4096 vectors each. The functional test patterns will be tested at a minimum of one-tenth of the circuit operating frequency. Each pattern must be separately initialized in less than 100 vectors. The input timing, as defined in section VII part A, will be scaled accordingly and the outputs will be strobed at the end of the period. The input voltage levels are Vil ≤ 0.1Vdd and Vih ≥ 0.9Vdd. The output voltage levels are Vol ≤ 1.5V and Voh ≥ 1.5V. The functional patterns will be tested at both minimum and maximum Vdd.

AC Testing: One propagation delay path will be chosen by the customer and tested at a convenient frequency (on one edge) determined by Gould Electronics. The transition on the pin will only be measured from the rising or falling edge of the second transition of the pin. The output pin to be tested for delay should not be an open drain device since one edge would be driven by the device and the other by external circuitry. The pin to be tested is pin # ___.

The **propagation delay** will be measured from the period edge of the second transition on the pin. The delay is determined by simulation, not from a system specification of the application. The input voltage levels are Vil ≤ 0.1Vdd and Vih ≥ 0.9Vdd. The output voltage levels are Vol ≤ 1.5V and Voh ≥ 1.5V. The Vdd supply is at Vdd = Vdd_{min}. The AC load on the output pin is 50pF.

Static Idd: The static Idd will be tested at the last vector of the Static Idd pattern. The pattern will be less than 200 vectors and will cause the device to have no floating gates. All clocks will be stopped and all inputs tied to Vdd or Vss, configured to draw minimum current. Pins with pullups will be left floating and pins with pulldowns will be driven low. The Idd maximum must be adjusted to account for any input with pullups that must be pulled low.

Parametric Verification: As defined in section VII parts A and B of this specification. The input parametric pattern will test section VII, part B, section 1 and 3, and the output parametric pattern will test section VII, part B, section 2 and 3. Each pattern will be less than 200 vectors and will be initialized within 100 vectors..

Schmitt trigger testing: Specified input levels will be tested in one pass of the Input Parametric pattern. Hysteresis will be tested by using a binary regression routine to determine both threshold values, then subtracting Vt- from Vt+. These tests will be performed at minimum and maximum Vdd. The hysteresis test is performed on one representative buffer for each group of schmitt input types. In order to test hysteresis, there must be a direct Input to output relation for the representative cell via a Nand Tree or similar structure. If this is not possible, the hysteresis test feasibility will be reviewed during registration.

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IX. FUNCTIONAL TEST DESCRIPTION

The Functional Test Description is a customer supplied description of the simulation vectors. A well designed pattern set is a prerequisite to a reliable and comprehensive test. The following description is an overview of the functional pattern and is intended for reference only. The customer starts with the length of restart and continues from there.

Bit Times	Description
0– ___	Reset: place all internal nodes into a known state.

Document Rev. 1.00 Parametric Rev. 1.00

1.8

START PACKAGE CHECKLIST

Gate Array Start Package Checklist
Logic Input

General Information

Customer _____ Customer Device Number _____

Technology (1.25µm, 2µm, 3µm) _____

Customer Supplied Data

	Filename	Date or Rev.
☐ Schematic (Hard and Soft copies)		
☐ Vectors (Gould format, individually initialized, and less than 4000 clock cycles each)		
☐ Functional Patterns		
☐ Static Idd Pattern		
☐ Input Parametric Pattern		
☐ Output Parametric Pattern		
☐ Standard Test Specification		
☐ Hardcopy of tape/floppy directory filenames		

1

Data Medium (Workstation)

☐ 8" Floppy (Daisy, Mentor) ☐ 5.25" Floppy (PC Workstations)

☐ 0.5" 9-track ASCII Magnetic Tape (PRIME, VAX, Daisy, Mentor).

☐ 1600 BPI ☐ Record Length _____ ☐ Blocking Factor _____

Authorized Customer Representative(s)

	Technical Contact	Administrative Contact
Name		
Position		
Phone Number		
Mail Stop		
Address		
Signature		

Gould Electronics Use Only

Sales Representative _____

Marketing _____

	Approval	Date
Quote/NRE Validation (Eng Ops)		
Customer Information Received (Eng Ops)		
Work Statement (Eng Ops)		
Customer Information Validated (Des Eng)		
Proposed T0 Schedule (Eng Ops)		

Start Date Approval

All of the above information must be approved prior to the designation of the start date.

Start Date (T0)_____

	Approval	Date
Department Manager		
Design Engineering		
Test Engineering		

Gate Array Start Package Checklist
Semi-Validated Netlist Input

General Information

Customer _____ Customer Device Number _____

Technology (1.25µm, 2µm, 3µm) _____ Library Revision _____

Workstation Type _____ Netlister Revision _____

Operating System Revision _____

Customer Supplied Data

	Filename	Date or Rev.
☐ Schematic (Hard and Soft copies)		
☐ BOLT Netlist		
☐ Synonym table (Mentor)		
☐ Vectors (Gould format, individually initialized, and less than 4000 clock cycles each)		
☐ Functional Pattern(s)		
☐ Static Idd Pattern		
☐ Input Parametric Pattern		
☐ Output Parametric Pattern		
☐ Standard Test Specification		
☐ Design Log (Mentor)		
☐ Hardcopy of tape/floppy directory filenames		
☐ Package (Mentor)		

1

Data Medium (Workstation)

☐ 8" Floppy (Daisy, Mentor) ☐ 5.25" Floppy (PC Workstations)

☐ 0.5" 9-track ASCII Magnetic Tape (PRIME, VAX, Daisy, Mentor).

☐ 1600 BPI ☐ Record Length _____ ☐ Blocking Factor _____

Authorized Customer Representative(s)

	Technical Contact	Administrative Contact
Name		
Position		
Phone Number		
Mail Stop		
Address		
Signature		

Gould Electronics Use Only

Sales Representative _____

Marketing _____

	Approval	Date
Quote/NRE Validation (Eng Ops)	_____	_____
Customer Information Received (Eng Ops)	_____	_____
Work Statement (Eng Ops)	_____	_____
Customer Information Validated (Des Eng)	_____	_____
Proposed T0 Schedule (Eng Ops)	_____	_____

Start Date Approval

All of the above information must be approved prior to the designation of the start date.

Start Date (T0)_____

	Approval	Date
Department Manager	_____	_____
Design Engineering	_____	_____
Test Engineering	_____	_____

Gate Array Start Package Checklist
Functionally Validated Netlist Input

General Information

Customer _____ Customer Device Number _____

Technology (1.25µm, 2µm, 3µm) _____ Library Revision _____

Workstation Type _____ Netlister Revision _____

Operating System Revision _____

Customer Supplied Data

	Filename	Date or Rev.
☐ Schematic (Hard and Soft copies)		
☐ BOLT Netlist		
☐ Synonym table (Mentor)		
☐ Vectors (Gould format, individually initialized, and less than 4000 clock cycles each)		
☐ Functional Pattern(s)		
☐ Static Idd Pattern		
☐ Input Parametric Pattern		
☐ Output Parametric Pattern		
☐ Standard Test Specification		
☐ Design Log (Mentor)		
☐ Hardcopy of tape/floppy directory filenames		
☐ Package (Mentor)		

1

Data Medium (Workstation)

☐ 8" Floppy (Daisy, Mentor) ☐ 5.25" Floppy (PC Workstations)

☐ 0.5" 9-track ASCII Magnetic Tape (PRIME, VAX, Daisy, Mentor).

☐ 1600 BPI ☐ Record Length _____ ☐ Blocking Factor _____

Authorized Customer Representative(s)

	Technical Contact	Administrative Contact
Name		
Position		
Phone Number		
Mail Stop		
Address		
Signature		

Gould Electronics Use Only

Sales Representative _____

Marketing _____

	Approval	Date
Quote/NRE Validation (Eng Ops)	_____	_____
Customer Information Received (Eng Ops)	_____	_____
Work Statement (Eng Ops)	_____	_____
Customer Information Validated (Des Eng)	_____	_____
Proposed T0 Schedule (Eng Ops)	_____	_____

Start Date Approval

All of the above information must be approved prior to the designation of the start date.

Start Date (T0)_____

	Approval	Date
Department Manager	_____	_____
Design Engineering	_____	_____
Test Engineering	_____	_____

Gate Array Start Package Checklist
Database Input (Mentor Only)

General Information

Customer _____
Technology (1.25µm, 2µm, 3µm) _____
Workstation Type Mentor
Operating System Revision _____

Customer Device Number _____
Library Revision _____
Netlister Revision _____
Gate Station Revision _____

Customer Supplied Data

	Filename	Date or Rev.
☐ Schematic (Hard and Soft copies)		
☐ BOLT Netlist	CIRCUIT.BOLT	
☐ Synonym Table	BOLT.SYN	
☐ Geometrical Data File	DESIGN.DDF	
☐ Interconnect Load Capacitance File	NETPARM.DD	
☐ Vectors (Gould format, individually initialized, and less than 4000 clock cycles each)		
☐ Functional Pattern(s)	FUNC1.PAT	
	FUNC2.PAT	
	FUNC3.PAT	
☐ Static Idd Pattern	IDD.PAT	
☐ Input Parametric Pattern	INPUT.PAT	
☐ Output Parametric Pattern	OUTPUT.PAT	
☐ Simulator File	CIRCUIT_SIM	
☐ Plot of Pin Layout	CIRCUIT/PACKAGE	
☐ Design Log		
☐ Standard Test Specification		
☐ Hardcopy of tape/floppy directory filenames		
☐ Package (Mentor)		

1

Data Medium (Workstation)

☐ 8" Floppy
☐ 0.5" 9-track ASCII Magnetic Tape
☐ 1600 BPI ☐ Record Length _____ ☐ Blocking Factor _____

Authorized Customer Representative(s)

	Technical Contact	Administrative Contact
Name		
Position		
Phone Number		
Mail Stop		
Address		
Signature		

Gould Electronics Use Only

Sales Representative _____

Marketing _____

	Approval	Date
Quote/NRE Validation (Eng Ops)		
Customer Information Received (Eng Ops)		
Work Statement (Eng Ops)		
Customer Information Validated (Des Eng)		
Proposed T0 Schedule (Eng Ops)		

Start Date Approval

All of the above information must be approved prior to the designation of the start date.

Start Date (T0)_____

	Approval	Date
Department Manager		
Design Engineering		
Test Engineering		

Gate Array Start Package Checklist
Semi-Validated Netlist Input, Option - L

General Information

Customer _____ Customer Device Number _____

Technology (1.25µm, 2µm, 3µm) _____

Workstation Type _____ Operating System Revision _____

Customer Supplied Data (Reference current Gould Gate Array Design Manual)

(Filename(s) and Date or Rev. must be filled in.)

- ☐ Schematic (Hard copy) — Filename _____ Date or Rev. _____
- ☐ Tape/floppy directory (Hard copy)
- ☐ Synonym table (if needed)
- ☐ Standard Test Specification (Reference Chapter 6)

1

	Filename	Date or Rev.	Filename	Date or Rev.
☐ NDL or TDL Netlist				
☐ Vectors (Reference Chapter 5) Functional Pattern(s)				
Static Idd Pattern				
Input Parametric Pattern				

Data Medium (Specify which)

- ☐ 8" Floppy (Daisy, Mentor)
- ☐ 5.25" Floppy (IBM PC Format)
- ☐ 0.5" 9-track Magnetic Tape
  - ☐ 1600 BPI ☐ Record Length _____ ☐ Block Size _____ ☐ Format (ASCII, EBCDIC) _____

Authorized Customer Representative(s)

	Technical Contact	Administrative Contact
Name		
Position		
Phone Number		
Mail Stop		
Address		
Signature		

Gould Electronics Use Only

Sales Representative _____

Marketing _____

	Approval	Date
Quote/NRE Validation (Eng Ops)	_____	_____
Customer Information Received (Eng Ops)	_____	_____
Work Statement (Eng Ops)	_____	_____
Customer Information Validated (Des Eng)	_____	_____
Preposed T0 Schedule (Eng Ops)	_____	_____

Start Date Approval

All of the above information must be approved prior to the designation of the start date.

Start Date (T0)_____

	Approval	Date
Department Manager	_____	_____
Design Engineering	_____	_____
Test Engineering	_____	_____