



# E1-32XS

## RISC/DSP Processor

**A 32-Bit microcontroller design with an integrated RISC/DSP core architecture offering maximum power efficiency in portable multimedia and consumer electronics applications**

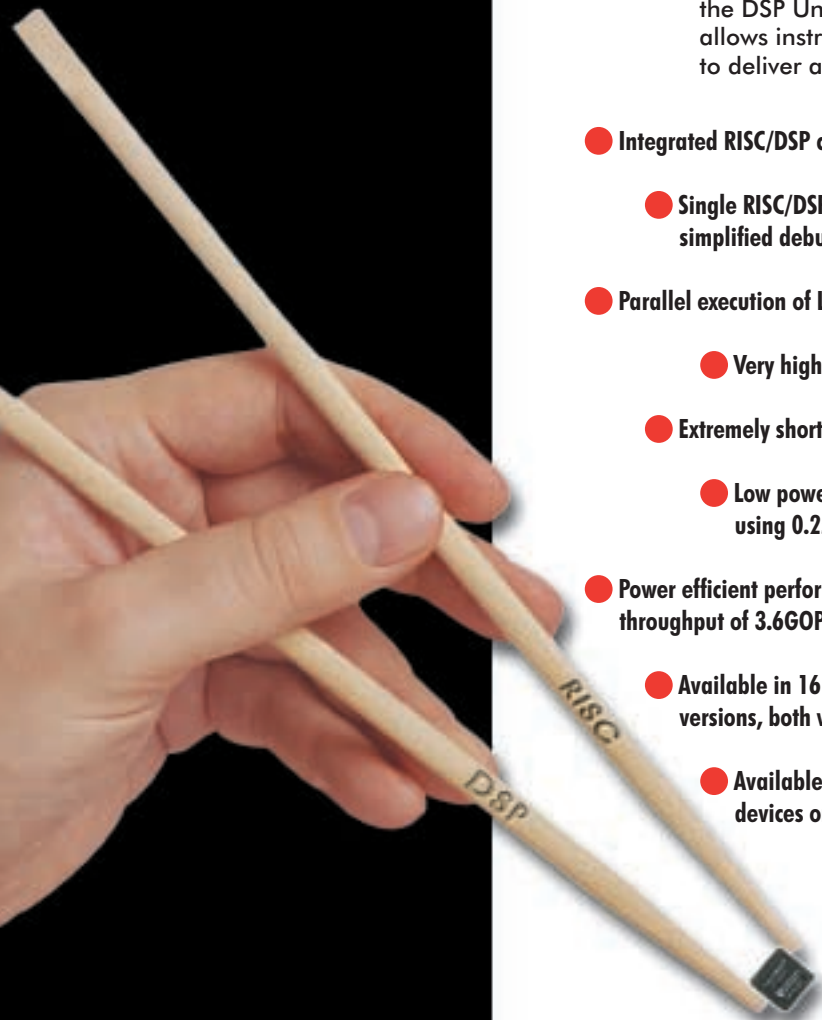
### **RISC and DSP Working Together**

The new E1-32XS offers a powerful RISC architecture with integrated DSP support and 16KByte on-chip SRAM. This unique integrated design delivers a power-efficient and cost effective solution for a wide range of portable multimedia and consumer electronic products. Now developers can have the best of both worlds – a fast RISC processor for control functions, and a DSP unit for efficient algorithm execution – yet avoid the silicon overhead and software complexity of a dual-core design.

### **Integrated Core Functionality**

The Hyperstone core has been specifically designed to combine both RISC and DSP functions – but as a single integrated core and instruction set, rather than a combination of a 2 different cores on single piece of silicon. This fully integrated core is based on a single processor model with a single instruction stream. Simple and efficient communication between the RISC and DSP units is achieved via the 96-way 32-bit internal register set. A major factor in achieving the high power-efficiency delivered by this design is the parallel operation of three functional blocks of the integrated core: the RISC ALU, the DSP Unit and the Load/Store Unit. The integrated architecture allows instructions to be streamed through all 3 units simultaneously to deliver a peak performance of 720 MOPS.

- Integrated RISC/DSP core with peak performance of 720 MOPS at 180MHz
- Single RISC/DSP instruction stream for rapid development and simplified debugging environment
- Parallel execution of Load/Store, RISC and DSP Units
  - Very high code density using variable length 16, 32 and 48 bit instructions
  - Extremely short interrupt latency - starts code execution in less than 50 ns @180MHz
  - Low power consumption of 200mW@180MHz at 2.5 V using 0.25m technology
- Power efficient performance of integrated core delivers peak throughput of 3.6GOPS/Watt
- Available in 16 or 32-bit external bus interface versions, both with full internal 32-bit execution
- Available as "off-the-shelf" standard LQFP devices or as IP core for ASIC integration



## General Architecture

The E1-32XS is based on a load/store architecture built around a large register set that includes 64 general-purpose and 32 special-purpose registers, as well as an instruction cache of 128 bytes. Local registers are organised into a 64-word, circular register stack to hold function/subroutine stack frames. The stack is organised into frames comprising as many as 16 words; the E1-32XS keeps current frames on-chip and automatically pushes the frame to off-chip memory as the register stack fills and moves frames back on-chip as the register stack empties. For fast parameter passing, the current stack frame can overlap the previous one with a variable range. Other on-chip resources include 16KByte of single-cycle access fully static SRAM, a memory and peripheral-interface controller and 3 programmable I/O lines. An integrated PLL is user programmable, allowing multiplication of the external clock by a factor of 0.5/1/2 and 4.

The variable-length 16, 32, or 48 bit instructions, automatically prefetched by the E1-32XS, support constants and native addresses of 16 and 32 bits. A 2-stage pipeline accelerates standard or delayed branches. The 4-GByte address memory space is divided into seven blocks: internal functions, on-chip SRAM and 5 external memory areas; each external block can be user-configured in software for bus width, timing and memory type. The memory interface supports glueless connection of SDRAM, extended-data-out DRAM, SRAM, EPROM, or other memory mapped devices. The separate I/O-address space also allows each I/O device to have its own timing.

## DSP Capabilities

The fully integrated DSP unit, working in parallel with the ALU and the load/store unit, can perform DSP calculations while the ALU is performing loop counts, address calculations, or load-and-store operations.

The DSP unit shares all of the E1-32XS's functional blocks, including the register set; however, it uses dedicated result registers and 32- and 64-bit hardware accumulators. The DSP unit supports 16- and 32-bit data types.

The special DSP instructions include 16x16 and 32x32 multiply, complex and real multiply-accumulate, multiply-subtract, and complex addition/subtraction. Other special instructions include test-leading-zeros.

## External Memory Support

The E1-32XS contains an SDRAM controller that allows the user to program page size, refresh rate, timing, and access parameters by using on-chip-memory registers. The controller supports synchronous DRAMs as well as fast-page-mode and extended-data-out DRAMs. Each of five external memory blocks can be supported with independent timing and bus width.

## Interrupt Latency

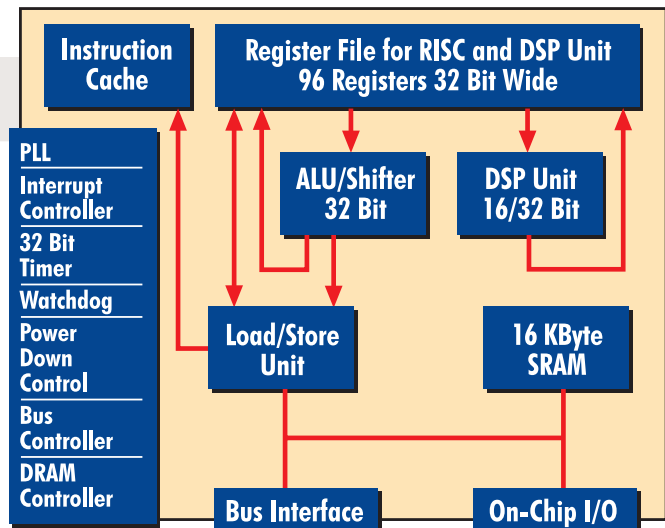
The E1-32XS is designed for very fast interrupt response. An interrupt service routine will commence within 7 clock cycles, unless blocked by a higher priority interrupt. This results in the start of code execution in less than 50 ns, at a clock rate of 180MHz. In addition to the internal interrupts, 7 external priority-controlled interrupts are provided.

## Timer Support

The on-chip hardware timer is coupled to the clock via a programmable predivider from 2 to 254, running at speeds up to 90 MHz with a resolution of about 10 ns for interrupt generation. Using the hyRTK kernel, the user has access to 254 independent "virtual" timers with very low processing overhead.

## Power Management Support

Ultra low system power consumption can be achieved by using the various on-chip mechanisms of this fully static design. In Power-Down Mode, only the interrupt logic, clock, timer, and DRAM-refresh logic remain active. Sleep Mode additionally disables external DRAM refresh. At 2.5V, current consumption in power-down and sleep modes is less than 2 mA and 100  $\mu$ A, respectively. The integrated PLL function is software programmable and provides opportunities for additional power management by modifying the internal clock frequency with multiplication factors of 1/2, 1, 2 and 4, dynamically programmable according to application requirements.



## Power Supply Voltage

The E1-32XS is designed for a core voltage of 2.5V. Interface to external memory and I/O are 3.3V tolerant.

## Packaging

The E1-32XS is available in a 144 pin LQFP, and the E1-16XS as a 100 pin LQFP (flatpack package)

## Environmental Rating

Temperature range is 0 to 70°C for the commercial and -40 to +85° for the industrial product range.

## Development Software Support

Development support includes a Development Board with expansion interfaces, a low-cost Starter Kit and the hyICE serial monitor/debugger for stand-alone operation. Development software comprises a hyMASM Macro Assembler, hyC C Compiler, hyDEBUG Source- and Task-Level Debugger, the multitasking real-time kernel hyRTK, Linker, Library Manager, and a Profiler. A hyDSP software library including more than 135 functions is available providing support for Assembler and C programming.

# RISC + DSP = hyperstone

Hyperstone AG, Am Seerhein 8, D-78467 Konstanz, Germany

Phone: +49 (7531) 98030 Fax: +49 (7531) 51725

E-mail: [info@hyperstone.de](mailto:info@hyperstone.de)

Website: [www.hyperstone-ag.com](http://www.hyperstone-ag.com)