CSS Descrambler Chip

Preliminary Datasheet

LSI LOGIC

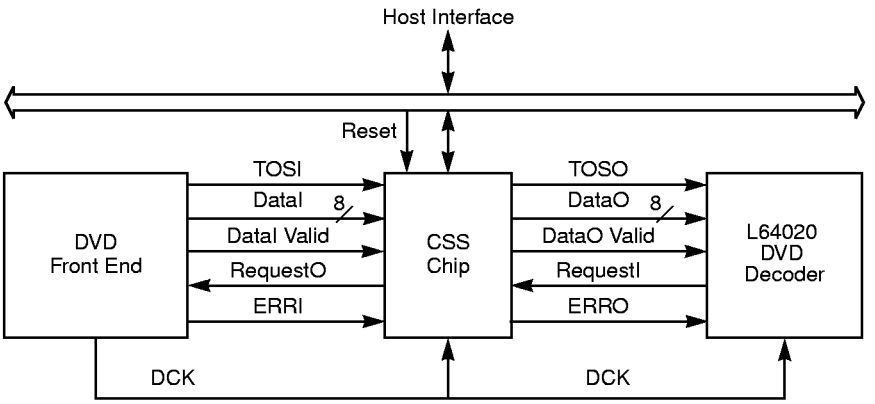
The CSS (Content Scramble System) Descrambler Chip is a low-cost authenticator/descrambler designed for easy implementation into an LSI Logic L64020–based DVD decoding system.

The CSS Chip is fully compatible with LSI Logic's L64020 single-chip DVD Decoder. It provides a seamless interface to the L64020 and may be bypassed for direct decoding of nonscrambled MPEG-2 data streams. The system block diagram in Figure 1 shows a basic CSS Chip application within a typical DVD decoding system. The CSS Chip may also be integrated into PC DVD systems that feature standard VMI, VIP, or PCI bus interfaces. (Application specifications are under development.)

The CSS Chip is designed to support DVD players with 2064 bytes per sector or PC DVD drives with 2048 bytes per sector.

The CSS Chip is available in an 80-pin plastic quad flat pack (PQFP). It is manufactured using a 0.35 micron CMOS process and is available in a 3.3-V version for low-power applications.

Figure 1 System Block Diagram



Note: The DCK output is optional. In this system, the DCK signal for the L64020 is provided via the CSS Chip.

Features

- Performs authentication and descrambling of DVD data streams
- All signals fully compatible with the L64020 DVD Decoder
- Seamless interface with the L64020 DVD Decoder
- CSS descrambling may be bypassed for direct decoding of nonscrambled MPEG-2 data streams
- Disc Key extraction and authentication, Title Key decryption and authentication, and data stream descrambling modes enabled through the Host Interface
- Supports DVD players (2064 bytes/sector) or PC DVD drives (2048 bytes/sector)
- 27 MHz system clock
- Stream data transfer rate: 27 MHz/4 (bytes/s)
- TTL compatible I/O pins
- Low-power version available (V_{DD} = 3.3 V)
- 0.35 micron CMOS process
- 80-pin PQFP package

Register Descriptions

Table 1 contains a register map for the CSS Chip. This table is followed by a description of the register fields.

Table 1 CSS Chip Register Map

Register	Bits	R/W	Description
0	7	R	TOS Error Interrupt Status 1: TOS Error Detected 0: Not Detected (default)
		W	TOS Error Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	6	R	Key Data Error Interrupt Status 1: Key Data Error Detected 0: Not Detected (default)
		W	Key Data Error Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	5	R	Title Key Different Interrupt Status 1: Title Key Different 0: Not Different (default)
		W	Title Key Different Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	4	R	Title Key Decryption Complete Interrupt Status 1: Title Key Decryption Complete 0: Not Complete (default)
		W	Title Key Decryption Complete Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	3	R	Disc Key Extraction Error Interrupt Status 1: Disc Key Extraction Error 0: Not Error (default)
		W	Disc Key Extraction Error Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	2	R	Disc Key Extraction Complete Interrupt Status 1: Disc Key Extraction Complete 0: Not Complete (default)
		W	Disc Key Extraction Complete Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	1	R	Decoder Response Data Ready Interrupt Status 1: Decoder Response Data Ready0: Not Ready (default)
		W	Decoder Response Data Ready Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask
	0	R	Drive Challenge Data Ready Interrupt Status 1: Drive Challenge Data Ready 0: Not Ready (default)
		W	Drive Challenge Data Ready Interrupt Mask 1: Interrupt Mask (default) 0: Non Mask

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Table 1 CSS Chip Register Map (Cont.)

Register	Bits	R/W	Description
1	7:3		Reserved
	2	R/W	Force non-descramble enable 1: Force non-descramble 0: Descramble (default)
	1	R/W	TOS enable 1: TOS enable (default) 0: TOS disable
	0	R/W	Application Type 1: PC DVD drive with 2048 bytes/sector 0: DVD player with 2064 bytes/sector (default)
2	7:4		Reserved
	3	W	Software Reset
	2:0	R/W	CSS Mode **Bits** **Description** 0 0 0 bypass (CSS bypass, default) 0 0 1 DK (DK extraction) 0 1 0 AV_Desc (A/V descramble) 0 1 1 Auth_DK (authentication and DK extraction) 1 0 0 Auth_TK (authentication and TK decryption) 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved
3	7:1		Reserved
	0	W	Clear Interrupt Pin
4–13	80 bits	R	Challenge Data (Drv_Chal)
		W	Challenge Data (Dec_Chal)
14–18	40 bits	R	Response Data (Dec_Res)
		W	Response Data (Drv_Res)
19–23	40 bits	W	Bus Encrypted Title Key
24–511			Reserved

(Sheet 2 of 2)

Register 0

TOS Error Interrupt Status (R) **[7]**

1: TOS Error detected
0: Not detected (default)

A Top of Sector (TOS) Error occurs when the internal byte counter does not match the timing of the TOS signal. For example, in DVD player systems, the TOS signal must be asserted at 2064 active byte intervals (2048 bytes/sector in PC DVD drive systems). If this timing constraint is not met, a TOS Error Interrupt occurs.

TOS Error Interrupt Mask (W) **[7]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the TOS Error Interrupt.

Key Data Error Interrupt Status (R) **[6]**

1: Key Data Error detected
0: Not detected (default)

This bit indicates that the error input pin (CS_ERROR_BI) has been asserted resulting from a data error that has occurred during Disc Key or Title Key Extraction. Upon detecting a Key Data Error, the Host may take action, if necessary.

Key Data Error Interrupt Mask (W) **[6]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Key Data Error Interrupt.

Title Key Different Interrupt Status (R) **[5]**

1: Title Key Different
0: Not Different (default)

This bit indicates that the most recently extracted Title Key (in the AV_Desc mode) does not match the previously extracted Title Key. In a DVD Book title, the Title Keys in the sector header must remain constant. A mismatch between the new Title Key and the previous one results in an error. In the event of this interrupt, the CSS continues to descramble and update each sector header.

Title Key Different Interrupt Mask (W) **[5]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Title Key Different Interrupt.

Title Key Decryption Complete Interrupt Status (R) **[4]**

1: Title Key Decryption Complete
0: Not Complete (default)

By reading this bit, the Host monitors the Title Key Decryption Complete Interrupt Status. An interrupt occurs when the CSS completes the Title Key Decryption. As a result, this bit is set. The Host clears this bit upon reading it. After the Host receives the interrupt, the CSS may proceed to the AV_Desc mode.

Title Key Decryption Complete Interrupt Mask (W) **[4]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Title Key Decryption Complete Interrupt.

Disc Key Extraction Error Interrupt Status (R) **[3]**

1: Disc Key Extraction Error
0: Not Error (default)

This bit indicates that an error has occurred during the Disc Key Extraction. This bit is set when DK mismatching is detected. Since DK mismatching is a fatal error, the Host must take some action, such as “Disc TOC read retry.”

Disc Key Extraction Error Interrupt Mask (W) **[3]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Disc Key Extraction Error Interrupt.

Disc Key Extraction Complete Interrupt Status (R) **[2]**

1: Disc Key Extraction Complete
0: Not Complete (default)

By reading this bit, the Host monitors the Disc Key Extraction Complete Interrupt Status. After a Disc Key Extraction Complete Interrupt has occurred, this bit is set. The Host clears this bit upon reading it. After the Host receives the interrupt, the CSS may proceed into the AV_Desc mode.

Disc Key Extraction Complete Interrupt Mask (W) **[2]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Disc Key Extraction Complete Interrupt.

Decoder Response Data Ready Interrupt Status (R) **[1]**

1: Decoder Response Data Ready
0: Not Ready (default)

By reading this bit, the Host monitors the Decoder Response Data Ready Interrupt Status. After the CSS generates the Decoder Response Data, this bit is set, thereby indicating that a Decoder Response Data Ready Interrupt has occurred. The Host clears this bit upon reading it.

Decoder Response Data Ready Interrupt Mask (W) **[1]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Decoder Response Data Ready Interrupt.

Drive Challenge Data Ready Interrupt Status (R) **[0]**

1: Drive Challenge Data Ready
0: Not Ready (default)

By reading this bit, the Host monitors the Drive Challenge Data Ready Interrupt Status. After the CSS generates the Drive Challenge Data, this bit is set, indicating that a Drive Challenge Data Ready Interrupt has occurred. The Host clears this bit upon reading it.

Drive Challenge Data Ready Interrupt Mask (W) **[0]**

1: Interrupt Mask (default)
0: Non Mask

Setting this bit masks the Drive Challenge Data Ready Interrupt.

Register 1

Reserved **[7:3]**

Force Non-descramble Enable (R/W) **[2]**

1: Force Non-descramble
0: Descramble (default)

When the Host sets this bit, the CSS disables the descrambling mode and outputs the unscrambled sector data regardless of the status of the scrambling control flag. The CSS performs this function in order to prevent the playback of an illegally copied disc.

TOS enable (R/W) **[1]**

1: TOS enable (default)
0: TOS disable

This bit enables and disables the Top of Sector (TOS) input pin (CS_TOSI). When the Host sets this bit, the CSS observes the TOS signal and resets all sector-related counters in accordance with the TOS status. The TOS signal must be issued only at the first byte of each sector. When the Host clears this bit, the CSS ignores the TOS signal and continues descrambling in sync with the internal counter.

Application Type (R/W) **[0]**

1: PC DVD drive with 2048 bytes/sector
0: DVD player with 2064 bytes/sector (default)

Setting this bit indicates that a PC DVD drive with 2048 bytes per sector is in operation. The default setting indicates that a DVD player with 2064 bytes per sector is in operation.

Register 2

Reserved **[7:4]**

Software Reset (W) **[3]**

When this bit is set, the CSS Chip is initialized. This software reset functions in the same manner as a hard reset (power-on reset), with the exception that the Host register settings for the decrypted Disc Key and the decrypted Title Key are maintained.

CSS Mode (R/W) **[2:0]**

000: bypass (CSS bypass, default)

The CSS is bypassed and all channel interface signals are directly connected to the L64020. Immediately following reset, the CSS Mode is reset to this default.

001: DK (DK extraction)

This mode must be set when a DVD disc is inserted on the DVD player tray. This mode is required only when the system incorporates a DVD player. When the Host sets this bit, the CSS is ready to accept the Disc Key sector in the lead-in area. Once the CSS reads the Disc Key sector, it subsequently generates the Disc Key and Title Key. When the CSS completes this sequence, it issues the Disk Key Extraction Complete Interrupt (see the “Disk Key Extraction Complete Interrupt” field, page 7).

010: AV_Desc (A/V descramble)

This mode must be set when the Host or the Front End Drive is ready to start A/V contents descrambling. When the system incorporates a DVD player, the CSS extracts the Title Key from the sector header area and recovers the active Title Key necessary for descrambling the A/V contents. In the A/V sector area (2048 bytes), the CSS descrambles the A/V contents based on the status of the scramble control flag in the sector header. When a PC DVD drive is used, the CSS only descrambles the A/V contents. The CSS extracts the Title Key while in the Auth_TK mode (100) described next.

011: Auth_DK (authentication and DK extraction)

This mode is used for DK authentication when a DVD disc is inserted on the PC DVD drive tray. When the Host sets this mode, the CSS generates the challenge code and informs the Host that the code is ready for authentication with an interrupt (see the "Drive Challenge Data Ready Interrupt Status" field, page 7). Once the challenge code is ready, the Host may perform authentication according to the Host control flow (see "Control Flow for Disc Key Authentication (PC DVD Drive)," page 13).

100: Auth_TK (authentication and TK decryption)

When a PC DVD drive is incorporated in the system, the Host must select this mode in order to play back the DVD title. When the Host sets this mode, the CSS generates the challenge code and informs the Host that the code is ready for authentication with an interrupt (see the "Drive Challenge Data Ready Interrupt Status" field, page 7). Once the challenge code is ready, the Host may perform authentication according to the Host control flow (see "Control Flow for Disc Key Authentication (PC DVD Drive)," page 13).

101: Reserved

110: Reserved

111: Reserved

Register 3

Reserved **[7:1]**

Clear Interrupt Pin (W) **[0]**

The Host sets this bit in order to clear the pin on which the interrupt was issued.

Other Registers

Challenge Data (R/W) **Registers 4–13 (80 Bits)**

After a Drive Challenge Data Ready Interrupt occurs, the Host reads this register and sends the drive challenge code (Drv_Chal) to the PC DVD drive. The Host also writes the decoder challenge code (Dec_Chal) from the PC DVD drive to this register. Once the Decoder challenge code is written to this register, the CSS continues performing authentication without any additional action.

Response Data (R/W) **Registers 14–18 (40 Bits)**

The Host reads the drive response data (Drv_Res) from the PC DVD drive and writes it to this register. Once the data is written, the CSS continues performing authentication and generates decoder response data (Dec_Res) to this register. After a Decoder Response Data Ready Interrupt occurs, the Host reads this register and transfers the Dec_Res data to the PC DVD drive (see “Host CPU Control Flow,” page 13).

BUS Encrypted Title Key (W) **Registers 19–23 (40 Bits)**

In the Auth_TK mode (CSS Mode = “100”), the Bus Encrypted Title Key cannot be transferred by means of the data bus. Therefore, the Host must transfer the Title Key from the PC DVD drive to this register (see “Host CPU Control Flow,” page 13).

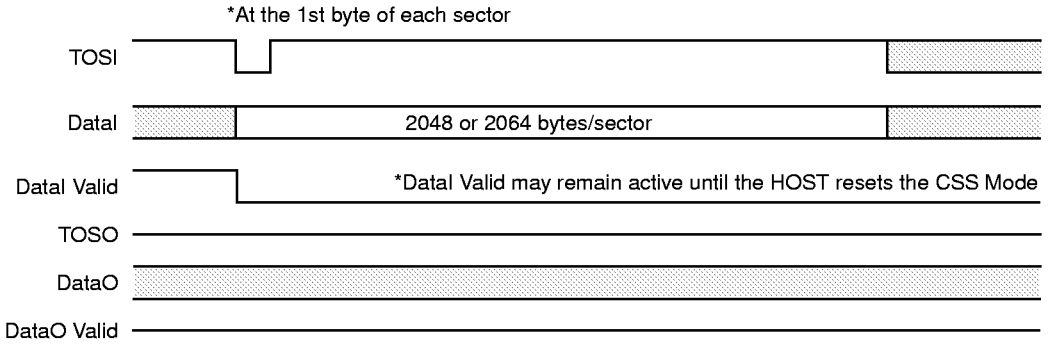
Reserved **Registers 24–511**

Functional Waveforms

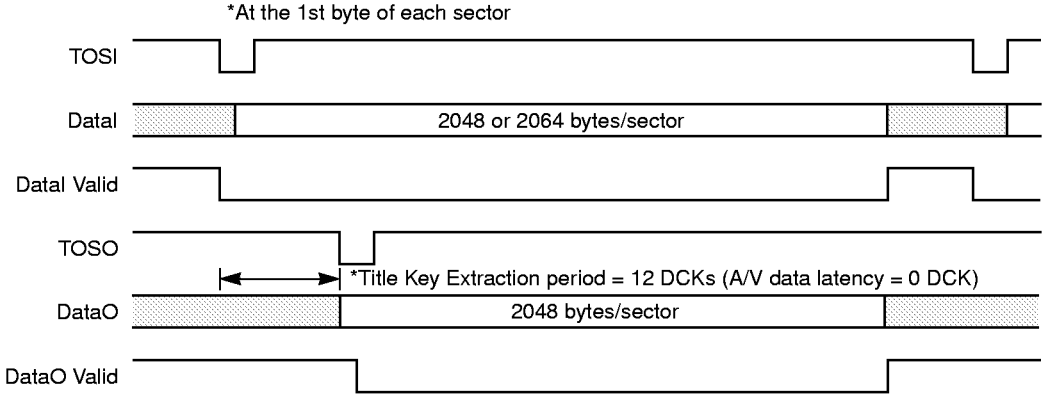
Figure 2 shows the functional waveforms for the CSS Chip while it is operating in the Disk Key Extraction and Main Data Descrambling modes, respectively.

Figure 2 Functional Waveforms

Disc Key Extraction Mode



Main Data Descrambling Mode



Host CPU Control Flow

This section provides three examples of CSS operation flows as controlled by an external Host CPU. The first example is a typical control flow for the CSS in descramble mode (AV_Desc) while a DVD player is in operation. The second example is a Host control flow while the CSS is in the authentication and Disc Key extraction mode (Auth_DK), following DVD disc insertion into a PC DVD drive. The last example lists the control flow for the playback of a DVD title (CSS in Auth_TK mode) and for subsequent descrambling (CSS in AV_Desc) while a PC DVD drive is in operation.

Typical Control Flow for CSS Descrambling (DVD Player)

1. Insert a disc into the DVD player.
2. Reset the CSS Chip with a software reset.
3. Set the *CSS Mode* field to the *DK* mode (001).
4. Start reading the Disc Key sector in the lead-in area.
5. Wait for the *Disc Key Extraction Complete Interrupt*.
6. Stop reading the DVD Front End.
7. Change the *CSS Mode* to the *AV_Desc* mode (010).
8. Start reading the Main Data sectors.
9. After 12 channel data clock cycles, following the top of the sector signal (CS_TOSI), the CSS descrambles the first byte of A/V data and begins continuous data transfer.

Control Flow for Disc Key Authentication (PC DVD Drive)

1. Insert a disc into the PC DVD drive.
2. Reset the CSS Chip with a software reset.
3. Set the *Application Type* field to PC DVD drive (1).
4. Set the *CSS Mode* field to the *Auth_DK* mode (011).
5. Wait for the *Drive Challenge Data Ready Interrupt*.
6. Read the *Challenge Data* register and send the *Drv_Chal* data to the DVD drive.

7. Read the *Drv_Res* data from the DVD drive and write it to the *Response Data* register.
8. Read the *Dec_Chal* data from the DVD drive and write it to the *Challenge Data* register.
9. Wait for the *Decoder Response Data Ready Interrupt*.
10. Read the *Response Data* register and send the *Dec_Res* data to the DVD drive.
11. Start reading the Disc Key sector to the lead-in area.
12. Wait for the *Disc Key Extraction Complete Interrupt*.
13. Stop reading the DVD Front End.

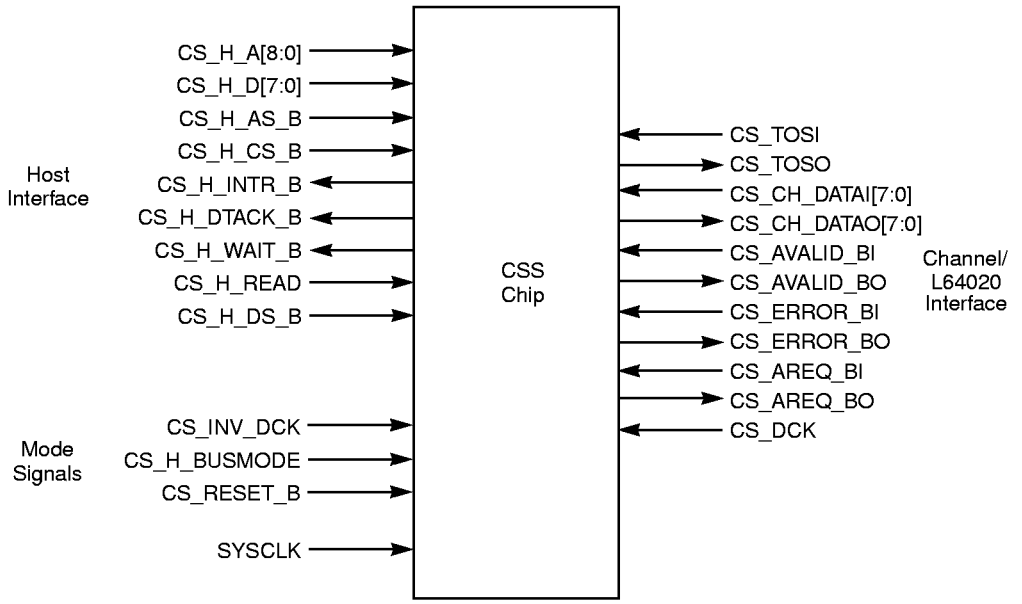
Playback of DVD Title and Descramble Control Flow (PC DVD Drive)

1. Set the *Application Type* field to PC DVD drive (1).
2. Set the *CSS Mode* field to the *Auth_TK* mode (100).
3. Wait for the *Drive Challenge Data Ready Interrupt*.
4. Read the *Challenge Data* register and send the *Drv_Chal* data to the DVD drive.
5. Read the *Drv_Res* data from the DVD drive and write it to the *Response Data* register.
6. Read the *Dec_Chal* data from the DVD drive and write it to the *Challenge Data* register.
7. Wait for the *Decoder Response Data Ready Interrupt*.
8. Read the *Response Data* register and send the *Dec_Res* data to the DVD drive.
9. Read the *Bus-Encrypted Title Key* from the DVD drive and write it to the *Bus Encrypted Title Key* register.
10. Wait for the *Title Key Decryption Complete Interrupt*.
11. Change the *CSS Mode* field to the *AV_Desc* mode (010).
12. Start reading the Main Data sectors.
13. The CSS generates the first byte of descrambled A/V data and begins continuous data transfer with no clock delay.

Signal Descriptions

This section describes the CSS Chip interface signals. Because the CSS is an intermediate device between the DVD player and the L64020 DVD Decoder, it shares signals names with the L64020. The channel interface signal names, with the exception of the data clock signal (CS_DCK), occur as I/O pairs. The channel interface input signal names have the suffix “I,” and their corresponding output signal names have the suffix “O” (for example, CS_TOSI and CS_TOSO). Figure 3 shows the interface signals for the CSS Chip. A description of each signal follows. The suffixes “_B,” “_BI,” and “_BO” indicate that the signal is active-LOW.

Figure 3 CSS Chip Interface Signals



Host Interface

CS_H_A[8:0] Address Bus **Input**
This 9-bit address bus provides access to the CSS internal registers. The address value on these lines is latched on the falling edge of CS_H_AS_B (Motorola) or on the falling edge of CS_H_READ_B/CS_H_WRITE_B (Intel).

CS_H_AS_B Address Strobe (Motorola only) **Input**
On the falling edge of the CS_H_AS_B signal, the CSS latches the address that appears on the CS_H_A[8:0] bus. CS_H_AS_B LOW and CS_H_CS_B LOW indicate the start of a bus transaction. The rising edge of CS_H_AS_B indicates the end of a bus transaction.

CS_H_CS_B Chip Select (Motorola and Intel) **Input**
This active-LOW signal indicates an attempt by the Host CPU to access the CSS either for a read or a write bus cycle. CS_H_CS_B LOW and CS_H_AS_B LOW indicate the start of a bus transaction in the Motorola mode. CS_H_CS_B LOW and CS_H_READ_B LOW or CS_H_WRITE_B LOW indicate the start of a bus cycle in the Intel mode. The actual transaction type (either read or write) is determined by the CS_H_READ polarity (Motorola type interface) or by the CS_H_READ_B and WRITE_B polarity (Intel type interface). The end of a bus cycle is determined by the rising edge of CS_H_AS_B (Motorola) or by the rising edge of CS_H_READ_B or WRITE_B (Intel). CS_H_CS_B may remain active LOW for more than one bus transaction cycle.

CS_H_D[7:0] Host Data Bus **Bidirectional**
This host data bus is an 8-bit bidirectional data line used for data communication between the Host CPU and the CSS Chip. CS_H_DTACK_B or CS_H_WAIT_B indicate the moment at which the data on the Host data bus is valid. The rising edge of CS_H_WRITE_B (Intel) or CH_H_DS_B (Motorola) prompts the CSS to strobe the data into the chip.

CS_H_DS_B (Motorola) or CS_H_WRITE_B (Intel)
Data Strobe **Input**
CS_H_DS_B (Motorola) indicates when the CPU strobes the data in or out of the CSS. During a read bus cycle, the start of a read transaction is triggered when

CS_H_DS_B, CS_H_CS_B, and CS_H_AS_B are all LOW. During a write bus cycle, the rising edge of CS_H_DS_B indicates when the CSS latches the data present on CS_H_D[7:0].

CS_H_WRITE_B (Intel) LOW indicates that the Host CPU is performing a write bus cycle. CS_H_READ/CS_H_READ_B must be HIGH during a write cycle. CS_H_CS_B LOW indicates that the host CPU is attempting to write to the internal registers of the CSS. The address is registered on the falling edge of CS_H_READ_B. On the rising edge of CS_H_WRITE_B, the CSS latches the data present on CS_H_D[7:0].

CS_H_DTACK_B (Motorola) or CS_H_RDY_B (Intel)

Data Acknowledge **3-State Output**

The CSS drives the CS_H_DTACK_B (Motorola) signal LOW to notify the external Host CPU that the current bus transaction can be completed. The CSS drives this signal HIGH when it is not ready to complete the bus cycle. CS_H_DTACK_B is a 3-state signal when CS_H_CS_B is inactive.

The CSS drives the CS_H_RDY_B (Intel) signal LOW to notify the external Host CPU that the CSS is ready to complete the current bus transaction. The CSS drives CS_H_RDY_B HIGH when the CSS is not ready. This is a 3-state signal if CS_H_CS_B is not active.

CS_H_INTR_B

Interrupt **OD Output**

This signal is an open drain active-LOW interrupt output. The host interface of the CSS drives this signal LOW in order to send an interrupt to the Host CPU.

CS_H_READ (Motorola) or CS_H_READ_B(Intel)

Read/Write Strobe **Input**

CS_H_READ (Motorola) indicates whether the current bus cycle is a read cycle or a write cycle. When CS_H_READ is HIGH, a read bus cycle is in progress. When CS_H_READ is LOW, a write bus cycle is in progress. CS_H_CS_B must be LOW for the CPU to access the CSS.

CS_H_READ_B (Intel) is LOW when the external CPU is performing a bus read cycle. CS_H_WRITE_B must be HIGH during a read cycle. When CS_H_CS_B and CS_H_READ_B are LOW, the Host CPU is reading from the internal registers of the CSS. The address is registered on the falling edge of CS_H_READ_B.

CS_H_WAIT_B (Motorola) or CS_H_WTN(Intel)

Device Wait **3-State Output**

This signal is 3-state or active-LOW when used as a CS_H_WAIT_B signal. With the exception of an inverse polarity, this signal functions similarly to the CS_H_DTACK_B/CS_H_RDY_B signal (described earlier). The CSS drives this signal HIGH to notify the external Host CPU that the current bus transaction can be completed. This is a 3-state signal when CS_H_CS_B is inactive. The CSS drives this signal LOW when it is not ready to end the bus cycle.

Channel/L64020 Interface

CS_AREQ_BI (CS_AREQ_BO)

Audio Transfer Request **Input (Output)**

When the CS_AREQ_BI signal is asserted LOW, it indicates that the L64020 DVD Decoder is ready to receive a new byte of coded audio data. The CSS relays this signal to the DVD player by asserting the CS_AREQ_BO signal LOW. The maximum transfer rate over this interface is 40 Mbit/s.

CS_AVALID_BI (CS_AVALID_BO)

Audio Data Valid **Input (Output)**

The rising edge of CS_AVALID_BI writes the next byte of audio data or program stream data that is present on the CS_CH_DATAI[7:0] pins. In the AV descramble mode, the CSS descrambles the incoming data and asserts the CS_AVALID_BO signal LOW. In the bypass mode, the CSS relays the audio data valid input to the L64020 by immediately asserting the CS_AVALID_BO signal LOW. The CS_AVALID_BI signal may be used in combination with the CS_DCK data clock to obtain synchronous input on the CSS's data channel interface.

CS_CH_DATAI[7:0] (CS_CH_DATAO[7:0])

Channel Data Bus **Input (Output)**

CS_CH_DATAI[7:0] is an input bus line that serves as a parallel path for channel data from the DVD player. CS_CH_DATAO[7:0] is an output bus line that serves as a parallel path for channel data to the L64020 DVD Decoder.

CS_DCK **Channel Data Clock** **Input**

The CS_DCK signal is a free-running clock from the external channel. The CS_DCK and CS_AVALID_BI signals combined can synchronously write data to the CSS channel input.

CS_ERROR_BI (CS_ERROR_BO)

Error **Input (Output)**

CS_ERROR_BI is an active-LOW input signal. The DVD player asserts this signal to indicate that the channel data contains an error and to invoke error handling in the CSS. The CS_ERROR_BI signal is latched with the data on the rising edge of CS_AVALID_BI. CS_ERROR_BI is not used for DMA transfers. Once CS_ERROR_BI is asserted LOW, the CSS activates CS_ERROR_BO LOW, thereby relaying the error signal to the L64020.

CS_TOSI (CS_TOSO)

Top of Sector **Input (Output)**

The DVD player asserts CS_TOSI during the pack start code at the top of a sector. The CSS uses CS_TOSI for error detection and registers this signal on the rising edge of CS_AVALID_BI. The CSS asserts CS_TOSO LOW in order to relay the top of sector signal to the L64020.

Mode Signals

CS_H_BUSMODE
Controller Select Pin **Input**
This signal specifies whether the Host CPU is an Intel or a Motorola microprocessor. When HIGH, the Motorola mode is selected. When LOW, the Intel mode is selected. The Motorola processor uses a single pin to specify read and write transfers. The Intel processor uses two separate pins to specify read and write transfers.

CS_INV_DCK **DCK Invert Mode** **Input**
The CS_INV_DCK is the invert channel data clock mode (CS_DCK) signal.

CS_RESET_B **Reset** **Input**
This is an active-LOW input signal. When an external source asserts CS_RESET_B, the CSS resets itself. The minimum RESET pulse width is eight cycles of SYSCLK. SYSCLK must be running during reset.

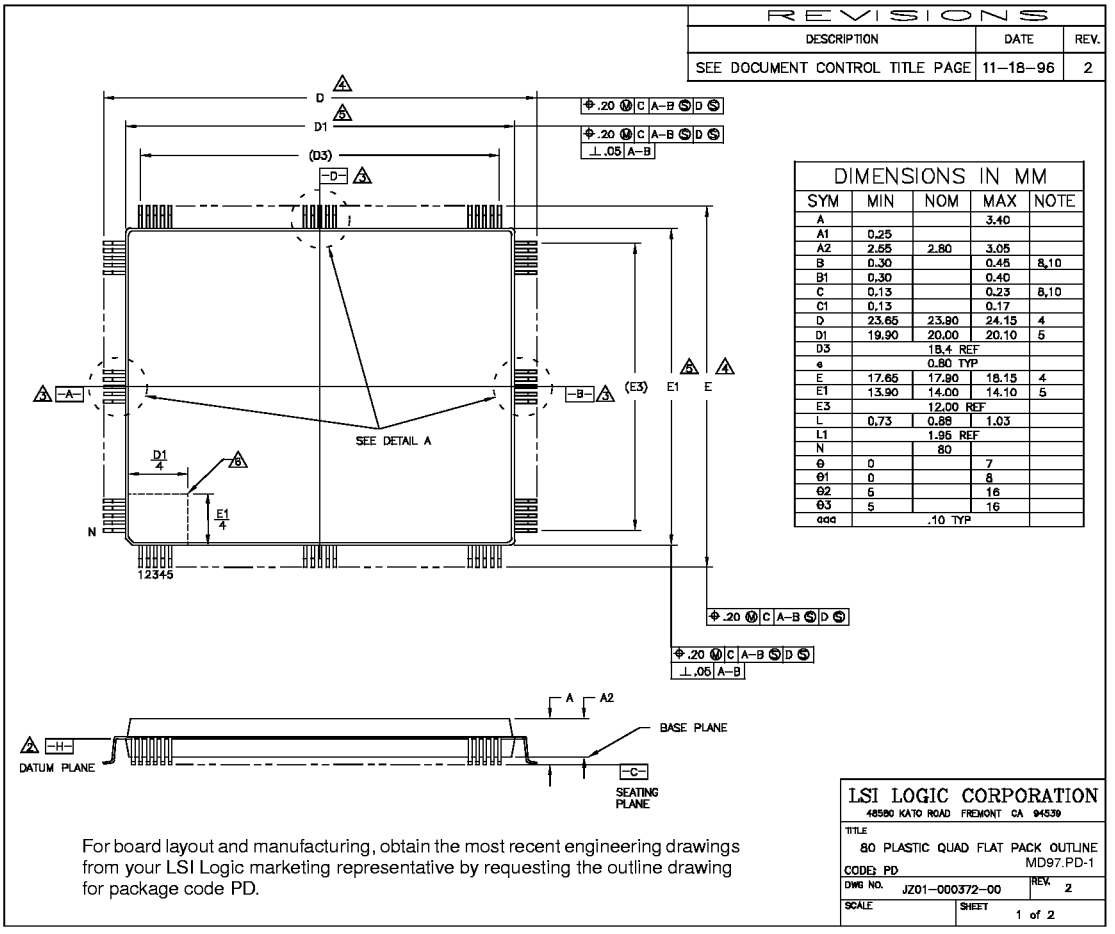
Other Signals

SYSCLK **Device Clock** **Input**
SYSCLK is the input system clock for the CSS. The clock runs at a nominal frequency of 27 MHz.

Package Dimensions

This sections contains the mechanical drawings for the 80-pin plastic quad flat pack (PQFP).

Figure 4 80-pin PQFP Package Dimensions



For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PD.

Figure 4 (Cont.) 80-pin PQFP Package Dimensions