PRELIMINARY

ADV MICRO (TELECOM)

T-75-15

Am79C30A

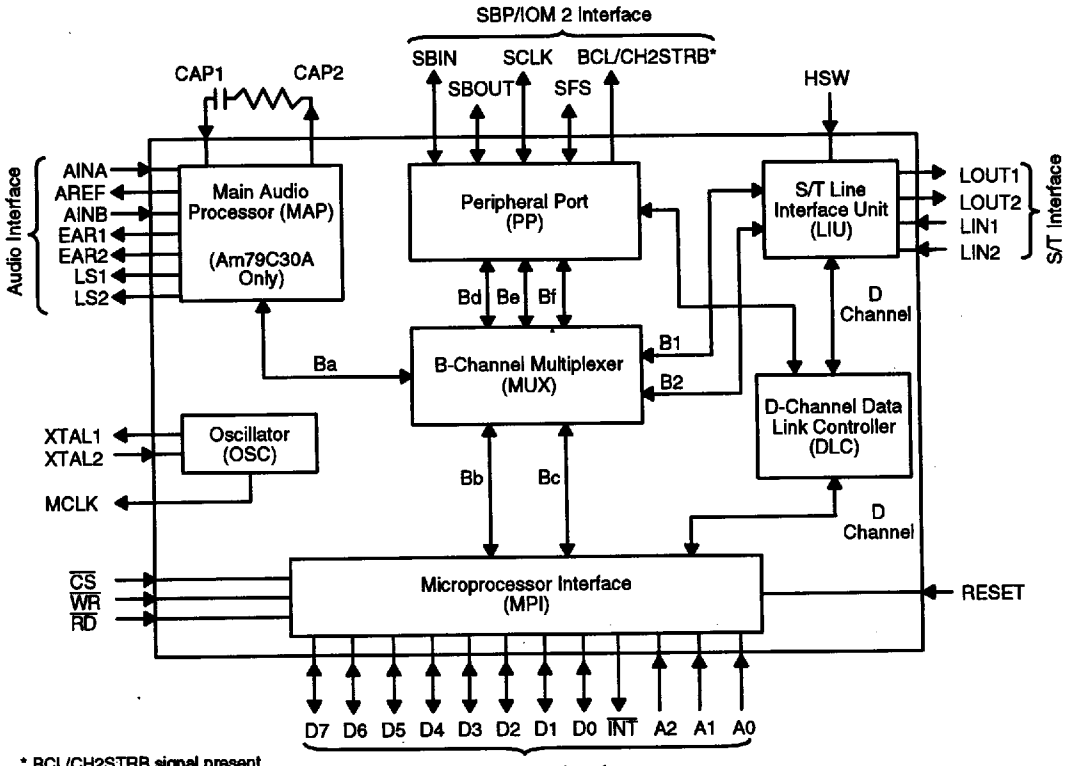
Digital Subscriber Controller™ (DSC™) Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Combines CCITT I.430 S/T-Interface Transceiver, D-Channel LAPD Processor, Audio Processor (DSC device only), and IOM 2 Interface in a single chip**
- **Special operating modes allow realization of CCITT I.430 power-compliant terminal equipment**
- **S- or T-Interface Transceiver**
  - —Level 1 Physical Layer Controller
  - —Supports point-to-point, short and extended passive bus configurations
  - —Provides multiframe support
- **Certified protocol software support available**
- **CMOS technology, TTL compatible**
- **D-channel processing capability**
  - —Flag generation/detection
  - —CRC generation/checking
  - —Zero insertion/deletion
  - —Four 2-byte address detectors
  - —32-byte receive and 16-byte transmit FIFOs

BLOCK DIAGRAM



* BCL/CH2STRB signal present only for PLCC package.

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DISTINCTIVE CHARACTERISTICS (continued)

- **Audio processing capability (DSC circuit only)**
  - —Dual audio inputs
  - —Earpiece and loudspeaker drivers
  - —Codec/filter with A/μ selection
  - —Programmable gain and equalization filters
  - —Programmable sidetone level
  - —Programmable DTMF, single tone, progress tone, and ringer tone generation
  - —Programmable on-chip microphone amplifier
- **Pin and software compatible with the Am79C32A ISDN Data Controller (IDC™) Circuit. The Am79C32A is used in data-only applications**

GENERAL DESCRIPTION

The Am79C30A Digital Subscriber Controller (DSC) Circuit and Am79C32A ISDN Data Controller (IDC) Circuit, shown in the Block Diagram, allow the realization of highly-integrated Terminal Equipment for the ISDN. The Am79C30A/32A is fully compatible with the CCITT I-series recommendations for the S and T reference points, ensuring that the user of the device may design TEs which conform to the international standards.

The Am79C30A/32A provides a 192-kb/s full duplex digital path over four wires between the TE located on the subscriber's premises and the NT or PABX linecard. All physical Layer functions and procedures are implemented in accordance with CCITT Recommendation I.430, including framing, synchronization, maintenance, and multiple terminal contention. Both point-to-point and point-to-multipoint configurations are supported.

The Am79C30A/32A processes the ISDN basic rate bit stream, which consists of B1 (64 kb/s), B2 (64 kb/s), and D (16 kb/s) Channels. The B Channels are routed to and from different sections of the Am79C30A/32A under software control. The D Channel is partially processed by the DSC/IDC circuit and is passed to the microprocessor for further processing.

The Main Audio Processor (MAP) uses Digital Signal Processing (DSP) to implement a high performance codec/filter function. The MAP interface supports a loudspeaker, an earpiece, and two separate audio inputs. Programmable on-chip gain is provided to simplify use of low output level microphones. The user may alter frequency response and gain of the MAP receive and transmit paths. Tone generators are included to implement ringing, call progress, and DTMF signals.

A Peripheral Port (PP) is provided to allow the B Channels to be routed off-chip for processing by other peripherals. This port is configurable as either an industry-standard IOM 2 port, or as a serial bus port (SBP).

The TE design process is simplified by the availability of certified protocol software packages, which provide complete system solutions through OSI Layer 3.

CONNECTION DIAGRAMS
Top View

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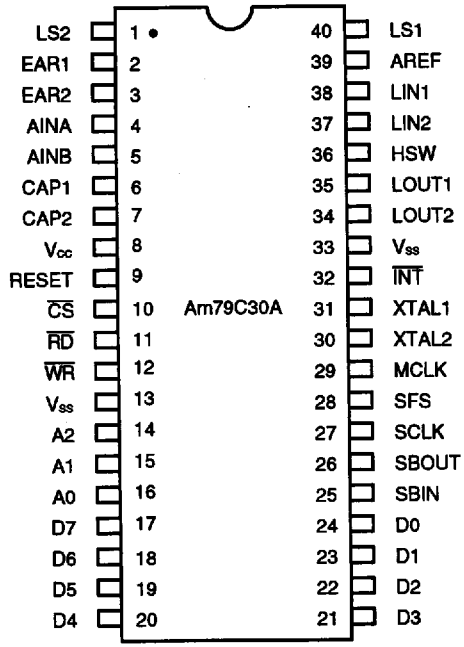
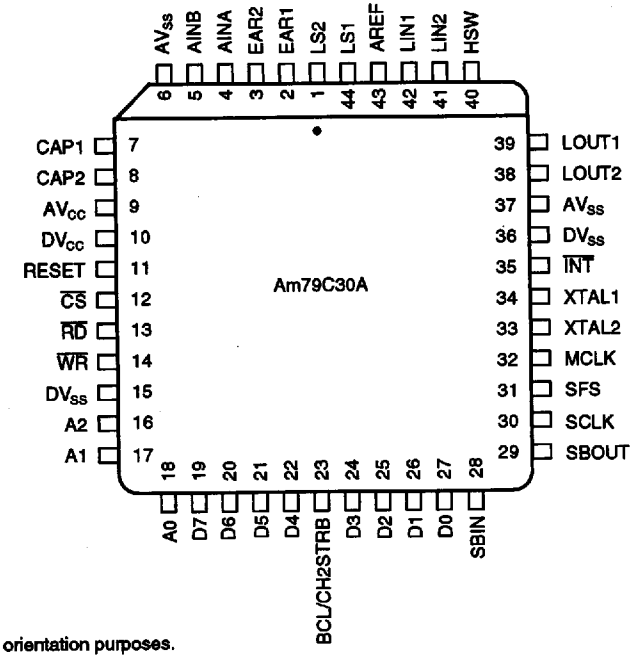
40-Pin DIP



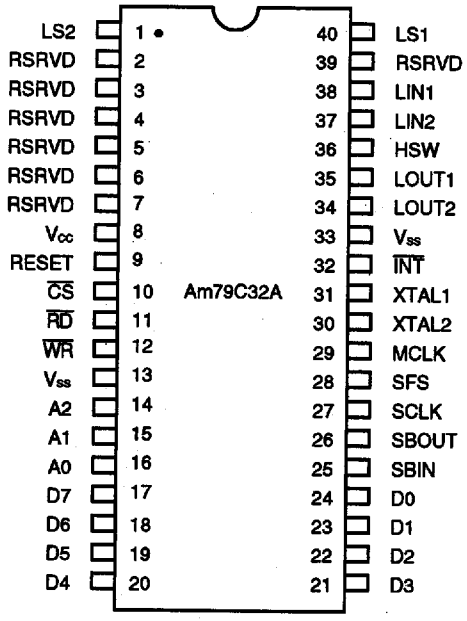
44-Pin PLCC



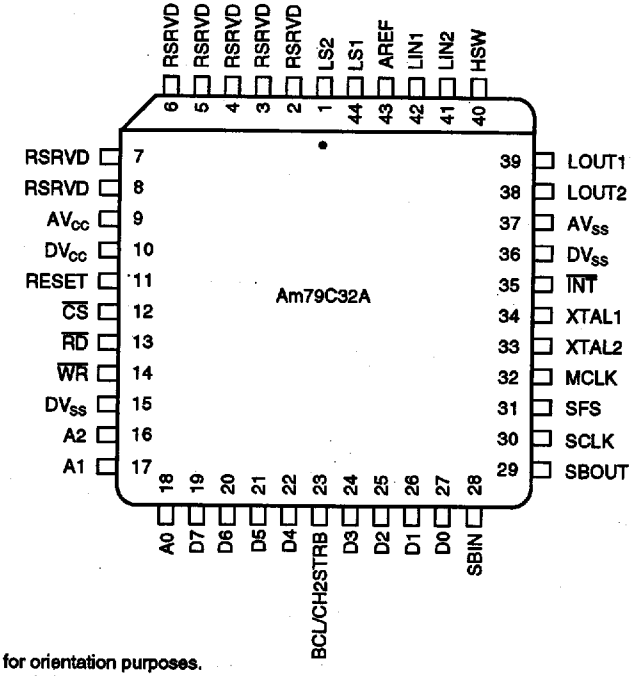
Note: Pin 1 is marked for orientation purposes.

CONNECTION DIAGRAMS (continued)
Top View

40-Pin DIP



44-Pin PLCC



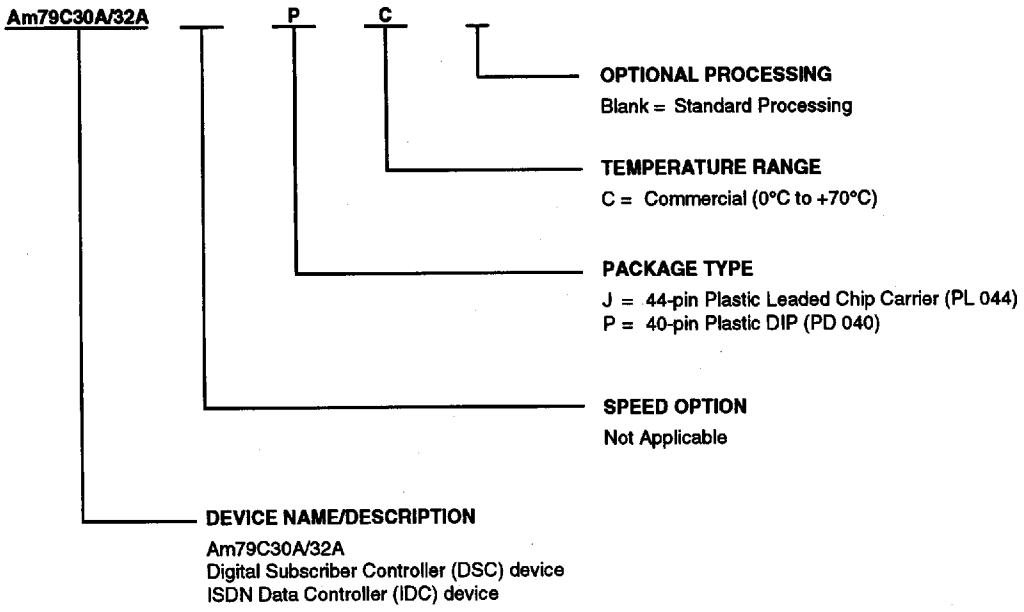
Notes: 1. Pin 1 is marked for orientation purposes.
2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

ADV MICRO (TELECOM)

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C30A	PC, JC
AM79C32A	PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on the AMD standard military grade products.

PIN DESCRIPTION*

Line Interface Unit (LIU)

HSW
Hook-Switch (Input)

The HSW signal indicates if the hook-switch is on or off hook. This signal may be generated with a mechanical switch wired to ground with a pull-up resistor to V_{CC}. Any change in the HSW state causes an interrupt.

LIN1, LIN2
Subscriber Line Input (Differential Inputs)

The LIN1 and LIN2 inputs interface to the subscriber (S reference point) via an isolation transformer. LIN2 is the positive input; LIN1 is the negative input. These pins are not TTL compatible.

LOUT1, LOUT2
Subscriber Line Output (Differential Outputs)

The LOUT1 and LOUT2 line driver output signals interface to the subscriber line at the S reference point via an isolation transformer and resistors. LOUT2 is the positive S-interface driver (sources current during a High mark), and LOUT1 is the negative S-interface driver (sources current during Low mark). For multipoint applications, all TEs must maintain the same polarity on the S Interface. These pins are not TTL compatible.

Main Audio Processor (MAP)

All MAP pins are analog, and therefore are not TTL compatible.

AINA, AINB
Analog (Inputs)

These analog inputs allow for two separate analog (audio) inputs to the transmit path of the codec/filter. Input signals on either of these pins must be referenced to AREF.

AREF
Analog Reference (Output)

This is a nominal 2.4-V reference voltage output for biasing the analog inputs. When the MAP is disabled, this pin is high-impedance.

CAP1, CAP2
Capacitor/Resistor (CAP1, Input; CAP2, Output)

An external resistor and capacitor are connected in series between these pins. These components are needed for the integrator in the Analog-to-Digital Converter (ADC).

EAR1, EAR2
Earpiece Interface (Differential Outputs)

EAR1 and EAR2 are the outputs from the receive path of the codec/filter. These differential outputs can directly drive a minimum load of 540 ohms.

LS1, LS2
Loudspeaker Interface (Differential Outputs)

LS1 and LS2 are push-pull outputs which can directly drive a minimum load of 40 ohms.

Microprocessor Interface (MPI)

A2–A0
Address Line (Inputs)

A2, A1, and A0 signals select source and destination registers for read and write operations on the data bus.

$\overline{CS}$
Chip Select (Input)

$\overline{CS}$ must be Low to read or write to the Am79C30A/32A. Data transfer occurs over the bidirectional data lines (D7–D0).

D7–D0
Data Bus (Bidirectional with High Impedance State)

The eight bidirectional data bus lines are used to exchange information with the microprocessor. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). A High on the data bus line corresponds to a logic 1, and Low corresponds to a logic 0. These lines act as inputs when both $\overline{WR}$ and $\overline{CS}$ are active and as outputs when both $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive or both $\overline{RD}$ and $\overline{WR}$ are inactive, the D7–D0 pins are in a high-impedance state.

$\overline{INT}$
Interrupt (Output)

An active Low output on the $\overline{INT}$ pin informs the external microprocessor that the Am79C30A/32A needs interrupt service. $\overline{INT}$ is updated once every 125 µs. The $\overline{INT}$ pin remains active until the Interrupt Register (IR) is read or the Am79C30A/32A is reset.

RESET
Reset (Input)

Reset is an active High signal which causes the Am79C30A/32A to immediately terminate its present activity and initialize to the reset condition. When reset returns Low, the Am79C30A/32A enters the Idle Mode. The MCLK output remains active while RESET is held High.

* All signal levels are TTL compatible unless otherwise stated.

$\overline{RD}$
Read (Input)

The active Low read signal is conditioned by $\overline{CS}$ and indicates that internal information is to be transferred onto the data bus. A number of internal registers are user accessible. The contents of the accessed register are transferred onto the data bus after the High to Low transition of the $\overline{RD}$ input.

$\overline{WR}$
Write (Input)

The active Low write signal is conditioned by $\overline{CS}$ and indicates that external information on the data bus is to be transferred to an internal register. The contents of the data bus are loaded on the Low to High transition of the $\overline{WR}$ input.

Oscillator (OSC)

MCLK
Master Clock (Output)

The MCLK output is available for use as the system clock for the microprocessor. MCLK is derived from the 12.288-MHz crystal via a programmable divider in the Am79C30A/32A which provides the following MCLK output frequencies: 12.288, 6.144, 4.096, 3.072, 1.536, 0.768, and 0.384 MHz.

XTAL1, XTAL2
External Crystal (Output, Input)

XTAL1 and XTAL2 are connected to an external parallel resonant crystal for the on-chip oscillator. XTAL2 can also be connected to an external source instead of a crystal, in which case XTAL1 should be left disconnected. The frequency must be 12.288 MHz, ± 80 ppm.

Peripheral Port (PP)

SBIN
Serial Data (Input/Output)

When the Peripheral Port is programmed to SBP Mode, SBIN operates as an input for serial data. When the Peripheral Port is programmed to IOM 2 Mode, SBIN functions as the data input except in the special case of IOM 2 Slave Mode, when it becomes an open-drain output during sub-frame 0 or when deactivated.

SBOUT
Serial Data (Input/Output)

When the Peripheral Port is programmed to SBP Mode, SBOUT operates as an output for serial data. When the Peripheral Port is programmed to IOM 2 Mode, SBOUT functions as the data output except in the special case of IOM 2 Slave Mode when it becomes an input during sub-frame 0.

SCLK
Serial Data Clock (Input/Output)

When the PP is programmed to SBP Mode, SCLK outputs a 192-kHz data clock, which may be inverted under software control. When the PP is programmed to IOM 2 Master Mode, SCLK outputs a 1.536-MHz 2X data clock. In IOM 2 Slave Mode, SCLK functions as the clock input. The SCLK pin defaults to a high-impedance state upon reset, but becomes active after any MUX connection is made or if the PP is programmed to IOM 2 Master Mode.

SFS
Serial Frame Sync (Input/Output)

In SBP Mode, SFS outputs an 8-kHz frame synchronization signal. SFS is an output in IOM 2 Master Mode, and an input in IOM 2 Slave Mode. As an output, SFS is active for 8-bit periods. The SFS pin defaults to a high-impedance state upon reset, but becomes active after any MUX connection is made or if the PP is programmed to IOM 2 Master Mode. For SBP Mode, the active signal state is Low during Idle and 8 kHz in Active Data Only and Active Voice and Data Modes.

BCL/CH2STRB
Bit Clock/SBP Channel 2 Strobe
(Output, Three-state) (present only in PLCC package)

In SBP Mode, this pin provides a strobe during the 8-bit times of the second 64-kb/s data channel. In IOM 2 Master Mode, this pin provides a 768-kHz bit clock to aid in the connection of non-IOM 2 devices to the port. In IOM 2 Slave Mode, this pin is high-impedance.

Power Supply Pins

PLCC Packages

AV_{CC}	+5-V analog power supply, ±5% (PLCC only)
AV_{SS}	Analog ground (PLCC only)
DV_{SS}	Digital ground (PLCC only)
DV_{CC}	+5-V digital power supply, ±5% (PLCC only)

DIP Packages

V_{CC}	+5-V power supply, ±5% (DIP only)
V_{SS}	Ground (DIP only)

Note: For best performance, decoupling capacitors should be installed between V_{CC} and V_{SS} as close to the chip as possible. Do not use separate supplies for analog and digital power and ground connections.

OPERATIONAL DESCRIPTION

Overview of Power Modes

The minimization of power consumption is a key factor in the design of Terminal Equipment for the ISDN, and the DSC/IDC circuit employs two basic approaches to power management:

1. The power consumption of the DSC/IDC circuit itself is managed by using four basic power modes which allow unused functional blocks to be disabled. The INIT register may be programmed to select Active Voice and Data, Active Data Only, Idle, or Power-Down Mode, depending upon which DSC/IDC device resources are required at the time.
2. The power consumption of the controlling microprocessor system may be controlled by driving the processor clock with the DSC/IDC circuit MCLK output. A wide range of MCLK operating frequencies may be selected, and a special Clock Speed-up function is provided which increases the speed of MCLK upon the occurrence of a key event, without processor intervention. Control of MCLK frequency and Clock Speed-up is accomplished by programming the INIT and INIT2 registers, as described later.

Active Voice and Data Mode

In Active Voice and Data Mode all functional blocks of the DSC/IDC circuit are available. Device registers may be accessed through the MPI, the LIU and DLC are available, the OSC is running, the Peripheral Port is available, MUX connections may be made, the Secondary Tone Ringer may be activated, and the MAP is operational (DSC circuit only).

Active Data Only Mode

Active Data Only Mode is similar to Active Voice and Data Mode, except that the MAP (DSC circuit only) is disabled to reduce system power consumption. This increases the amount of power available for the Secondary Tone Ringer or microprocessor system during the phases of call setup and teardown, or during a data-only telephone call.

Idle Mode

Idle Mode is the RESET default mode of DSC/IDC circuit operation, and represents an operational state in which power consumption is reduced, yet the microprocessor system is operational to program DSC/IDC circuit registers or perform other required background tasks. Idle Mode may also be entered by appropriate programming of the INIT register.

In Idle Mode, the MCLK output is available to drive the microprocessor system, the MPI is available for programming of DSC/IDC registers, and the LIU is available to initiate or respond to S/T interface activity. The HSW hookswitch interrupt is also available in Idle Mode.

Idle Mode reduces DSC/IDC circuit power consumption by disabling the MUX, DLC, and MAP functional blocks. The Peripheral Port is also disabled, except that an IOM 2 activation request interrupt is possible, and the SFS and SCLK outputs may still be activated. The SFS and SCLK outputs are high-impedance upon RESET, but become active after any MUX connection is programmed. The DLC read-only registers are cleared when the DSC/IDC circuit enters the Idle Mode.

Power-Down Mode

Power-Down Mode consumes the least power of all the DSC/IDC power options, and differs from Idle Mode in that all clocks, including the XTAL oscillator, are stopped. Most functional blocks are disabled, except for those required to recognize key external events that will force the DSC/IDC circuit to return to Idle Mode.

The Power-Down Mode is not available unless the Power-Down Enable bit is set in the INIT2 register; see the INIT2 register description for further details.

Entering the Power-Down Mode

The Power-Down Mode is entered by appropriate programming of the INIT and INIT2 registers. Selection of the Power-Down Mode causes the DSC/IDC circuit to begin an internal countdown of at least 250 MCLK cycles after which the MCLK and XTAL1 outputs are both stopped and held High, and the XTAL2 input will be disregarded. The purpose of this countdown cycle is to allow the microprocessor time for housekeeping operations before its clock is stopped. If an interrupt causes the DSC $\overline{\text{INT}}$ pin to go Low during the countdown, the Power-Down Mode bits in the INIT register will be reset and the countdown will be canceled.

If the LIU is enabled and in any state other than F3 at the end of the countdown, MCLK is stopped but the oscillator continues to run. This allows the LIU to identify the incoming signal and either (1) generate an interrupt and force the DSC/IDC circuit to Idle Mode when activation is complete, or (2) move to the F3 state and stop the oscillator once the line goes idle.

Exiting the Power-Down Mode

The DSC/IDC circuit will exit the Power-Down Mode and enter the Idle Mode if any of the following events occur:

- The DSC/IDC circuit receives a hardware reset via the RESET pin.
- The $\overline{\text{CS}}$ and $\overline{\text{WR}}$ pins are both pulled Low at the same time, as would occur during a normal write operation from the microprocessor to the DSC circuit. No data will be transferred by this operation.
- The HSW hookswitch pin changes state, and the hookswitch interrupt is enabled.

- The LIU receiver is enabled, detects an incoming signal on the S/T Interface, and achieves activation as indicated by a transition to state F7. Both the $\overline{\text{INT}}$ pin and the F7 transition interrupt must be enabled for Power-Down Mode to be exited. If the LIU is enabled, it may restart the oscillator so that it can identify the activity on the interface. If the activity is determined to be noise, the LIU will stop the oscillator and continue to monitor the line without an interrupt or returning to Idle Mode.
- The IOM 2 Interface is enabled as a clock master and the SBIN input pin goes Low. This indicates that a slave device wants to activate the IOM 2 Interface and communicate with the DSC circuit. Both the $\overline{\text{INT}}$ pin and the IOM 2 timing request interrupts must be enabled for Power-Down Mode to be exited.
- The IOM 2 Interface is enabled as a clock slave and the SCLK input pin goes High. This indicates that the master device is activating the IOM 2 Interface and the DSC circuit must wake up in order to monitor the data. Both the $\overline{\text{INT}}$ pin and the IOM 2 timing request interrupts must be enabled for Power-Down Mode to be exited.

If the DSC/IDC circuit is awakened by any condition other than RESET, the MCLK output will be restored to its previously programmed frequency, and will not generate any shortened or spurious output cycles. If the DSC/IDC circuit is revived by RESET, MCLK will default to its normal 6.144-MHz rate. The DSC/IDC circuit provides a minimum of two MCLK cycles prior to activating the interrupt pin when exiting Power-Down Mode.

MCLK Frequency Control

The MCLK frequency selection bits in the INIT register are unchanged from Revision D. However, additional MCLK frequencies are available by programming bits in the INIT2 register. No shortened or spurious clock pulses that might disrupt the external microprocessor will result when the MCLK frequency is changed.

In order to reduce the probability of errant software disrupting system operation, the INIT2 register requires two consecutive writes before the value will be entered into the register. Note that there will be no MCLK countdown as is the case for entering Power-Down Mode if INIT2 is programmed to cause MCLK to STOP, and there will be no shortened or spurious MCLK pulses.

MCLK Clock Speed-up Function

A programmable automatic MCLK speed-up option is provided that will force a hardware reset of INIT2 Bits 3–0, which will cause the MCLK frequency to be restored to the value programmed in the INIT register. There are two events that will trigger the clock speed-up function:

1. The DLC receive FIFO threshold has been reached; or,
2. a second packet begins to be received while data from a prior packet is still in the receive FIFO.

The second packet case requires provision of an interrupt; see the DLC register section for further information. The clock speed-up function allows the user to program a very slow MCLK frequency using INIT2 when D-channel activity is minimal. If a burst of activity is seen on the D Channel which exceeds the programmed threshold of the receive FIFO or threatens to overrun the receive FIFO status buffers, MCLK will instantly toggle back to the higher frequency programmed in the INIT register. This eliminates the latency incurred if an interrupt has to be serviced to change the clock speed, and allows the overall system power to be reduced during typical voice connections. Note that automatic clock speed-up will not function unless at least one of the associated interrupts are enabled so the processor can be informed that the clock speed has been altered.

Global Register Functions

INIT Register (INIT) default = 00H; Address = Indirect 21 Hex, Read/Write

Bit 7 6 5 4 3 2 1 0	Function
X X X X X X 0 0	Idle Mode
X X X X X X 0 1	Active Voice and Data Mode
X X X X X X 1 0	Active Data Only Mode
X X X X X X 1 1	Power-Down Mode
X X X X X 0 X X	$\overline{\text{INT}}$ output enabled
X X X X X 1 X X	$\overline{\text{INT}}$ output disabled
X X 0 0 0 X X X	MCLK frequency = 6.144 MHz
X X 0 0 1 X X X	MCLK frequency = 12.288 MHz
X X 0 1 0 X X X	MCLK frequency = 3.072 MHz
X X 0 1 1 X X X	MCLK frequency = 6.144 MHz
X X 1 0 0 X X X	MCLK frequency = 4.096 MHz
X X 1 0 1 X X X	MCLK frequency = 6.144 MHz
X X 1 1 0 X X X	MCLK frequency = 6.144 MHz
X X 1 1 1 X X X	MCLK frequency = 6.144 MHz
X 0 X X X X X X	DLC receiver abort disabled
X 1 X X X X X X	DLC receiver abort enabled
0 X X X X X X X	DLC transmitter abort disabled
1 X X X X X X X	DLC transmitter abort enabled

INIT2 Register (INIT2) default = 00H; Address = Indirect 20 Hex, Read/Write

A special write procedure must be followed in order to modify the contents of the INIT2 Register, since the INIT2 register includes control bits which could result in the stopping of the microprocessor clock. This procedure greatly reduces the probability of errant software disabling the system, and is described as follows:

1. Write the INIT2 address to the Command Register.
2. Write to the Data Register (INIT2 is not yet updated).
3. Write the INIT2 address to the Command Register.
4. Write to the Data Register (INIT2 is updated).

The writes must take place without any intervening indirect accesses to the DSC/IDC circuit.

Bit 7 6 5 4 3 2 1 0	Function
0 0 X X X X X X	Reserved, must be written to 0 READ's are undefined
0 0 0 X X X X X	Power-Down disabled; writing 11 to the INIT register will put the DSC/IDC circuit into Idle Mode
0 0 1 X X X X X	Power-Down enabled; writing 11 to the INIT register will put the DSC/IDC circuit into Power-Down Mode
0 0 X 0 X X X X	Multiframe Interrupt Filter disabled
0 0 X 1 X X X X	Multiframe Interrupt Filter enabled (see LIU section for detailed description)
0 0 X X 0 X X X	Clock speed-up option disabled
0 0 X X 1 X X X	Clock speed-up option enabled; if set, this register bit will be cleared when the DLC FIFO receive threshold or second packet received interrupt is triggered
0 0 X X X 0 0 0	MCLK frequency determined by INIT register
0 0 X X X 0 0 1	MCLK frequency is 1.536 MHz
0 0 X X X 0 1 0	MCLK frequency is 768 kHz
0 0 X X X 0 1 1	MCLK frequency is 384 kHz
0 0 X X X 1 0 0	MCLK stopped in High state
0 0 X X X 1 0 1	Reserved
0 0 X X X 1 1 0	Reserved
0 0 X X X 1 1 1	Reserved

RESET Operation

The Am79C30A/32A can be reset by driving the RESET pin High. When power is first supplied to the DSC/IDC circuit, a reset must be performed. This initializes the DSC/IDC circuit to its default condition as defined in the following table.

Pin Name	State following RESET
D7–D0	High Impedance
MCLK	6.144 MHz
$\overline{INT}$	Logical 1
SBOUT	High Impedance
SFS	High Impedance
SCLK	High Impedance
LS1, LS2	High Impedance
EAR1	High Impedance
EAR2	High Impedance
AREF	High Impedance
LOUT1	High Impedance
LOUT2	High Impedance

Receive and Transmit Abort Commands

The microprocessor has the option via INIT register bits 6 and 7 to abort the receive and transmit D-channel packets. When the microprocessor sets one of these bits, the Am79C30A/32A aborts the respective operation. The frame abort sequence is defined in greater detail later. (See Data Link Controller section.)

Interrupt Handling

The Am79C30A/32A generates either no interrupt or only one interrupt every 125 µs. Once asserted, $\overline{INT}$ remains active until the microprocessor responds by interrogating the Am79C30A/32A's Interrupt Register (IR) (see Table 1). Reading the IR in response to an activated $\overline{INT}$ pin deactivates the $\overline{INT}$ pin, and clears the IR.

If an event causing an interrupt occurs while the IR is being read by the microprocessor, the effect of the event is held until the microprocessor has completed its read cycle. A reset clears all conditions causing interrupts.

Bits 0,1, and 4 of the IR, if set, advise the microprocessor that the respective buffer is ready for reading or writing. If Bit 0 is set due to an empty buffer, the D-Channel Transmit Buffer must be serviced within 375 µs. If Bit1 is set and the D-Channel Receive Buffer is full, the buffer must be serviced within 425 µs. This is to prevent erroneous data transfers causing transmitter underrun and receiver overrun errors. If Bit 4 is set then the Bb or Bc buffers must be accessed within 122.4 µs. This is to prevent erroneous data transfers. Only one interrupt is used to signal accessibility for both B Channels of the S Interface. Since the data transfer must occur synchronously to the S Interface, any data access to either Bb or Bc or both must be made within the 122.4 µs limit.

Note that even though only a single interrupt is issued, either or both S-interface B Channels must be serviced. IR bits 2, 3, 5, 6, and 7, if set, indicate that a bit has

been set in the associated status or error register. All of the interrupts generated by the Am79C30A/32A can be individually disabled. In the case of IR Bit 7, the interrupt can also be masked by setting PPIER Bit 7 to 0.

DMR1, DMR2, DMR3, LMR2, MCR4, and MF control the mask conditions which affect the $\overline{INT}$ pin. The $\overline{INT}$ pin is activated only by interrupts which are not disabled.

The Interrupt Register reflects the status of enabled interrupts. The $\overline{INT}$ pin can be disabled by setting INIT register bit 2 to a logical 1.

The Am79C30A/32A has facilities that allow the microprocessor to read the status registers (status update is inhibited during status read) or the IR at any time during functional operation.

Table 1. Format of the Interrupt Register (IR), Read Only

Bit	Interrupt Generated/Action Required		Interrupt Mask
0	D-channel transmit threshold interrupt/load D-Channel Transmit Buffer		DMR1 bit 0
1	D-channel receive threshold interrupt/read D-Channel Receive Buffer		DMR1 bit 1
2	D-channel status interrupt/read DSR1		
	Source	Cause	
	DSR1 bit 0	Valid Address (VA) or End of Address (EOA)	DMR3 bit 0
	DSR1 bit 1	When a closing flag is received or a receive error occurs	DMR1 bit 3
	DSR1 bit 6	When a closing flag is transmitted	DMR3 bit 1
3	D-channel error interrupt/read DER and DSR2 bit 2		
	Source	Cause	
	DER bit 0	Current received packet has been aborted	DMR2 bit 0
	DER bit 1	Non-integer number of bytes received	DMR2 bit 1
	DER bit 2	Collision abort detected	DMR2 bit 2
	DER bit 3	FCS error	DMR2 bit 3
	DER bit 4	Overflow error	DMR2 bit 4
	DER bit 5	Underflow error	DMR2 bit 5
	DER bit 6	Overrun error	DMR2 bit 6
	DER bit 7	Underrun error	DMR2 bit 7
	DSR2 bit 2	Receive packet lost	DMR3 bit 6
4	Bb or Bc byte available or buffer empty interrupt/read or write Bb or Bc buffers		MCR4 bit 3
5	LIU status interrupt/read LSR		
	Source	Cause	
	LSR bit 3	Change of state to F3	LMR2 bit 3
	LSR bit 4	Change of state from/to F7	LMR2 bit 6
	LSR bit 5	Change of state from/to F8	LMR2 bit 4
	LSR bit 7	HSW change of state	LMR2 bit 5
6	D-channel status interrupt/read DSR2		
	Source	Cause	
	DSR2 bit 0	Last byte of received packet	DMR3 bit 2
	DSR2 bit 1	Receive byte available	DMR3 bit 3
	DSR2 bit 3	Last byte transmitted	DMR3 bit 4
	DSR2 bit 4	Transmit buffer available	DMR3 bit 5
	DSR2 bit 7	Start of second packet	EFCR bit 1
7	Multiframe or PP interrupt/read MFSB and PPSR		
	Source	Cause	
	MFSB bit 5	S-data available	MF bit 1
	MFSB bit 6	Q-bit buffer empty	MF bit 2
	MFSB bit 7	Multiframe change of state (in/out of sync)	MF bit 3
	PPSR bit 0	Monitor receive, data available	PPIER bit 0
	PPSR bit 1	Monitor transmit, buffer available	PPIER bit 1
	PPSR bit 2	Monitor EOM received	PPIER bit 2
	PPSR bit 3	Monitor abort received	PPIER bit 3
	PPSR bit 4	C/I channel 0, data change	PPIER bit 4
	PPSR bit 5	C/I channel 1, data change	PPIER bit 5
	PPSR bit 6	IOM 2 timing request	PPIER bit 6

FUNCTIONAL DESCRIPTION

Microprocessor Interface (MPI)

The Am79C30A/32A can be connected to any general purpose 8-bit microprocessor via the MPI. The MCLK from the Am79C30A/32A can be used as the clock for the microprocessor. The MPI is an interrupt driven interface containing all the circuitry necessary for access to the internal programmable registers, status registers, coefficient RAM, and transmit/receive buffers.

MPI External Interface

The MPI has the following external connections:

Name	Direction	Function
D7–D0	Bidirectional	Data Bus
A2–A0	Inputs	Address Line
$\overline{RD}$	Input	Read Enable
$\overline{WR}$	Input	Write Enable
$\overline{CS}$	Input	Chip Select
RESET	Input	Initialization
$\overline{INT}$	Output	Interrupt

Direct Registers

Access to the Direct Registers of the Am79C30A/32A is controlled by the state of the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A2, A1, and A0 input pins, as defined below by Table 2.

Indirect Registers

To read from or write to any of the Indirect Registers, an indirect address command is first written to the Command Register (CR). One or more data bytes may then be transferred to or from the selected register through the Data Register (DR).

Registers within certain groups can be quickly accessed by using internal circuitry which automatically increments the indirect value. In Table 3, the "bytes transferred numbers" are the number of bytes which are read or written to the DR after the CR has been loaded. Whenever the CR is loaded, any previous commands are automatically terminated.

Table 2. Direct Register Access Guide

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A2	A1	A0	Register(s) Accessed	Mode
0	1	0	0	0	0	Command Register (CR)	W
0	0	1	0	0	0	Interrupt Register (IR)	R
0	1	0	0	0	1	Data Register (DR)	W
0	0	1	0	0	1	Data Register (DR)	R
0	0	1	0	1	0	D-Channel Status Register 1 (DSR1)	R
0	0	1	0	1	1	D-Channel Error Register (DER) (2-byte FIFO)	R
0	1	0	1	0	0	D-Channel Transmit Buffer (DCTB) (8- or 16-byte FIFO)	W
0	0	1	1	0	0	D-Channel Receive Buffer (DCRB) (8- or 32-byte FIFO)	R
0	1	0	1	0	1	Bb-Channel Transmit Buffer (BBTB)	W
0	0	1	1	0	1	Bb-Channel Receive Buffer (BBRB)	R
0	1	0	1	1	0	Bc-Channel Transmit Buffer (BCTB)	W
0	0	1	1	1	0	Bc-Channel Receive Buffer (BCRB)	R
0	0	1	1	1	1	D-Channel Status Register 2 (DSR2)	R
1	X	X	X	X	X	No access (X = logical 0 or 1)	—

Note: The $\overline{RD}$ and $\overline{WR}$ signals must never both be Low under normal operating conditions.

Table 3. Indirect Register Access Guide

Operation Block	Register	Register Number	Indirect Name	Mode	Address	Byte Sequence
INIT		1	INIT	R/W	21H	One byte transferred
INIT		2	INIT2	R/W	20H	One byte transferred
LIU	LIU Status Register	1	LSR	R	A1H	One byte transferred
LIU	LIU Priority Register	2	LPR	R/W	A2H	One byte transferred
LIU	LIU Mode Register 1	3	LMR1	R/W	A3H	One byte transferred
LIU	LIU Mode Register 2	4	LMR2	R/W	A4H	One byte transferred
LIU	—	5	Perform 2–4	—	A5H	LPR, LMR1, LMR2
LIU	Multiframe Register	6	MF	R/W	A6H	One byte transferred
LIU	Multiframe S-Bit/Status Register	7	MFSB	R	A7H	One byte transferred
LIU	Multiframe Q-Bit Buffer	8	MFQB	W	A8H	One byte transferred
MUX		1	MCR1	R/W	41H	One byte transferred
MUX		2	MCR2	R/W	42H	One byte transferred
MUX		3	MCR3	R/W	43H	One byte transferred
MUX		4	MCR4	R/W	44H	One byte transferred
MUX		5	Perform 1–4	—	45H	MCR1, 2, 3, 4
MAP	X Filter Coefficient Register	1	X Coeff.	R/W	61H	h0 LSB, h0 MSB...h7 MSB
MAP	R Filter Coefficient Register	2	R Coeff.	R/W	62H	h0 LSB, h0 MSB...h7 MSB
MAP	GX Gain Coefficient Register	3	GX Coeff.	R/W	63H	LSB, MSB
MAP	GR Gain Coefficient Register	4	GR Coeff.	R/W	64H	LSB, MSB
MAP	GER Gain Coefficient Register	5	GER Coeff.	R/W	65H	LSB, MSB
MAP	Sidetone Gain Coefficient Register	6	STG Coeff.	R/W	66H	LSB, MSB
MAP	Frequency Tone Generator Register 1, 2	7	FTGR1,FTGR2	R/W	67H	FTGR1, 2
MAP	Amplitude Tone Generator Register 1, 2	8	ATGR1,ATGR2	R/W	68H	ATGR1, 2
MAP	MAP Mode Register 1	9	MMR1	R/W	69H	One byte transferred
MAP	MAP Mode Register 2	10	MMR2	R/W	6AH	One byte transferred
MAP	—	11	Perform 1–10	—	6BH	46 bytes loaded 1–10
MAP	MAP Mode Register 3	12	MMR3	R/W	6CH	One byte transferred
MAP	Secondary Tone Ringer Amplitude	13	STRA	R/W	6DH	One byte transferred
MAP	Secondary Tone Ringer Frequency	14	STRF	R/W	6EH	One byte transferred
DLC	First Received Byte Address Registers 1, 2, 3	1	FRAR1, 2, 3	R/W	81H	FRAR1, 2, 3
DLC	Second Received Byte Address Registers 1, 2, 3	2	SRAR1, 2, 3	R/W	82H	SRAR1, 2, 3
DLC	Transmit Address Register	3	TAR	R/W	83H	LSB, MSB
DLC	D-Channel Receive Byte Limit Register	4	DRLR	R/W	84H	LSB, MSB
DLC	D-Channel Transmit Byte Count Register	5	DTCR	R/W	85H	LSB, MSB
DLC	D-Channel Mode Register 1	6	DMR1	R/W	86H	One byte transferred
DLC	D-Channel Mode Register 2	7	DMR2	R/W	87H	One byte transferred

Table 3. Indirect Register Access Guide (continued)

Operation Block	Register	Register Number	Indirect Name	Mode	Address	Byte Sequence
DLC	—	8	Perform 1–7	—	88H	4 bytes loaded 1–7
DLC	D-Channel Receive Byte Count Register	9	DRCR	R	89H	LSB, MSB
DLC	Random Number Generator Register	10	RNGR1 (LSB)	R/W	8AH	One byte transferred
DLC	Random Number Generator Register	11	RNGR2 (MSB)	R/W	8BH	One byte transferred
DLC	First Received Byte Address Register 4	12	FRAR4	R/W	8CH	One byte transferred
DLC	Second Received Byte Address Register 4	13	SRAR4	R/W	8DH	One byte transferred
DLC	D-Channel Mode Register 3	14	DMR3	R/W	8EH	One byte transferred
DLC	D-Channel Mode Register 4	15	DMR4	R/W	8FH	One byte transferred
DLC	—	16	Perform 12–15	—	90H	FRAR4, SRAR4, DMR3, DMR4
DLC	Address Status Register	17	ASR	R	91H	One byte transferred
DLC	Extended FIFO Control Register	18	EFCR	R/W	92H	One byte transferred
PP	Peripheral Port Control Register 1	1	PPCR1	R/W	C0H	One byte transferred
PP	Peripheral Port Status Register	2	PPSR	R	C1H	One byte transferred
PP	Peripheral Port Interrupt Enable Register	3	PPIER	R/W	C2H	One byte transferred
PP	Monitor Transmit Data Register	4	MTDR	W	C3H	One byte transferred
PP	Monitor Receive Data Register	5	MRDR	R	C3H	One byte transferred
PP	C/I Transmit Data Register 0	6	CITDR0	W	C4H	One byte transferred
PP	C/I Receive Data Register 0	7	CIRDR0	R	C4H	One byte transferred
PP	C/I Transmit Data Register 1	8	CITDR1	W	C5H	One byte transferred
PP	C/I Receive Data Register 1	9	CIRDR1	R	C5H	One byte transferred
PP	Peripheral Port Control Register 2	10	PPCR2	R/W	C8H	One byte transferred

Line Interface Unit (LIU)

The LIU connects to the four-wire S Interface through a pair of isolation transformers, one for the transmit and one for the receive direction, as shown in Figure 1.

The receiver section of the LIU consists of a differential receiver, circuitry for bit timing recovery, circuitry for detecting High and Low marks, and a frame recovery circuit for frame synchronization. The receiver converts the received pseudo-ternary coded signals to binary before delivering them to the other blocks of the Am79C30A/32A. It also performs collision detection (E- and D-bit comparison) per the CCITT recommendations so several TEs can be connected to the same S Interface.

The transmitter consists of a binary to pseudo-ternary encoder and a differential line driver which meets the CCITT recommendations for the S Interface.

The Am79C30A/32A can establish multiframe synchronization, receive S Bits, and transmit Q bits synchronized to the received frame.

External Interface

The LIU can be connected to both point-to-point and point-to-multipoint configurations at the CCITT S reference point. The point-to-point configuration consists of one TE connected to the NT or PABX linecard. The point-to-multipoint configuration can have multiple TEs connected to one NT.

Line Code

Pseudo-ternary coding is used for both transmitting and receiving over the S Interface. In this type of coding, a binary 1 is represented by a space (zero voltage), and a binary 0 is represented by a High mark or a Low mark. Two consecutive binary 0s are represented by alternate

marks to reduce DC offset on the line. A mark followed, either immediately or separated by spaces, by a mark of the same polarity, is defined as a code violation. Code violations are used to identify the boundaries of the frame.

Frame Structures

In both transmit and receive directions, the bits are grouped into frames of 48 bits each. The frame structure is identical for both point-to-point and point-to-multipoint configurations. Each frame transmitted at 4 kHz consists of several groups of bits.

Multiframing

If multiframing is enabled, the Am79C30A/32A recognizes and establishes multiframe synchronization based on the monitoring of the F_A (Q-bit control) and M (M-bit control) Bits. The Am79C30A/32A also receives and compiles S Bits, and transmits Q Bits synchronized to the received frame.

Establishment of Multiframe Synchronization

When the enable multiframe synchronization bit (Bit 0 of the Multiframe Register) is set and the LIU is in state F7, the LIU monitors the F_A (Q-bit control) and M (M-bit control) Bits. When three consecutive multiframes with the M Bits and F_A Bits set as defined in Table 4 are received, the multiframe synchronized bit (Bit 7 of the Multiframe Register) and multiframe change of state bit (Bit 7 of the Multiframe S Bit/Status Buffer) are set. Note that S-bit data is received, compiled and transferred to the user after attaining synchronization at the start of the next multiframe.

S-Bit Reception

The default operation of the DSC/IDC circuit is that the LIU will receive and pass multiframe data to the user in 5-bit increments four times per multiframe, regardless of the value of the data. After multiframe synchronization has been requested and established, the microprocessor can read the Multiframe S Bit/Status Buffer (MFSB) once the S-bit available bit (MFSB Bit 5) is set. The S-data available bit is set to a logical 1 when the Am79C30A/32A has received five S Bits (one S Bit per S-interface frame) synchronized to the setting of the FA-bit to a logical 1 and transferred them into the MFSB. Once the S-bit available bit is set, the MFSB must be accessed within 1.25 ms or succeeding S data will be lost.

Subsequent to the original definition of the DSC/IDC circuit, the CCITT has defined a structure for the 20 multiframe bits, which specifies five 4-bit channels. Furthermore, the idle code for these channels has been defined as 0000. An enhanced mode of multiframe reception has been included, which may be enabled by setting INIT2 Bit 4 to a 1. This enhanced mode reduces processor overhead by generating an interrupt only upon the reception of a non-zero S-channel word. INIT2 Bit 4 will be automatically cleared by hardware when the five received data bits in the MFSB are not all 0s, as long as MF Bit 1 (interrupt enable) is set. This allows subsequent valid all-zero words to be received. Furthermore, when the first five S Bits of the multiframe are loaded into the MFSB, Bit 4 of the MF register will be set, which allows identification of the position of received words within the multiframe.

HSW

The hookswitch circuitry on the DSC circuit provides the attached microprocessor with a way of converting an external mechanical hookswitch into a software status condition capable of generating an interrupt. Debounce and glitch rejection are provided internal to the DSC circuit. The logic rejects glitches less than 162 ns and provides debounce of 16 ms. HSW status reporting is disabled after RESET. It is enabled by any of the following: taking the device out of Idle Mode, a write to a MUX Control register (MCR3–MCR1), or unmasking the HSW interrupt.

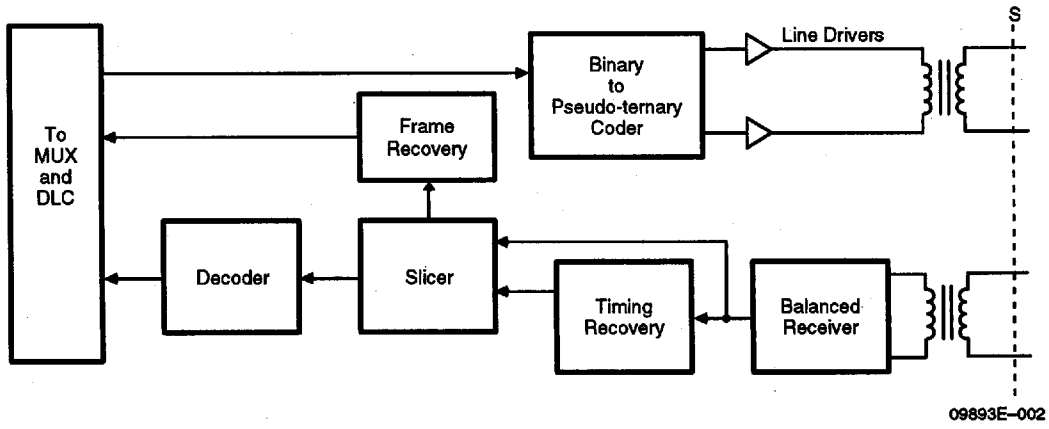


Figure 1. LIU Block Diagram

Table 4. Multiframing Structures

Frame Number	NT-to-TE Q Control Bit FA	NT-to-TE M Bit (M)	NT-to-TE S Bit (S)	TE-to-NT F_A Bit (Q Bit)
1	1	1	SC11	Q1
2	0	0	SC21	0
3	0	0	SC31	0
4	0	0	SC41	0
5	0	0	SC51	0
6	1	0	SC12	Q2
7	0	0	SC22	0
8	0	0	SC32	0
9	0	0	SC42	0
10	0	0	SC52	0
11	1	0	SC13	Q3
12	0	0	SC23	0
13	0	0	SC33	0
14	0	0	SC43	0
15	0	0	SC53	0
16	1	0	SC14	Q4
17	0	0	SC24	0
18	0	0	SC34	0
19	0	0	SC44	0
20	0	0	SC54	0
1	1	1	SC11	Q1
2	0	0	SC21	0
etc.				

Transmission of Q-bits

The microprocessor can load the Multiframe Q-bit Buffer (MFQB) once the Q-bit buffer empty bit (Bit 6 of the Multiframe S Bit/Status Buffer) is set. The Q-bit buffer empty bit is set to a logical 1 at reset or when data that has been written to the Multiframe Q-bit Buffer is transferred to the LIU. The Q-bit buffer empty bit is cleared to a logical 0 when the Multiframe S-bit/Status Buffer is read. After multiframing has been requested and established the Am79C30A/32A transfers the data written into the Q-bit Register to the LIU, synchronized to the multiframe, irrespective of the receipt of valid Q-control bits. If the microprocessor does not reload the Q-bit Register for retransmission, the Q-bit pattern is repeated in the next multiframe.

If multiframing is enabled but multiframe synchronization is not established, the LIU transmits the value loaded in MFQB Bit 4 in all Q Bits. The default value of MFQB Bit 4 is a logical 0 which satisfies the CCITT recommendations. When synchronization is achieved, the contents of MFQB Bits 3 to 0 are transmitted according to Table 4.

Loss of Multiframe Synchronization

The Am79C30A/32A continuously monitors the F_A (Q-bit control) and the M Bits to assure multiframe synchronization. Once multiframe synchronization is established, multiframe synchronization is lost if three consecutive invalid multiframes are received, or the LIU exits state F7, or multiframing is disabled. When loss of multiframe synchronization occurs, Bit 7 of the Multiframe Register is set to a logical 0, and Bit 7 of the Multiframe S Bit/Status Buffer is set to a logical 1. The Am79C30A/32A also terminates the reception of S Bits and transmission of Q Bits until multiframing synchronization is re-established.

LIU Registers

The LIU contains the following registers:

Registers	No./Registers	Mnemonic
LIU Status Register	1	LSR
LIU Priority Register	1	LPR
LIU Mode Registers	2	LMR1, LMR2
Multiframe Register	1	MF
Multiframe S-Bit/Status Register	1	MFSB
Multiframe Q-Bit Buffer	1	MFQB

LIU Status Register (LSR), Read Only; Address = Indirect A1H

The LSR has the following format:

ADV MICRO (TELECOM)

Bit	Logical 1	Generates Interrupt
2,1,0	Binary values 000 through 110 represent the LIU activation circuitry's current state (F2 through F8, respectively) Bit 2 is MSB	No
3	Change of state to F3	If LMR2 bit 3 = 1
4	Change of state from/to F7	If LMR2 bit 6 = 1
5	Change of state from/to F8	If LMR2 bit 4 = 1
6	HSW state	No
7	HSW change of state	If LMR2 bit 5 = 1

When the microprocessor reads the LSR, Bits 3, 4, 5, and 7 are cleared. The other bits retain the current status of the LIU. Bits 0 to 2 are defined such that state F2 (see CCITT I.430 state matrix tables) is coded as 0, F3 as 1, F4 as 2, and so on, where Bit 0 is the LSB. The LIU interrupts the microprocessor via Bit 4 of the LSR when activation has been achieved (that is, when the LIU moves to state F7 upon receipt of INFO 4). During reset the LSR is 0.

Even though the LIU Status Register (LSR) is read-only, no default value upon power-up is given due to the uncertain state of Bit 6 (Hookswitch State). Following RESET, The LIU State is F2 and the HSW bit reflects the HSW pin, producing a power-up value of either 00H or 40H.

LIU D-Channel Priority Register (LPR), Read/Write

The LPR contains the priority level for D-channel access. Its default value after reset is 0.

The D-channel access procedure of the Am79C30A/32A uses the priority level programmed in the LPR. The priority mechanism defined by the CCITT I-series recommendations is fully implemented if the LPR is programmed via the microprocessor to conform to the priority class of the Layer-2 frame to be transmitted. The LPR has 16 possible programmable priority levels. The priority levels are numbered 0–15. Priority Level 0 corresponds to counting eight 1s in the echo channel, priority Level 1 corresponds to counting ten 1s in the echo channel, priority Level 2 corresponds to counting twelve 1s, etc. The DSC circuit automatically handles transitions between the programmed priority level n and the associated odd value n+1. The priority is incremented following a successfully transmitted packet, and decremented when the higher count has been satisfied.

The LPR has the following format:

Bits	Description
3,2,1,0	D-channel access priority level Bit 0 is LSB
7,6,5,4	Reserved, reads logical 0

LIU Mode Register (LMR1), Read/Write; Address = Indirect A3H

LMR1 is defined as follows:

Bit	Logical 1	Logical 0 (default value)
0	Enable B1 transmit	Disable B1 transmit
1	Enable B2 transmit	Disable B2 transmit
2	Disable F transmit	Enable F transmit
3	Disable F_A transmit	Enable F_A transmit
4	Activation request	No activation request
5	Go from F8 to F3	No transition
6	Enable receiver/transmitter	Disable receiver/transmitter
7	Reserved; must be set to logical 0	Reserved; must be set to logical 0

The F and F_A Bits in LMR1 (Bits 2 and 3) should be enabled during the activation procedure so the Am79C30A/32A can respond with INFO 3.

LMR1 Bit 4 is used to transfer the signals PH-AR and Expiry of Timer from the microprocessor to the LIU (see CCITT I.430 state diagram—activation request). PH-AR is defined as Bit 4 being a logical 1 and Expiry of Timer is defined as the transition of Bit 4 from a logical 1 to a logical 0. This bit must not be set until the LIU, as reflected in the LSR, is in state F3, F6 or F7 and the receiver has been enabled for a minimum of 250 µs.

LMR1 Bit 6 is primarily used to disable the receiver when the terminal does not require access to the S Interface signals. This bit is cleared by reset and must be written to logical 1 in order to receive activation from the S Interface, or to request activation.

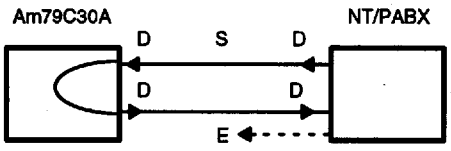
LIU Mode Register 2 (LMR2), Read/Write; Address = Indirect A4H

LMR2 is used to select the following operations: ADV MICRO (TELECOM)

Bit	Logical 1	Logical 0 (Default Value)
0	D-channel loopback at Am79C30A/32A enable	D-channel loopback at Am79C30A/32A disable
1	D-channel loopback at LIU enable	D-channel loopback at LIU disable
2	D-channel back-off disable	D-channel back-off enable
3	F3 change of state interrupt enable	F3 change of state interrupt disable
4	F8 change of state interrupt enable	F8 change of state interrupt disable
5	HSW interrupt enable	HSW interrupt disable
6	F7 change of state interrupt enable	F7 change of state interrupt disable
7	Reserved; must be set to logical 0	Reserved; must be set to logical 0

The three D-channel loopback controls defined in LMR2 Bits 0, 1, and 2 are explained below:

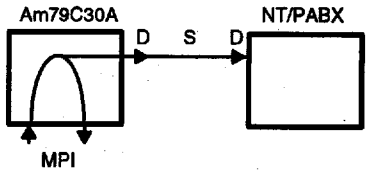
Bit 0, D-channel loopback at Am79C30A/32A enable:



This remote loopback is provided for maintenance purposes from the NT's perspective. The NT transmits D-channel bits to the Am79C30A/32A where they are internally looped (with the Data Link Controller) and transmitted back to the NT. The incoming D-channel data can be accessed by the microprocessor; however, the microprocessor cannot send data on the outgoing D Channel.

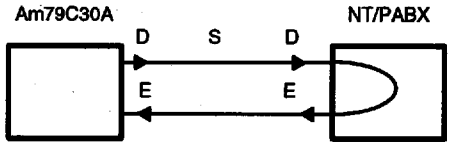
Any difference between the transmitted D-channel bits and the received E-channel bits to/from the Am79C30A/32A (normally detected as an error which halts the transmission) is ignored, thereby allowing the transmission to continue.

Bit 1, D-channel loopback at LIU enable:



This local loopback is provided for local testing. Data on the incoming D Channel is ignored. The data from the microprocessor is processed by the DLC and then looped back to the microprocessor in addition to being output to the S Interface.

Bit 2, D-channel back-off disable:



This loopback is provided for maintenance purposes from the TE's perspective. The Am79C30A/32A transmits D-channel bits to the NT where they are looped and transmitted back to the Am79C30A/32A in the E Channel. The operation is normal except differences between the D and E Channels do not halt the transmission.

Multiframe Register (MF), Read/Write; Address = Indirect A6H

Bit	Logical 1	Logical 0 (Default Value)
0	Enable multiframe synchronization	Disable multiframe synchronization
1	Enable S-data available interrupt	Disable interrupt
2	Enable Q-bit buffer empty interrupt	Disable interrupt
3	Enable Multiframe change of state interrupt	Disable interrupt
4	First subframe	Not first subframe
6,5	Not used, reads logical 0	Not used, reads logical 0
7	Multiframe synchronized (read only)	Multiframe not synchronized (read only)

Multiframe S-bit/Status Buffer (MFSB), Read Only; Address = Indirect A7H

Bit	Description	Generates Interrupt
0	S1	No
1	S2	No
2	S3	No
3	S4	No
4	S5	No
5	S-data available	If MF bit 1 = 1
6	Q-bit buffer empty	If MF bit 2 = 1
7	Multiframe change of state	If MF bit 3 = 1

The MFSB reset default value is 40H.

Multiframe Q-bit Buffer (MFQB), Write Only; Address = Indirect A8H

Bit	Description
0	Q1 (default = 1)
1	Q2 (default = 1)
2	Q3 (default = 1)
3	Q4 (default = 1)
4	Q-bit value when multiframing enabled but synchronization not achieved (default = 0)
5,6,7	Not used

Multiplexer (MUX)

The MUX contains the following registers:

Register	No./Registers	Mnemonic
MUX Control Registers	4	MCR1, MCR2, MCR3, MCR4

The Multiplexer is used to selectively route 64-kb/s full-duplex B Channels between the LIU (Line Interface Unit), MAP (Main Audio Processor), MPI (Microprocessor Interface), and the PP (Peripheral Port).

The logical channels available at the MUX are shown in Figure 2. They are:

1. From/to the LIU Channels B1 and B2
2. From/to the MAP Channel Ba
3. From/to the MPI Channels Bb and Bc
4. From/to the PP Channels Bd, Be, and Bf

For any specific application, the MUX can be programmed by the microprocessor to route any three B-channel ports to any other three B-channel ports. Programmable bidirectional bit reversal is provided for both of the MPI data channels Bb and Bc.

MUX Control Registers 1, 2, and 3 (MCR1, MCR2, and MCR3), Read/Write; Addresses = Indirect 41H, 42H, 43H

The MUX can support three bidirectional paths. The contents of the MUX Control Registers MCR1, MCR2, and MCR3 direct the flow of data between the eight MUX logical B Channels (see Figure 2). These three MCRs are programmed to connect any two B-channel ports together by writing the appropriate channel code into an MCR. These MCRs have the same format, where Bits 7–4 indicate port 1 and Bits 3–0 indicate port 2. In each of these three MCR registers, the following channel codes are used for both ports 1 and 2:

MCR Register Channel Codes

Code	Channel
0000	No connection (default value)
0001	B1 (LIU)
0010	B2 (LIU)
0011	Ba (MAP)
0100	Bb (MPI)
0101	Bc (MPI)
0110	Bd (PP channel 1)
0111	Be (PP channel 2)
1000	Bf (PP channel 3)

For example, to connect B1(LIU) with Bb (MPI) and B2 (LIU) with Ba (MAP), the contents of the MCRs would be:

Register	Port1 / Port2 7 6 5 4 3 2 1 0	Channel Connection
MCR1	0 0 0 1 0 1 0 0	B1 (LIU)<—>Bb (MPI)
MCR2	0 0 1 0 0 0 1 1	B2 (LIU)<—>Ba (MAP)
MCR3	0 0 0 0 0 0 0 0	No connect<->No connect

Therefore, in this example, MCR1 provides a data link from the S Interface and MCR2 sets up a voice connection across the S Interface.

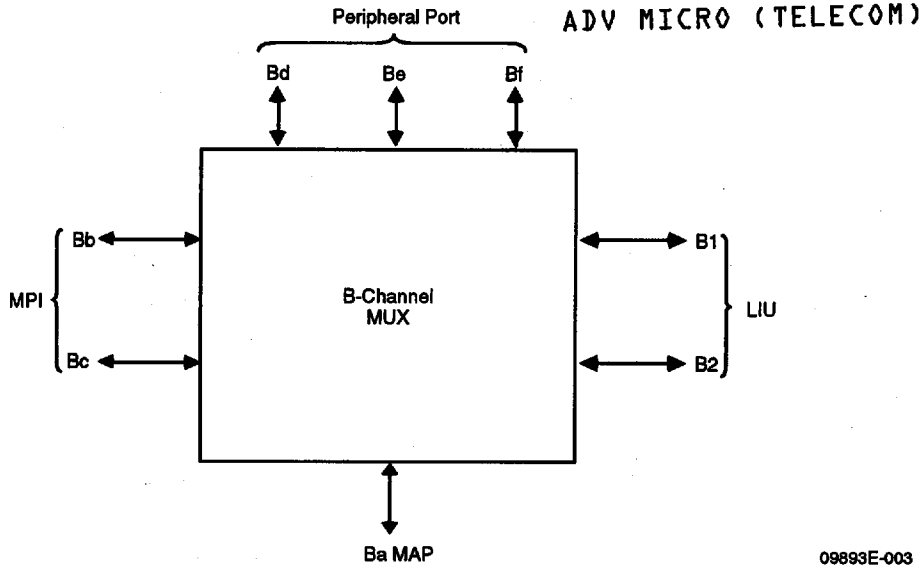


Figure 2. MUX Logical Channels

To loopback a channel, the same channel code is used for port 1 and port 2. For example, to loopback B1, B2, and Ba, the MCRs would be:

Register	Port1 / Port2 7 6 5 4 3 2 1 0	Channel Connection
MCR1	0 0 0 1 0 0 0 1	B1 (LIU) Loopback
MCR2	0 0 1 0 0 0 1 0	B2 (LIU) Loopback
MCR3	0 0 1 1 0 0 1 1	Ba (MAP) Loopback

MCR3 has higher priority than MCR2. MCR2 has higher priority than MCR1.

If multiple connections are made to the same port, the data from the connecting ports in the highest priority MCR will overwrite the data from the connecting port in the lower priority MCR, for example:

Register	Port1 / Port2 7 6 5 4 3 2 1 0	Channel Connection
MCR1	0 0 0 0 0 0 0 0	No connect
MCR2	0 0 0 1 0 1 0 0	B1 (LIU)<—>Bb (MPI)
MCR3	0 1 0 0 0 0 1 1	Bb (MPI)<—>Ba (MAP)

The final data transfers are:

B1 (LIU) receives Bb (MPI),
Ba (MAP) receives Bb (MPI),
Bb (MPI) receives Ba (MAP).

Therefore, the data transfer from B1(LIU) to Bb(MPI) is lost in the arrangement proposed in MCR2.

MUX Control Register 4 (MCR4), Read/Write; Address = Indirect 44H

The MUX Control Register 4 (MCR4) can prevent interrupt generation by masking the output of IR Bit 4. MCR4 has the following format:

Bit	Logical 1	Logical 0 (Default Value)
2,1,0	Reserved, must be set to logical 0	Reserved, must be set to logical 0
3	Enable Bb- or Bc-channel byte available interrupt (IR Bit 4)	Disable interrupt
4	Reverse bit order of Bb (LSB transmitted/received first)	No Bb bit reversal (MSB transmitted/received first)
5	Reverse bit order of Bc (LSB transmitted/received first)	No Bc bit reversal (MSB transmitted/received first)
6	Reserved, must be set to logical 0	Reserved, must be set to logical 0
7	Reserved, must be set to logical 0	Reserved, must be set to logical 0

Main Audio Processor (MAP)

(Am79C30A Only)

Overview

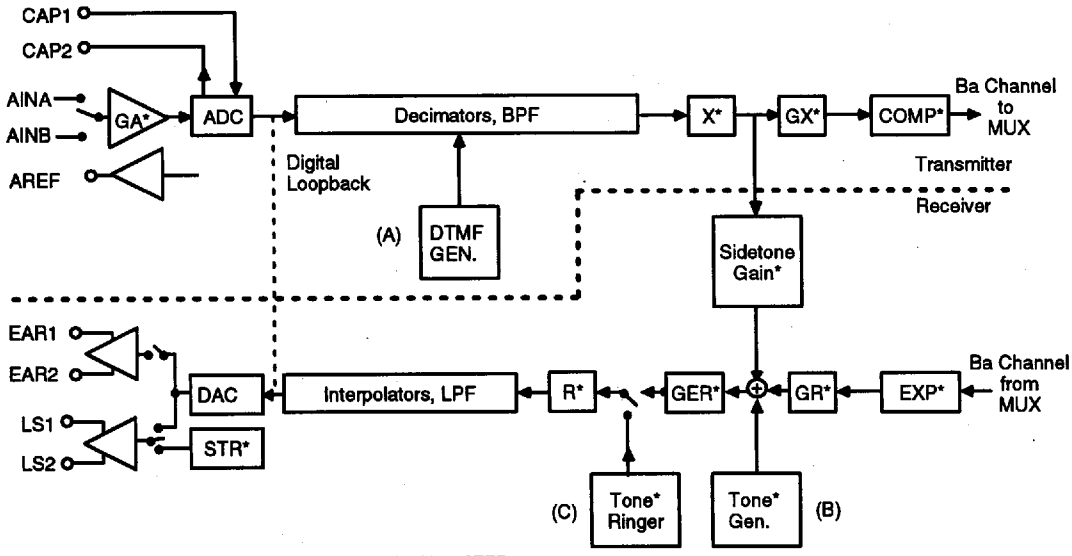
The MAP, as illustrated in Figure 3, implements audio-band analog-to-digital (ADC) and digital-to-analog (DAC) conversions together with a wide variety of audio support functions. Analog interfaces are provided for a handset earpiece, a handset mouthpiece, a microphone, and a loudspeaker. A programmable analog preamplifier is included in front of the A/D converter. The codec and filter functions are implemented using digital signal processing (DSP) techniques to provide operational stability and programmable features. There is one programmable digital gain stage in the transmit path and two in the receive path to allow precise signal level control. Sidetone attenuation is programmable, and programmable equalization filters are present in both the receive and transmit paths in order to modify the frequency response of either or both paths. Tone generation capability is included to allow generation of ringing signals, DTMF tones, and call progress signals. MAP operation is described in detail in the following sections.

Audio Inputs

The audio input port consists of two inputs (AINA and AINB) which are selectable, one at a time, by register programming. Signals applied to these inputs must be AC-coupled.

Earpiece and Loudspeaker Drivers

The earpiece and loudspeaker drivers each consist of amplifiers with differential, low-impedance outputs. The MAP receive path signal may be routed to either of these outputs, or to both outputs simultaneously. Alternatively, the MAP receive path may be routed to the EAR outputs while the Secondary Tone Ringer (STR) is routed to the LS outputs. The EAR drivers can drive loads ≥540 ohms between the EAR1 and EAR2 pins, while the LS drivers can drive loads ≥40 ohms between the LS1 and LS2 pins. The maximum capacitive-loading between EAR1 and EAR2 or between LS1 and LS2 is 100 pF. The EAR outputs are high-impedance when the MAP is disabled. The LS outputs are high impedance when both the MAP and the Secondary Tone Ringer are disabled.



	MINIMUM	DEFAULT	MAXIMUM	STEP
GX	0 dB**	0 dB	12 dB	0.5 dB
GER	−10 dB**	0 dB	18 dB	0.5 dB
GR	−12 dB**	0 dB	0 dB	0.5 dB
STG	−18 dB**	−18 dB	0 dB	0.5 dB
GA	0 dB	0 dB	24 dB	6.0 dB

09893E-004

* Programmable
**These registers can also be programmed for infinite attenuation to break the signal path if desired.

Figure 3. Main Audio Processor Block Diagram

Programmable Analog Preamplifier

A programmable analog preamplifier GA is included in front of the A/D converter, and is adjustable in 6-dB increments from 0 dB to +24 dB. The existing GX gain stage in the transmit path may be used for finer adjustment of transmit gain. This preamplifier eliminates the need for an external operational amplifier when interfacing electret-type handsets to the DSC circuit.

Signal Processing

Transmitter

The transmitter performs a series of operations as described below:

1. An ADC converts the incoming analog signal at a sampling rate of 512 kHz.
2. The Band Pass Filter and a series of decimators reject DC and 50- to 60-Hz line frequencies while reducing the sampling rate to 8 kHz.
3. The X filter is an 8-tap user-programmable filter for tuning the microphone. The default is flat with unity gain.
4. The GX filter is a programmable gain filter that allows the user to program a gain of 0 to +12 dB in 0.5-dB steps. The default value is 0 dB.
5. The μ-law or A-law digital compression algorithm converts the linear output of the GX filter to μ- or A-law code. The default algorithm is μ-law code. The MSB (sign bit) is transferred first to (or from) the MUX.

Receiver

The receiver performs a series of operations described as follows:

1. An expander converts the input A- or μ-law data to digital linear data. The most significant bit is transferred from the MUX first. The default value is μ-law.
2. The GR filter is a programmable gain filter that allows the user to program a gain of –12 to 0 dB in 0.5-dB steps. The default value of GR is 0 dB.
3. The GER and Sidetone Gain (STG) are programmable constant multipliers which allow the user to program a gain of –10 to +18 dB in 0.5-dB steps (default value 0 dB) and –18 to 0 dB in 0.5-dB steps (default value –18 dB) respectively. The GER provides volume control (for the hearing impaired) and should be programmed to 0 dB for normal operation. The sidetone gain path provides feedback from the transmitter.
4. The R filter is provided to correct for speaker attenuation distortion and is a user-programmable filter similar to the X filter in the transmitter.
5. A series of interpolators increases the sampling frequency.
6. A DAC converts the digital signal to the analog audio output signal.

Tone Generators

The MAP contains three tone generators which can be enabled via MAP Mode Register 2 Bits 2, 3, and 4. Only one of the three tone generator bits in the register can be set at a time. If more than one bit is set, all three bits are considered set to zero and tone generation is disabled. The tone generators are:

DTMF Generator

This generator provides tone injection at a sampling rate of 32 kHz into the transmit and sidetone paths (Figure 3, Block A). The DTMF frequencies generated are guaranteed to ±1.2% deviation.

Tone Generation

This generator provides call progress tones to the receive path, where it is added to the incoming speech (Figure 3, Block B).

Tone Ringer

This generator provides tone alert signals output through the receive path to the loudspeaker or earpiece (Figure 3, Block C).

To program the DTMF tone generators, two frequency values and two amplitude values must be written to the two 8-bit Frequency Tone Generator Registers (FTGR1, FTGR2) and the two 8-bit Amplitude Tone Generator Registers (ATGR1, ATGR2), respectively.

The Tone Generator and the Tone Ringer use the frequency programmed in FTGR1. The Tone Generator uses the amplitude programmed in ATGR1 while the Tone Ringer uses the amplitude programmed in ATGR2.

The FTGR codes to obtain DTMF dialing output frequencies are listed in the table below:

FTGR 1 OR 2 (HEX REG VALUE)	FREQ	FTGR 2 or 1: 9BH	ABH	BFH	D3H
		1209	1336	1477	1633
5AH	697	1	2	3	A
63H	770	4	5	6	B
6EH	852	7	8	9	C
79H	941	*	0	#	D

The output frequency of the DTMF tone generator approximately equals :

$$\text{DTMF Frequency in Hz} = \frac{64000}{\text{integer}\,(8192/i) + 1}$$

where i is the decimal equivalent of value programmed into the FTGR register. This allows the DTMF generator to supply common dual tone call progress signals such as Busy or Dial tones.

Table 5. Tone Ringer and Tone Generator Frequency Coefficients

Frequency (Hz)	Hex Code
2666	AB
2000	81
1600	67
1333	56
1142	4A
1000	41
889	39
800	34
727	2F
667	2B
615	28
571	25
533	23
500	21
471	1F
444	1D
421	1B
400	1A
381	19
364	18
348	17
333	16
320	15

Note: These coefficients do not apply to the DTMF generator.

The ATGR registers allow the user to program a gain of –18 dB to 0 dB in 2-dB steps. Example ATGR codes to obtain amplitude gains are listed in the following table.

0 dB implies a level of +3 dBm0. The gain values are rounded off to the nearest 1 dB.

Amplitude Gain Coefficients

Gain (dB)	Hex Code
–18	37
–16	32
–14	31
–12	27
–10	22
–8	21
–6	20
–4	12
–2	11
0	10

Secondary Tone Ringer

A Secondary Tone Ringer is included, which is able to ring the phone using the LS outputs while a voice conversation is in progress on the EAR outputs. The STR is louder than the Tone Generator, and may be used with or without enabling the MAP in order to provide flexible control of system power consumption. The STR is not available if the INIT register is programmed to Idle or Power-Down Mode. The amplitude and frequency of the STR square-wave output waveform is programmable via the STRA and STRF registers, respectively. If both the LS outputs from the MAP receive path and the STR are simultaneously enabled, priority is given to the STR connection. The STR is available for both the DSC and IDC circuits. A legal value must be programmed in the STRF register before the STR is enabled.

Programmable Gain Coefficients

The GER, GR, GX, and Sidetone gain coefficients are each 16 bits in length. Two consecutive register locations correspond to one gain coefficient. The LSB is transferred first to (or from) the microprocessor. Sample coefficients for the GER filter are listed in Table 6. The gain values are rounded off to the nearest 0.1dB.

Table 6. GER Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB	Gain (dB)	Hex Code MSB	Hex Code LSB
−10.0	AA	AA	4.0	31	DD
−9.5	9B	BB	4.5	44	1F
−9.0	79	AC	5.0	43	1F
−8.5	09	9A	5.5	33	1F
−8.0	41	99	6.0	40	DD
−7.5	31	99	6.5	11	DD
−7.0	9C	DE	7.0	44	0F
−6.5	9D	EF	7.5	41	1F
−6.0	74	9C	8.0	31	1F
−5.5	54	9D	8.5	55	20
−5.0	6A	AE	9.0	10	DD
−4.5	AB	CD	9.5	42	11
−4.0	AB	DF	10.0	41	0F
−3.5	74	29	10.5	11	1F
−3.0	64	AB	11.0	60	0B
−2.5	6A	FF	11.5	00	DD
−2.0	2A	BD	12.0	42	10
−1.5	BE	EF	12.5	40	0F
−1.0	5C	CE	13.0	11	0F
−0.5	75	CD	13.4	22	10
0.0	00	99	14.0	72	00
0.5	55	4C	14.5	42	00
1.0	43	DD	15.0	21	10
1.5	33	DD	15.5	10	0F
2.0	52	EF	15.9	22	00
2.5	77	1B	16.6	11	10
3.0	55	42	16.9	00	0B
3.5	41	DD	17.5	21	00
			18.0	00	0F

Note: The coefficient 0008 provides an attenuation of infinity when GER gain is enabled.

Example coefficients for the GR, GX, and STG filters are listed in the following table. The gain values are rounded off to the nearest 0.1 dB.

GX Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB
0.0	08	08
0.5	4C	B2
1.0	3D	AC
1.5	2A	E5
2.0	25	33
2.5	22	22
3.0	21	22
3.5	1F	D3
4.0	12	A2
4.5	12	1B
5.0	11	3B
5.5	0B	C3
6.0	10	F2
6.5	03	BA
7.0	02	CA
7.5	02	1D
8.0	01	5A
8.5	01	22
9.0	01	12
9.5	00	EC
10.0	00	32
10.5	00	21
11.0	00	13
11.5	00	11
12.0	00	0E

GR Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB
−12.0	91	F9
−11.5	91	C5
−11.0	91	B6
−10.5	92	12
−10.0	91	A4
−9.5	92	22
−9.0	92	32
−8.5	92	FB
−8.0	92	AA
−7.5	93	27
−7.0	93	B3
−6.5	94	B3
−6.0	9F	91
−5.5	9C	EA
−5.0	9B	F9
−4.5	9A	AC
−4.0	9A	4A
−3.5	A2	22
−3.0	A2	A2
−2.5	A6	8D
−2.0	AA	A3
−1.5	B2	42
−1.0	BB	52
−0.5	CB	B2
0.0	08	08

STG Gain Coefficients

Gain (dB)	Hex Code MSB	Hex Code LSB
−18.0	8B	7C
−17.5	8B	44
−17.0	8B	35
−16.5	8B	2A
−16.0	8B	24
−15.5	8B	22
−15.0	91	23
−14.5	91	2E
−14.0	91	2A
−13.5	91	32
−13.0	91	3B
−12.5	91	4B
−12.0	91	F9
−11.5	91	C5
−11.0	91	B6
−10.5	92	12
−10.0	91	A4
−9.5	92	22
−9.0	92	32
−8.5	92	FB
−8.0	92	AA
−7.5	93	27
−7.0	93	B3
−6.5	94	B3
−6.0	9F	91
−5.5	9C	EA
−5.0	9B	F9
−4.5	9A	AC
−4.0	9A	4A
−3.5	A2	22
−3.0	A2	A2
−2.5	A6	8D
−2.0	AA	A3
−1.5	B2	42
−1.0	BB	52
−0.5	CB	B2
0.0	08	08

The coefficient 9008 provides an attenuation of infinity when GR, GX, and/or STG are enabled.

Overflow/Underflow Precautions When Using Programmable Gains

Care must be taken so that at *any* point in the signal processing path, the combination of gains and filters and/or tones does not result in a signal that is larger than full scale. Full scale is defined as the digital representation of the maximum analog signal that is allowed into the transmitter or out of the receiver with all filters and gain stages at their default (0 dB) settings (e.g., in A-Law, the transmitter full scale is $\pm 1.25\ V_P$ and the receiver full scale is $\pm 2.5\ V_P$). Likewise, it is desirable that the peak signal be kept as close to full scale as possible at any point in the signal processing path in order to minimize digital truncation effects in the A/D, D/A, and MAP DSP.

Consider the following example: STG is programmed for infinite attenuation, GR is programmed to −6 dB while GER is programmed to +12 dB, and the R filter is

programmed to exhibit a net gain of –6 dB. Assume the analog full scale out of the receiver is ±2.5 V_P, and a full scale PCM code is possible from the MUX. After GR, the equivalent analog signal will be 2.5/2 = ±1.25 V_P. However, after GER the signal will be 1.25 · 4, or ±5 V_P. Even though the R filter will have a net gain of –6 dB, the signal will be clipped after GER and distorted for PCM codes between full scale and 6 dB below full scale due to the intermediate result at the output of GER.

Be very careful when programming the tone ringers/ generators. For example, if one of the DTMF tones is programmed to 0 dB, a tone is generated that is equivalent to a ± full scale signal in the transmit path. This means no headroom is left for the other DTMF tone. Therefore, the DTMF generator should never be programmed to exceed full scale if signal quality is to be maintained. In the receive path, similar caution should be exercised in order to prevent the combination of Tone Generator, Sidetone, GR, and GER from clipping the signal.

Programmable Filter Coefficients and Equations

The frequency domain transfer function equation for the X and R filters is:

$$h_f = h_0 + h_1z^{-1} + h_2z^{-2} + h_3z^{-3} + h_4z^{-4} + h_5z^{-5} + h_6z^{-6} + h_7z^{-7}$$

where:

$z = \cos(wT) + i \cdot \sin(wT)$
$i = (-1)^{1/2}$
w = frequency of input signal in Hz · 2pi
T = sample period in seconds (0.125 ms)
hj (j = 0,1,...7) = user defined coefficients.

Each hj coefficient is defined by the following equation:

$$hj = A3\{1 + A2[1 + A1(1 + A0)]\}$$

where each hj Coefficient Register pair has the following format:

Byte	7	6 5 4	3	2 1 0
LSB	S1	M1	S0	M0
MSB	S3	M3	S2	M2

and $Ai = -1^{Si}2^{-Mi}$, (i=0,1,2,3).

The X and R filter coefficients are programmed using a 16-byte transfer with the following format:

Byte	Value
0	h0 LSB
1	h0 MSB
2	h1 LSB
3	h1 MSB
4	h2 LSB
5	h2 MSB
6	h3 LSB
7	h3 MSB
8	h4 LSB
9	h4 MSB
10	h5 LSB
11	h5 MSB
12	h6 LSB
13	h6 MSB
14	h7 LSB
15	h7 MSB

AmMAP™ software, which calculates X and R filter coefficients, is available from Advanced Micro Devices. Contact your local AMD® Sales Office for more information.

Test Facilities

Three capabilities are provided for MAP operation verification:

MAP Analog Loopback

Signals sent in on AINA or AINB may be sent back out to EAR1/EAR2 or LS1/LS2 by looping the MAP path in the MUX. The MUX should be set up for Ba-to-Ba loopback by writing 33H to MCR1, MCR2, or MCR3. No other MUX connections overriding Ba-to-Ba should be programmed. This test allows the MAP analog and digital to be tested using a local signal source.

MAP Digital Loopback 1

This loopback mode connects the interpolator output to the decimator input, in place of the ADC output. This mode allows verification, from the S Interface or microprocessor, that the MAP digital circuitry is functional. Note that the digital patterns received after loopback will not be identical to the transmitted patterns. The D-D gain is approximately 2.5 dB.

MAP Digital Loopback 2

This loopback mode connects the analog D/A output path to the analog A/D input path, internal to the DSC circuit. The EAR and LS outputs and both AIN inputs will be disabled. This mode allows verification, from the S Interface or microprocessor, that the MAP analog and digital circuitry are functional. The digital patterns

received after loopback will not be identical to the transmitted patterns.

The bits in the MAP Mode Register define the enable/disable options for the various MAP configurations as follows:

MAP Registers

The MAP contains the following programmable registers:

MAP Register	# Bytes	Mnemonic
X-Filter Coefficient Register	16	X
R-Filter Coefficient Register	16	R
GX-Gain Coefficient Register	2	GX
GR-Gain Coefficient Register	2	GR
GER-Gain Coefficient Register	2	GER
Sidetone-Gain Coefficient Register	2	STGR
Frequency Tone Generator Register	2	FTGR
Amplitude Tone Generator Register	2	ATGR
MAP Mode Registers (3)	1	MMR
Secondary Tone Ringer Amplitude Reg.	1	STRA
Secondary Tone Ringer Frequency Reg.	1	STRF

Note: It is necessary to complete any transfers to the multi-byte MAP registers. For instance, a total of 16 bytes must be transferred to update the X filter.

Following reset, the MAP registers FTGR, MMR1, MMR2, MMR3, STRA, and STRF all default to 00 hex. All other MAP registers are not affected by reset and must be programmed by the microprocessor before being enabled. When the registers are disabled, or after reset, the MAP will have the following response:

Filter	Default Response
X Filter	Disabled (0 dB, Flat)
R Filter	Disabled (0 dB, Flat)
GX Filter	Disabled (0 dB, Gain)
GR Filter	Disabled (0 dB, Gain)
GER Filter	Disabled (0 dB, Gain)
Sidetone gain	Disabled (–18 dB, Gain)

MAP Mode Register 1 — (MMR1) — Read/Write

Address = Indirect 69H

Bit	Logical 1	Logical 0 (default mode)
0	A-Law	μ-Law
1	GX coefficient loaded from register	GX bypassed; gain = 0 dB
2	GR coefficient loaded from register	GR bypassed; gain = 0 dB
3	GER coefficient loaded from register	GER bypassed; gain = 0 dB
4	X coefficient loaded from register	X bypassed; response = flat
5	R coefficient loaded from register	R bypassed; response = flat
6	Sidetone gain coefficient loaded from register	STG gain = –18 dB*
7	Digital loopback at MAP enabled	Digital loopback at MAP disabled

*To remove the sidetone path completely, it is necessary to enable the STG function by setting MMR1 Bit 6 to 1, and program the STGR coefficient to 9008 (hex).

MAP Mode Register 2 — (MMR2) — Read/Write

Address = Indirect 6AH

Bit	Logical 1	Logical 0 (default mode)
0	AINB selected	AINA selected
1	LS1/LS2 selected	EAR1/EAR2 selected
2	DTMF enabled	DTMF disabled
3	Tone generator enabled	Tone generator disabled
4	Tone ringer enabled	Tone ringer disabled
5	High pass filter disabled	High pass filter enabled
6	ADC auto-zero function disabled	ADC auto-zero function enabled
7	Reserved, must be Logical 0	Reserved, must be Logical 0

Note: For most applications, MMR2 Bits 5 and 6 should always be written to logical 0. This enables the 50–60 Hz rejection filter and the internal offset cancellation circuits to operate normally. They can both be disabled when system or test conditions require the transmission of DC or low frequency signals.

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Map Mode Register 3—(MMR3)—Read/Write
Address Indirect 6CH

Bit 7	6	5	4	3	2	1	0	Function
0	X	X	X	X	X	X	X	Bit 7 Reserved, must be written to 0
0	0	0	0	X	X	X	X	0-dB pre-amplifier gain, 1.250-V maximum peak input voltage
0	0	0	1	X	X	X	X	+6-dB pre-amplifier gain, 0.625-V maximum peak input voltage
0	0	1	0	X	X	X	X	+12-dB pre-amplifier gain, 0.312-V maximum peak input voltage
0	0	1	1	X	X	X	X	+18-dB pre-amplifier gain, 0.156-V maximum peak input voltage
0	1	0	0	X	X	X	X	+24-dB pre-amplifier gain, 0.078-V maximum peak input voltage
0	1	0	1	X	X	X	X	Reserved; undefined
0	1	1	0	X	X	X	X	Reserved; undefined
0	1	1	1	X	X	X	X	Reserved; undefined
0	X	X	X	1	X	X	X	MUTE ON, AINA and AINB inputs disabled
0	X	X	X	0	X	X	X	MUTE OFF, AINA or AINB enabled
0	X	X	X	X	1	X	X	Digital Loopback 2 enabled; D/A output looped to A/D input; EAR, LS, and AIN pin disabled
0	X	X	X	X	0	X	X	Digital Loopback 2 disabled
0	X	X	X	X	X	1	X	EAR and LS simultaneously enabled
0	X	X	X	X	X	0	X	EAR or LS enabled by MMR2 Bit 1
0	X	X	X	X	X	X	1	Secondary Tone Ringer enabled
0	X	X	X	X	X	X	0	Secondary Tone Ringer disabled

Secondary Tone Ringer Amplitude Register—(STRA)—Read/Write
Address = Indirect 6DH

Bit 7	6	5	4	3	2	1	0	Peak-to-Peak Output Voltage	Relative Output	Approximate Power into 50 Ohms
0	0	0	0	0	0	0	0	Silent		
0	0	0	1	0	0	0	0	Reserved		
0	0	1	0	0	0	0	0	Reserved		
0	0	1	1	0	0	0	0	Reserved		
0	1	0	0	0	0	0	0	Reserved		
0	1	0	1	0	0	0	0	Reserved		
0	1	1	0	0	0	0	0	0.22 V	–27 dB	0.25 mW
0	1	1	1	0	0	0	0	0.31 V	–24 dB	0.5 mW
1	0	0	0	0	0	0	0	0.44 V	–21 dB	1.0 mW
1	0	0	1	0	0	0	0	0.62 V	–18 dB	2.0 mW
1	0	1	0	0	0	0	0	0.88 V	–15 dB	4 .0 mW
1	0	1	1	0	0	0	0	1.25 V	–12 dB	8 .0 mW
1	1	0	0	0	0	0	0	1.77 V	–9 dB	16.0 mW
1	1	0	1	0	0	0	0	2.50 V	–6 dB	31.25 mW
1	1	1	0	0	0	0	0	3.53 V	–3 dB	62.5 mW
1	1	1	1	0	0	0	0	5.00 V	0 dB	125.0 mW
X	X	X	X	0	0	0	0	Bits 0–3 Reserved; must be written to 0		

Secondary Tone Ringer Frequency Register (STRF), Read/Write; Address = Indirect 6EH

STRF is a Read/Write register controlling the frequency of the secondary tone ringer. Hex codes 7F and 00 are reserved and should not be used. The coefficients are defined in the following table:

Table 7. Frequencies for Secondary Tone Ringer

Counter Value	Frequency (Hz)	Counter Value	Frequency (Hz)	Counter Value	Frequency (Hz)	Counter Value	Frequency (Hz)
3F	Reserved	3B	727.3	D8	369.2	F7	247.4
1F	Reserved	9D	716.4	6C	366.4	FB	246.2
0F	12000.0	4E	705.9	36	363.6	FD	244.9
87	9600.0	27	695.7	1B	360.9	7E	243.7
43	8000.0	13	685.7	8D	358.2	BF	242.4
A1	6857.1	09	676.1	C6	355.6	5F	241.2
D0	6000.0	04	666.7	E3	352.9	2F	240.0
E8	5333.3	82	657.5	F1	350.4	97	238.8
F4	4800.0	41	648.7	78	347.8	CB	237.6
7A	4363.6	A0	640.0	3C	345.3	65	236.5
3D	4000.0	50	631.6	9E	342.9	32	235.3
1E	3692.3	A8	623.4	CF	340.4	99	234.2
8F	3428.6	D4	615.4	E7	338.0	CC	233.0
C7	3200.0	6A	607.6	73	335.7	66	231.9
63	3000.0	B5	600.0	39	333.3	B3	230.8
B1	2823.5	DA	592.6	9C	331.0	59	229.7
58	2666.7	6D	585.4	CE	328.8	AC	228.6
2C	2526.3	B6	578.3	67	326.5	56	227.5
16	2400.0	5B	571.4	33	324.3	2B	226.4
0B	2285.7	AD	564.7	19	322.2	15	225.4
05	2181.8	D6	558.1	8C	320.0	8A	224.3
02	2087.0	6B	551.7	46	317.9	C5	223.3
01	2000.0	35	545.5	A3	315.8	62	222.2
80	1920.0	9A	539.3	D1	313.7	31	221.2
40	1846.2	4D	533.3	68	311.7	18	220.2
20	1777.8	A6	527.5	B4	309.7	0C	219.2
10	1714.3	D3	521.7	5A	307.7	06	218.2
88	1655.2	69	516.1	2D	305.7	83	217.2
C4	1600.0	34	510.6	96	303.8	C1	216.2
E2	1548.4	1A	505.3	4B	301.9	E0	215.3
71	1500.0	0D	500.0	25	300.0	70	214.3
38	1454.6	86	494.9	12	298.1	B8	213.3
1C	1411.8	C3	489.8	89	296.3	5C	212.4
8E	1371.4	E1	484.9	44	294.5	AE	211.5
47	1333.3	F0	480.0	A2	292.7	57	210.5
23	1297.3	F8	475.3	51	290.9	AB	209.6
91	1263.2	7C	470.6	28	289.2	55	208.7
48	1230.8	BE	466.0	94	287.4	AA	207.8
A4	1200.0	DF	461.5	4A	285.7	D5	206.9
D2	1170.7	6F	457.1	A5	284.0	EA	206.0
E9	1142.9	B7	452.8	52	282.4	F5	205.1
74	1116.3	DB	448.6	A9	280.7	FA	204.3
3A	1090.9	ED	444.4	54	279.1	7D	203.4
1D	1066.7	F6	440.4	2A	277.5	3E	202.5
0E	1043.5	7B	436.4	95	275.9	9F	201.7
07	1021.3	BD	432.4	CA	274.3	4F	200.8
03	1000.0	5E	428.6	E5	272.7	A7	200.0
81	979.6	AF	424.8	72	271.2	53	199.2
C0	960.0	D7	421.1	B9	269.7	29	198.4
60	941.2	EB	417.4	DC	268.2	14	197.5
30	923.1	75	413.8	EE	266.7	0A	196.7
98	905.7	BA	410.3	77	265.2	85	195.9
4C	888.9	5D	406.8	BB	263.7	42	195.1
26	872.7	2E	403.4	DD	262.3	21	194.3
93	857.1	17	400.0	6E	260.9	90	193.6
49	842.1	8B	396.7	37	259.5	C8	192.8
24	827.6	45	393.4	9B	258.1	E4	192.0
92	813.6	22	390.2	CD	256.7	F2	191.2
C9	800.0	11	387.1	E6	255.3	F9	190.5
64	786.9	08	384.0	F3	254.0	FC	189.7
B2	774.2	84	381.0	79	252.6	FE	189.0
D9	761.9	C2	378.0	BC	251.3	FF	188.2
EC	750.0	61	375.0	DE	250.0		
76	738.5	B0	372.1	EF	248.7		

Data Link Controller (DLC)

Overview

A 16 kb/s D Channel is time multiplexed within the frame structure of the S Interface. The data carried by the D Channel is encoded using the Link Access Protocol D-channel (LAPD) format shown in Figure 5. The D Channel can be used to carry either end-to-end signaling or Low speed packet data. Further information concerning LAPD protocol can be found in the CCITT recommendations. The LIU controls the multiplexing and demultiplexing of the D-channel data between the S Interface and the DLC.

The DLC performs processing of Level 1 and partial Level-2 LAPD protocol, including flag detection and generation, zero deletion and insertion, Frame Check Sequence (FCS) processing for error detection, and some addressing capability. High level protocol processing is done by the external microprocessor. The microprocessor may process the address field in the LAPD frame depending on the programmed state of the DLC. The status of the DLC is held in the status registers and relevant interrupts are generated under user program control. In addition to transmit and receive data FIFOs, the DLC contains a 16-bit pseudo-random number generator (RNG) used in the CCITT D-channel address allocation procedure.

D-Channel Processing

Random Number Generator (RNG)

The RNG is accessible by the microprocessor and operates in the following manner:

On the Low-to-High transition of the reset signal, the RNG is cleared, then started. The RNG stops when the LSB or MSB of the 16-bit counter is read by the microprocessor, or when the MSB is loaded by the microprocessor. Writing to the MSB of the counter loads this byte but does not start the RNG. The RNG starts when the LSB of the counter is loaded by the microprocessor.

Frame Abort

The DLC aborts an incoming D-channel frame when seven contiguous logical 1s are received. When this occurs, an "End of Receive Packet" interrupt is issued to the processor. DER Bit 0 is set to a logical 1 when the last byte of the aborted packet is read from the D-Channel Receive Buffer. The "Receive Abort" interrupt can be masked by setting DMR2 Bit 0 to a logical 0. With the exception of the "Packet Reception in Progress" bit, no other bits associated with packet reception are updated after a receive packet abort. The receive frame can be aborted at any time by setting INIT Bit 6 to logical 1. Similarly, the transmit frame can be aborted by setting INIT Bit 7 to a logical 1. When the transmit frame is aborted, seven consecutive 1s are transmitted on the S Interface followed by a logical 0, and DSR1 Bit 7 is set to a logical 1. Seven consecutive 1s followed by a 0 will continue to be transmitted as long as INIT Bit 7 is set to 1. DSR1 Bit 7 will be set after each sequence of seven consecutive 1s followed by 0.

Level-2 Frame Structure

The D-channel Level-2 frame structure conforms to one of the formats shown in Figure 5. All frames start and end with the flag sequence consisting of one 0 followed by six 1s followed by one 0. A packet consists of a Level-2 frame minus the flag bytes. The LSB is transmitted first for all bytes except the FCS.

The flag preceding a packet is defined as the opening flag. Therefore, the byte following an opening flag, by definition, cannot be an abort or another flag. A closing flag is defined as a flag that terminates a packet. This flag can be followed by another flag(s), interframe fill consisting of all 1s or flags, or the address field of the next packet. In the latter case, the closing flag of one packet is the opening flag of the next packet. The DLC receiver can recognize interframe fill consisting of logical 1s or flags. The DLC transmitter follows the closing flag with interframe fill consisting of all 1's (mark Idle) if DMR4 Bit 4 is set to a logical 0, or all 0's (flag Idle) if DMR4 Bit 4 is set to a logical 1. CCITT I-series D-channel access protocol specifies use of mark Idle.

When a collision is detected (mismatch of a D and E Bit), a complete frame must be retransmitted. For transfer across the S Interface, the S-interface frame structure is impressed upon the D-channel frame structure (LAPD).

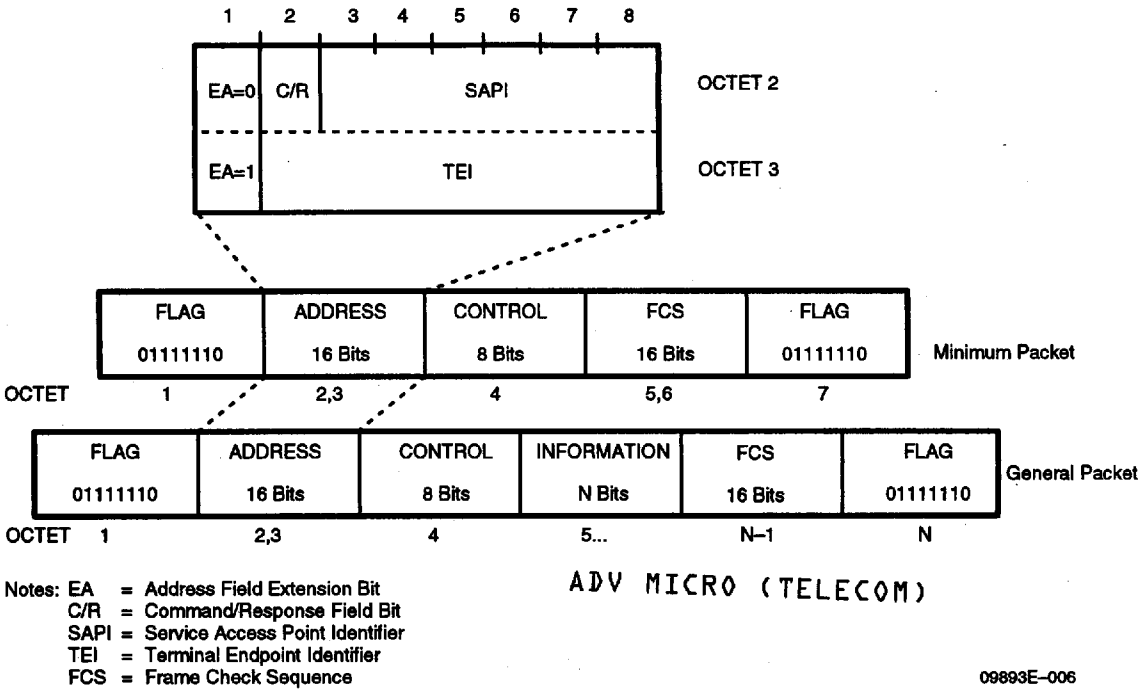
Zero Insertion/Deletion

When transmitting, the DLC examines the frame content between the opening and closing flags. To ensure that a flag sequence is not repeated within the flag boundaries of the frame, a logical 0 bit is automatically inserted after each sequence of five contiguous logical 1s. When receiving, the DLC examines the frame content between the opening and closing flags and automatically discards the first logical 0 which directly follows five contiguous logical 1s.

D-Channel Address Recognition

The address field, shown in Figure 5, allows for three types of addresses:

1. 1-byte address signified by the LSB of the first address byte being set to a logical 1
2. 2-byte address signified by the LSB of the first address byte being set to a logical 0, and the LSB of the second address byte being set to a logical 1
3. More than 2-byte address signified by the LSB of both the first and second address bytes being set to a logical 0



Notes: EA = Address Field Extension Bit
C/R = Command/Response Field Bit
SAPI = Service Access Point Identifier
TEI = Terminal Endpoint Identifier
FCS = Frame Check Sequence

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Figure 5. Level-2 Frame Structure Formats

In the case of the LAPD operating environments, the address is a 2-byte address where the first byte is analogous to the Service Access Point Identifier (SAPI) and the second byte is analogous to the Terminal Endpoint Identifier (TEI) as defined by the CCITT recommendations.

The DLC is able to recognize D-channel addresses of all of the three types outlined above. Note that only the first two bytes of a more than 2-byte address can be checked by the DLC. There are four First Received Byte Address Registers (FRARs) which hold the values used to match against the first byte of the incoming address. Similarly, there are four Second Received Byte Address Registers (SRARs) which hold the values used to match against the second byte of the incoming address.

FRAR4 defaults to FE hex; SRAR4 defaults to FF hex. This default is analogous to the broadcast address defined by the CCITT recommendations. The type of address recognition which is enabled is determined as follows:

DMR4 Bit 7	DMR4 Bit 5	DMR1 Bits 7	6	5	4		Type of address recognition
0	1	X	X	X	1	FRAR1	First received byte-only address
		X	X	1	X	FRAR2	
		X	1	X	X	FRAR3	
		1	X	X	X	FRAR4	
1	1	X	X	X	1	SRAR1	Second received byte-only address
		X	X	1	X	SRAR2	
		X	1	X	X	SRAR3	
		1	X	X	X	SRAR4	
X	0	X	X	X	1	FRAR1 : SRAR1	2-byte address
		X	X	1	X	FRAR2 : SRAR2	
		X	1	X	X	FRAR3 : SRAR3	
		1	X	X	X	FRAR4 : SRAR4	
X	X	0	0	0	0		Address recognition disabled

If DMR4 Bit 6 is set to a logical 0, Bit 1 of the FRARs is ignored when matching the first incoming address byte. If DMR4 Bit 6 is set to a logical 1, all bits of the FRARs are used when matching the first incoming address byte. FRAR Bit 1 is analogous to the C/R Bit defined by the CCITT recommendations. The address recognition mechanism for the four FRAR/SRAR addresses can be individually enabled/disabled via DMR1 bits 4–7.

First Received Byte-Only Address Recognition

If DMR4 Bit 5 is set to a logical 1 and DMR4 Bit 7 is set to a logical 0, only the first byte of the incoming address is compared with the values stored in the enabled FRARs. An interrupt is generated if there is an address match and the "Valid Address" interrupt is enabled. If the address matches, the packet will be received.

Second Received Byte-Only Address Recognition

If DMR4 Bits 5 and 7 are set to a logical 1, the DLC compares only the value in the second byte of the incoming address with values stored in the enabled SRARs. An interrupt is generated if there is an address match and the "Valid Address" interrupt is enabled. If the address matches, the packet will be received.

2-Byte Address Recognition

If DMR4 Bit 5 is set to a logical 0, the first byte of the incoming address is compared with the values stored in the enabled FRARs, and the second byte of the incoming address is compared with the value stored in the corresponding SRAR. An interrupt is generated if a match is found for both incoming address bytes with a FRAR/SRAR pair and the "Valid Address" interrupt is enabled. If the address matches, the packet will be received.

Disabling Address Recognition

If DMR1 Bits 4, 5, 6, and 7 are all set to logical 0, all address recognition is disabled and all addresses are recognized and received. In this case, the Am79C30A/32A receives the first two bytes following the opening flag (the incoming address), and then issues an "End of Address" interrupt if the "End of Address" interrupt is enabled.

DLC Operation

DLC Transmit and Receive FIFOs

The DLC Transmit and Receive FIFOs may be configured to the Normal or Extended mode of operation. Normal mode is fully backwards compatible with the Revision D or prior DSC circuit, and is activated upon RESET or if EFCR Bit 0 is programmed to logical 0. In Normal mode the Transmit and Receive FIFOs are each eight bytes in length.

The Extended mode of FIFO operation may be activated by programming EFCR Bit 0 to a logical 1, increasing the depth of the Transmit and Receive FIFOs to 16 bytes and 32 bytes, respectively. The setting of EFCR Bit 0 to logical 1 also alters the available programmable FIFO threshold values set by DMR4 Bits 2 and 3.

Receiving D-Channel Packets

The receiver controls the flow of D-channel data to the D-Channel Receive Buffer and the termination of a receive packet. Up to two packets can be contained in the D-Channel Receive Buffer.

After receiving an opening flag (a bit sequence of 01111110) and one byte of data which is not an abort or flag on the D Channel, the DLC sets the "Packet Reception in Progress" status bit (Bit 2) in D-Channel Status Register 1 (DSR1). The DLC then receives the first two bytes (the two address bytes). If address recognition is enabled, the Am79C30A/32A issues a "Valid Address" interrupt if a match between the programmed values and the received address is detected. If no match is detected and address recognition is enabled, the DLC ignores the packet. If address recognition is disabled, the Am79C30A/32A receives the first two bytes, issues an "End of Address" interrupt, and receives the packet. Both a "Valid Address" and an "End of Address" interrupt set Interrupt Register Bit 2 to a logical 1 and Bit 0 of the D-Channel Status Register 1 (DSR1) to a logical 1. The "Valid Address/End of Address" interrupt can be disabled via DMR3 Bit 0. There is an internal 3-byte delay which holds the first of the D-channel address bytes until the interrupt has been issued. Note that the incoming address bytes cannot be read however, until the "D-Channel Receive Byte Available" or "D-Channel Receive Threshold" interrupt is set.

After the address is received, the DLC continues to receive D-channel bytes into the D-Channel Receive Buffer FIFO. The DLC issues an interrupt when data is available in the D-Channel Receive Buffer. This interrupt can be disabled by setting DMR3 Bit 3 to a logical 0. The DLC also issues an interrupt when the receive threshold set in DMR4 is reached. This interrupt can be disabled by programming a logical 0 into DMR1 Bit 1. By polling, the microprocessor can then read the D-channel bytes. The 3-byte delay incurred during address recognition is maintained. Therefore, the DLC receives the Frame Check Sequence (FCS) before issuing an interrupt to signal the last byte of the packet has been received and appropriate status bits have been updated. If DMR3 Bit 7 is set, the two FCS bytes at the end of the packet are transferred into the D-Channel Receive Buffer along with the data.

The DLC issues an interrupt when the last byte of the packet is read from the DCRB. This interrupt can be disabled by setting DMR3 Bit 2 to a logical 0.

After the FCS is received, the DLC receiver detects the closing flag (a bit sequence of 01111110) and then terminates the packet by issuing an "End Of Receive Packet" interrupt (Bit 1 of DSR1) and returns to looking for opening flags. The DLC also terminates the packet when an abort, an overflow, or overrun error condition is detected. The "End Of Receive Packet" interrupt can be disabled by setting DMR1 Bit 3 to a logical 0.

The D-Channel Receive Byte Count Register (DRCR) is a 16-bit wide, two-word deep FIFO which is used to record the number of bytes in the incoming D-channel packets. Each count is terminated by an end-of-packet condition. Thus, the DRCR informs the microprocessor of the number of bytes, including the address bytes, which have been received. The counter is updated when the last byte of a packet is placed in the D-Channel Receive Buffer. When the FCS bytes are included in the data transferred to the D-Channel Receive Buffer, the FCS bytes are included in the byte count; if the FCS bytes are not included in the transfer, they are not included in the byte count. The opening flag and closing flag are not included in the byte count.

The D-Channel Error and Address Status Registers are also double buffered. Reading the last byte of a packet causes the DER byte to propagate to the output of the FIFO and updates the D-Channel Status and Interrupt Registers accordingly. Reading the MSB of the DRCR causes the next count and associated ASR byte to propagate to the output of the FIFOs and updates the D-Channel Status and Interrupt Registers accordingly. For this reason it is important to read ASR, DER, and DSR1 prior to reading the DRCR.

When a receive error occurs, an "End-of-Packet" interrupt is generated and the packet is terminated. When the last byte of the associated packet is read from the D-Channel Receive Buffer, the appropriate DER bits are set and an error interrupt is generated. All error interrupts can be individually masked by setting the corresponding bits in DMR2 to a logical 0.

There is one 16-bit D-Channel Receive Byte Limit Register (DRLR). The received byte count is compared with the DRLR. When the byte count of the currently received D-channel packet exceeds the limit value, a receiver overflow is detected, the packet is terminated, and an "End-of-Packet" interrupt is issued. D-Channel Error Register (DER) Bit 4 is set to a logical 1 and an overflow interrupt issued when the last byte of the associated packet is read from the D-Channel Receive Buffer. The "Overflow Error" interrupt can be masked by setting DMR2 Bit 4 to a logical 0.

The minimum packet length is five bytes for a 2-byte address packet (not including flags). If the packet length is less than the above, an interrupt is issued and DER Bit 5 is set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer. The error interrupt can be masked by setting DMR2 Bit 5 to a logical 0.

If packet reception is in progress and the D-Channel Receive Buffer is full, the microprocessor has a maximum of 425 µs to respond to the D-Channel "Receive Data Available" interrupt. If the microprocessor fails to do so, then an overrun error occurs when the data byte is overwritten. When this happens, the packet is terminated. DER Bit 6 is set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer. The "Overrun Error" interrupt can be masked by setting DMR2 Bit 6 to logical 0.

Error indication is given if two packets have been received and not serviced by the user and a third packet is received via DSR2 Bit 2. When this error occurs, the third packet is terminated (not received).

Error indication is given for a receiver abort (the reception of seven contiguous 1s) by DER Bit 0.

If the number of bits received between two flags is not an integer multiple of eight (if the received packet does not contain an integral number of bytes), DER Bit 1 is set and an interrupt is generated when the last byte of the associated packet is read from the D-Channel Receive Buffer.

The incoming bit stream (including FCS) is run through the FCS generation and compare block. Upon receipt of the closing flag, the result is checked and must be (MSB first) 0001110100001111. Any other pattern indicates an FCS error, and DER Bit 3 is set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

The DLC receiver does not assume the packet to be byte-aligned. The architecture supports shared flags between packets, interframe fill consisting of logical 1s (Mark idle), and interframe fill consisting of flags (Flag idle). Mark idle is defined as at least 15 or more contiguous 1s. Flag idle is defined as more than two consecutive flag characters, not including a closing flag. DSR2 Bit 5 is set to a logical 1 while Mark idle is being detected. DSR2 Bit 6 is set to a logical 1 while Flag idle is being detected. The receiver D-channel packet can be aborted at any time during reception by setting INIT Bit 6.

Transmitting D-Channel Packets

The DLC Transmitter is activated as soon as the MSB (the second byte) of the 16-bit D-Channel Transmit Byte Count Register (DTCR) has been loaded by the microprocessor.

Next, the LIU starts counting the number of consecutive 1s on the E Channel until the number of 1s defined by the LIU priority mechanism is detected. After the sequence of 1s, the DLC transmitter will begin packet transmission.

Address bytes for a transmit packet can be handled in two ways: they can be loaded into the transmit buffer or loaded into the Transmit Address Register (TAR).

There is one 16-bit TAR which can be loaded by the microprocessor. The bytes loaded into the TAR are transmitted LSB first followed by MSB. For LAPD operation, the LSB contains the SAPI, and the MSB contains TEI. This 16-bit address (loaded LSB first) is transmitted within the address field of the D-channel packet if enabled by setting DMR1 Bit 2 to a logical 1. If the TAR is enabled, the DTCR should be loaded with the number of bytes to be transmitted excluding the address, flags, and FCS. If the TAR is disabled, the DTCR should be loaded with the number of bytes to be transmitted excluding the flags and FCS, and the microprocessor must load the address to be transmitted as the first two bytes of the D-channel packet data.

The DLC issues an interrupt when a position is available in the D-Channel Transmit Buffer. This interrupt can be disabled by setting DMR3 Bit 5 to a logical 0. The DLC also issues an interrupt to the microprocessor to request D-channel data bytes when the D-Channel Transmit Buffer empties to the threshold specified in the D-Channel FIFO Mode Register. This interrupt can be disabled by setting DMR1 Bit 0 to a logical 0.

If the D-Channel Transmit Buffer is empty, the microprocessor has up to 375 µs to respond to the D-channel transmit buffer interrupt. If the microprocessor fails to load the data bytes in this time frame, an underrun interrupt is generated in DER Bit 7, and packet transmission is terminated with a transmitted abort. The "Underrun" interrupt can be masked by setting DMR2 Bit 7 to a logical 0. Transmission is also terminated when a collision is detected or LIU loss of synchronization occurs.

The D-Channel Transmit Byte Count Register is decremented each time a byte of data is transferred from the D-Channel Transmit Buffer to the DLC. The count represents the number of bytes left to be transferred, excluding the FCS and flags. If the transmit abort bit (INIT Bit 7) is set, the transmit byte count is frozen and indicates the number of bytes left to transfer, not the number of bytes transmitted. The last byte of the packet is determined by the D-Channel Transmit Byte Count decrementing to zero. When this occurs, DSR2 Bit 3 is set to a logical 1.

After the last byte of the packet is transmitted, the DLC adds the FCS and closing flag. Then the DLC issues an interrupt (Bit 6 of DSR1) to signify the end of the packet transmission. This interrupt can be masked by setting DMR3 Bit 1 to a logical 0, and is reset either by reading DSR1 or when the D-Channel Transmit Byte Count Register is loaded for the next packet.

Once the D-Channel Transmit Byte Count has decremented to 0, a second packet may be loaded into the D-Channel Transmit FIFO. If the MSB of the D-Channel Transmit Byte Count Register is loaded prior to the "end-of-transmit packet" interrupt, the second packet is transmitted back-to-back with the previous packet. The "End-of-Transmit Packet" interrupt is not set between the two packets. If the MSB of the D-Channel Transmit Byte Count Register is loaded after the "end-of-packet" interrupt, the second packet is transmitted once the LIU priority mechanism has been re-satisfied.

Collision Detection

The Network Terminator echoes the transmitted D-channel data back to the DLC in the E-channel bits of the S-interface frame. If there is a difference between the data transmitted and the data echoed back, a collision has occurred. The DLC alerts the microprocessor to this event by asserting the interrupt line ($\overline{INT}$) and setting DER Bit 2. If a collision occurs during the transmission of an abort sequence, the interrupt is still issued. The collision detect interrupt can be masked by setting DMR2 Bit 2 to a logical 0.

D-Channel Receive and Transmit Errors

Non-Integer Number of Bytes

A non-integer number of bytes occurs when the number of D-channel bits received between opening and closing flags is not divisible by eight. If a received packet consists of a non-integer number of bytes, the DLC sets Bit 1 in the D-Channel Error Register (DER) to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Frame Check Sequence Error

If a received packet, including its 16-bit Frame Check Sequence, is not received perfectly, the DLC sets DER Bit 3 to a logical 1 when the last byte of the associated packet is read from the Receive Buffer.

Receive Packet Abort

If seven contiguous 1s are received while receiving a packet, the packet will be terminated. DER Bit 0 will be set to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Overflow

Overflow occurs when the total number of D-channel bytes within a packet (including, only when enabled, the Frame Check Sequence bytes) exceeds the limit contained in the D-Channel Receive Byte Limit Register. (See Receiving D-Channel Packets section.) When this occurs, the DLC terminates the packet, and sets DER Bit 4 to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Underflow

If a received D-channel (including FCS) packet is less than five bytes for a 2-byte address packet, an underflow error condition occurs, and the DLC sets DER Bit 5 to a logical 1 when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Overrun

A D-channel overrun error occurs when the receiver buffer is full, and another byte is received. This can happen if the D-Channel Receive Buffer fills, and is not read within 425 µs. When this error occurs, the DLC sets DER Bit 6 to a logical 1 and terminates the packet.

Underrun

A D-channel underrun error occurs when an empty D-channel buffer is transmitted. This can happen if the D-Channel Transmit Buffer is not loaded within 375 µs of the D-Channel "Transmit Buffer Empty" interrupt being asserted (IR Bit 0). When this error occurs, the DLC sets DER Bit 7 to a logical 1 and terminates the packet.

Receive Packet Lost

"Receive Packet Lost" occurs when two outstanding packets have been received and not serviced (the microprocessor has not read the DRCB register), and a third packet is received. When this error occurs, DSR2 Bit 2 is set to a logical 1 and the incoming packet is terminated (not received).

DLC Registers

The DLC contains the following registers:

Registers	No./Registers	Mnemonic
First Received Byte Address Registers	4	FRAR
Second Received Byte Address Registers	4	SRAR
Transmit Address Register (16-bit)	1	TAR
D-Channel Receive Byte Limit Register (16-bit)	1	DRLR
D-Channel Receive Byte Count Register (16-bit) (2-word FIFO)	1	DRCR
D-Channel Transmit Byte Count Register (16-bit)	1	DTCR
Random Number Generator Registers	2	RNGR
D-Channel Mode Registers	4	DMR
Address Status Register (2-byte FIFO)	1	ASR
Extended FIFO Control Register	1	EFCR
D-Channel Transmit Buffer Register	–	DCTB
D-Channel Receive Buffer Register	–	DCRB

There are three other read-only accessible registers associated with the DLC:

D-Channel Status Registers (DSR1 and DSR2)
D-Channel Error Register (DER) (2-byte FIFO)

Transmit Address Register—(TAR)—Read/Write
Address = Indirect 83H

This register contains the address of the packet to be transmitted if the TAR bit is enabled (DMR1 Bit 2).

First Received Byte Address Register—(FRAR1–FRAR4)—Read/Write
Address = Indirect FRAR1–FRAR3 = 81H, FRAR4 = 8CH

These registers contain the value to match against the first byte of the incoming address. If DMR1 Bits 4–7 are disabled, these registers will be ignored.

Second Received Byte Address Register—(SRAR1–SRAR4)—Read/Write
Address = Indirect SRAR1–SRAR3 = 82H, SRAR4 = 8DH

These registers contain the value to match against the first byte of the incoming address. If DMR1 Bits 4–7 are disabled, these registers will be ignored.

D-Channel Receive Byte Count Register—(DRCR)—Read
Address = Indirect 89H

This register determines the maximum number of bytes in a received packet.

D-Channel Receive Byte Limit Register—(DRLR)—Read/Write
Address = Indirect 84H

This register contains the total number of received bytes.

D-Channel Transmit Byte Count Register—(DTCR)—Read/Write
Address = Indirect 85H

This register contains the total number of transferred bytes.

Random Number Generator Register—(RNGR1, RNGR2)—Read/Write
Address = Indirect RNGR1 = 8AH, RNGR2 = 8BH

These registers control the operation of the Random Number Generator. When read, they display the random number generated by the chip.

D-Channel Transmit Buffer Register—(DCTB)—Write

D-Channel transmit FIFO.

D-Channel Receive Buffer Register—(DCRB)—Read

D-Channel receive FIFO.

D-Channel Mode Register 1—(DMR1)—Read/Write
Address = Indirect 86H

DMR1 controls the enable/disable options for the DLC. It is under sole control of the microprocessor, and does not generate any interrupts. DMR1 is defined below.

Bit	Logical 1	Logical 0
0	Enable "D-channel Transmit Threshold" interrupt (see IR Bit 0)	Disable interrupt (default value)
1	Enable "D-channel Receive Threshold" interrupt (see IR Bit 1)	Disable interrupt (default value)
2	Enable Transmit Address Register	Disable Transmit Address Register (default value)
3	Enable "End of Receive Packet" interrupt (see DSR1 Bit 1)	Disable interrupt (default value)
4	Enable FRAR1/SRAR1	Disable FRAR1/SRAR1 (default value)
5	Enable FRAR2/SRAR2	Disable FRAR2/SRAR2 (default value)
6	Enable FRAR3/SRAR3	Disable FRAR3/SRAR3 (default value)
7	Enable FRAR4/SRAR4	Disable FRAR4/SRAR4

D-Channel Mode Register 2—(DMR2)—Read/Write
Address = Indirect 87H

DMR2 is used to enable/disable the interrupts generated in the DER (see DER definition on page 41). DMR2 is controlled by the microprocessor, and does not generate interrupts. DMR2 is defined below.

Bit	Logical 1	Logical 0 (default value)
0	Enable "Receive Abort" interrupt (see DER Bit 0)	Disable interrupt
1	Enable "Non-integer Number of Bytes Received" interrupt (see DER Bit 1)	Disable interrupt
2	Enable "Collision Abort Detected" interrupt (see DER Bit 2)	Disable interrupt
3	Enable "FCS Error" interrupt (see DER Bit 3)	Disable interrupt
4	Enable "Overflow Error" interrupt (see DER Bit 4)	Disable interrupt
5	Enable "Underflow Error" interrupt (see DER Bit 5)	Disable interrupt
6	Enable "Overrun Error" interrupt (see DER Bit 6)	Disable interrupt
7	Enable "Underrun Error" interrupt (see DER Bit 7)	Disable interrupt

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D-Channel Mode Register 3 — (DMR3) — Read/Write
Address = Indirect 8EH

Bit	Logical 1	Logical 0
0	Enable "Valid Address/End of Address" interrupt (default value)(see DSR1 Bit 0)	Disable interrupt
1	Enable "End of Valid Transmit Packet" interrupt (default value)(see DSR1 Bit 6)	Disable interrupt
2	Enable "Last Byte of Received Packet" interrupt (see DSR2 Bit 0)	Disable interrupt (default value)
3	Enable "Receive Byte Available" interrupt (see DSR2 Bit 1)	Disable interrupt (default value)
4	Enable "Last Byte Transmitted" interrupt (see DSR2 Bit 3)	Disable interrupt (default value)
5	Enable "Transmit Buffer Available" interrupt (see DSR2 Bit 4)	Disable interrupt (default value)
6	Enable "Received Packet Lost" interrupt (see DSR2 Bit 2)	Disable interrupt (default value)
7	Enable FCS transfer to FIFO	Disable FCS transfer to FIFO (default value)

D-Channel Mode Register 4 — (DMR4) — Read/Write
Address = Indirect 8FH

Bit 7 6 5 4 3 2 1 0	Control	Function
X X X X X X 0 0	Receiver Threshold	1 byte (EFCR Bit 0 = 0) 1 byte (EFCR Bit 0 = 1)
X X X X X X 0 1		2 bytes (EFCR Bit 0 = 0) 16 bytes (EFCR Bit 0 = 1)
X X X X X X 1 0		4 bytes (EFCR Bit 0 = 0) 24 bytes (EFCR Bit 0 = 1)
X X X X X X 1 1		8 bytes (EFCR Bit 0 = 0) 30 bytes (EFCR Bit 0 = 1)
X X X X 0 0 X X	Transmitter Threshold	1 byte (EFCR Bit 0 = 0) 1 byte (EFCR Bit 0 = 1)
X X X X 0 1 X X		2 bytes (EFCR Bit 0 = 0) 6 bytes (EFCR Bit 0 = 1)
X X X X 1 0 X X		4 bytes (EFCR Bit 0 = 0) 10 bytes (EFCR Bit 0 = 1)
X X X X 1 1 X X		8 bytes (EFCR Bit 0 = 0) 14 bytes (EFCR Bit 1 = 1)
X X X 0 X X X X X X X 1 X X X X	Interframe Fill	Mark Idle (default value) Flag Idle
X X 0 X X X X X 0 X 1 X X X X X 1 X 1 X X X X X	Address Recognition	2-byte (default value) First Received Byte only Second Received Byte only
X 0 X X X X X X X 1 X X X X X X	C/R Bit Compare	Disable FRAR Bit 1 compare (default value) Enable FRAR Bit 1 compare

Note: The receiver and transmitter thresholds can only be changed when the Am79C30A/32A is in Idle Mode.

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Address Status Register—(ASR)—Read Only
Address = Indirect 91H

Bit	Logical 1	Logical 0 (default value)
0	FRAR1/SRAR1 address recognized	No FRAR1/SRAR1 address match
1	FRAR2/SRAR2 address recognized	No FRAR2/SRAR2 address match
2	FRAR3/SRAR3 address recognized	No FRAR3/SRAR3 address match
3	FRAR4/SRAR4 address recognized	No FRAR4/SRAR4 address match
4–7	Reserved	Reserved

D-Channel Status Register 1—(DSR1)—Read Only
DSR1 has the following format:

Bit	Logical 1	Logical 0 (default value)
0	Valid Address (VA) if the address decode logic is enabled or End-of-Address (EOA) if the address decode logic is disabled	No valid address
1	End of receive packet	Not end of packet
2	Packet reception in progress	Packet not being received
3	Loopback in operation at Am79C30A/32A	No loopback in operation at Am79C30A/32A
4	Loopback in operation at LIU	No loopback in operation at LIU
5	D-channel back-off not in operation	D-channel back-off in operation
6	End of valid transmit packet	No end-of-transmit packet or no transmission
7	Current transmit packet has been aborted	No transmit packet abort

The DSR1 bits generate interrupts, and are set/reset under the following conditions (in addition to a hardware reset or Idle Mode):

Bit	Generate Interrupt	Bit Set	Bit Reset
0	Yes, if DMR3 Bit 0 = 1	Two bytes after an opening flag if a VA is decoded or address recognition is disabled	When the microprocessor reads DSR1 or associated DRCR
1	Yes, if DMR1 Bit 3 = 1	When a closing flag is received	When the microprocessor reads DSR1 or associated DRCR
2	No	One byte after the opening flag of any packet, valid or not	When a flag or an abort is received
3	No	When the operation is in progress	When the operation is not in progress
4	No	When the operation is in progress	When the operation is not in progress
5	No	When the operation is in progress	When the operation is not in progress
6	Yes, if DMR3 Bit 1 = 1	When the closing flag is transmitted	When the microprocessor reads DSR1 or when DTCR is loaded
7	No	When seven 1s and a 0 have been transmitted	When the microprocessor reads DSR1 or when DTCR is loaded

D-Channel Status Register 2—(DSR2)—Read Only

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DSR2 has the following format:

Bit	Logical 1	Logical 0 (default value)
0	Last byte of received packet	Not last byte of received packet
1	Receive byte available	Receive byte not available
2	Receive packet lost	Receive packet not lost
3	Last byte transmitted	Last byte not transmitted
4	Transmit buffer available	Transmit buffer not available*
5	Mark idle detected (15 or more contiguous 1s)	Mark idle not detected
6	Flag idle detected (more than two contiguous flags)	Flag idle not detected
7	Start of second received packet in FIFO	Second packet not yet in FIFO

*Following RESET, the Transmit Buffer Available (Bit 4) is set, producing a default value of 10H instead of 00H.

The DSR2 bits generate interrupts and are set/reset under the following conditions (in addition to a hardware reset or Idle Mode):

Bit	Generate Interrupt	Bit Set	Bit Reset
0	Yes, if DMR3 Bit 2=1	When last byte of a received packet is read from the DCRB	When the microprocessor reads the DSR2
1	Yes, if DMR3 Bit 3=1	When DCRB contains one or more bytes of data	When DCRB is empty
2	Yes, if DMR3 Bit 6=1	When two outstanding packets are received and not serviced, and a third packet is received	When the microprocessor reads DSR2
3	Yes, if DMR3 bit 4=1	When the last byte of a transmit packet is transferred from the DCTB	When the microprocessor reads DSR2
4	Yes, if DMR3 Bit 5=1	When the DCTB is available to be loaded with a data byte	When the DCTB is full
5	No	When 15 contiguous one bits have been detected in the incoming D Channel	When the first zero bit is detected on the incoming D Channel
6	No	When more than two contiguous flags are detected on the incoming D Channels not including a closing flag	When a non-flag character is detected on the incoming D Channel
7	Yes, if EFCR Bit 1=1	When start of second packet is in the receive FIFO	When second receive packet is not present

D-Channel Error Register—(DER)—Read Only

The DER has the following format:

Bit	Logical 1	Logical 0 (default value)
0	Received Packet Abort	No abort received
1	Non-integer number of bytes have been received	Integer number of bytes received
2	Collision Detected	No error
3	FCS Error	No error
4	Overflow Error	No error
5	Underflow Error	No error
6	Overrun Error	No error
7	Underrun Error	No error

The DER bits generate interrupts, and are set/reset under the following conditions (in addition to a hardware reset):

Bit	Generates Interrupt	Bit Set	Bit Reset
0	Yes, if DMR2 Bit 0=1	When seven consecutive 1s are received within a packet (DSR1 Bit 2=1)	When the microprocessor reads the DER or associated DRCR
1	Yes, if DMR2 Bit 1=1	Upon error condition after closing flag has been received	When the microprocessor reads the DER or associated DRCR
2	Yes, if DMR2 Bit 2=1	See section on collision detection	When the microprocessor reads the DER or when DTCR is loaded
3	Yes, if DMR2 Bit 3=1	If error occurs	When the microprocessor reads the DER or associated DRCR
4	Yes, if DMR2 Bit 4=1	If error occurs	When the microprocessor reads the DER or associated DRCR
5	Yes, if DMR2 Bit 5=1	If error occurs	When the microprocessor reads the DER or associated DRCR
6	Yes, if DMR2 Bit 6=1	If error occurs	When the microprocessor reads the DER or associated DRCR
7	Yes, if DMR2 Bit 7=1	If error occurs	When the microprocessor reads the DER or when DTCR is loaded

DER Bits 0, 1, 3, 4, 5, and 6 are set when the last byte of the associated packet is read from the D-Channel Receive Buffer.

Extended FIFO Control Register—(EFCR)—Read/Write

Address = Indirect 92H

Bit 7	6	5	4	3	2	1	0	Function
0	0	0	0	0	0	X	X	Bits 2–7 reserved, must be written to 0
0	0	0	0	0	0	0	X	"Start of Second Received Packet In FIFO" interrupt disabled
0	0	0	0	0	0	1	X	"Start of Second Received Packet In FIFO" interrupt enabled
0	0	0	0	0	0	X	0	Normal mode of FIFO operation
0	0	0	0	0	0	X	1	Extended mode of FIFO operation

Peripheral Port (PP)

Overview

The purpose of the Peripheral Port is to allow external peripherals to be connected to the DSC/IDC circuit. There are two basic modes of operation, Serial Bus Port Mode, and IOM 2 Terminal Mode. Within IOM 2 Terminal Mode, the DSC/IDC circuit may be configured as either an IOM 2 timing master or slave. The definition of the Peripheral Port pins depends on the operating mode of the port, as described in Table 8.

Serial Bus Port (SBP) Mode

The SBP Mode of operation is backwards compatible with the Revision D DSC circuit serial port, and is entered either following a device RESET or if programmed in PPCR1.

In SBP Mode, the SCLK output provides a 192-kHz 1X data clock of programmable polarity. The SBIN and SBOUT pins support three 8-bit serial data channels, designated Bd, Be, and Bf. The SFS output provides an 8-kHz serial frame sync pulse eight bit periods in width, coincident with the Bd channel. The SBP Mode timing is illustrated in Figure 6.

Following a RESET, the SCLK and SFS outputs will default to a high-impedance state, which will be maintained until any MUX connection is programmed (or until the Peripheral Port is programmed to an IOM 2 Mode). SCLK and SFS will remain in a high-impedance state if the Peripheral Port is explicitly disabled. The SCLK and SFS signals are synchronized to the received S-interface frame. If there is no S-interface frame synchronization, the SCLK and SFS signals will free-run at 192 kHz and 8 kHz respectively.

If the DSC/IDC circuit is programmed to Idle Mode, the SFS output is driven Low but SCLK continues to run. In Power-Down Mode, both the SFS and SCLK outputs are high-impedance.

IOM 2 Terminal Mode Overview

The IOM 2 Interface standard encompasses both a Linecard Mode and a Terminal Mode. The Terminal Mode was defined to provide four functions, as follows:

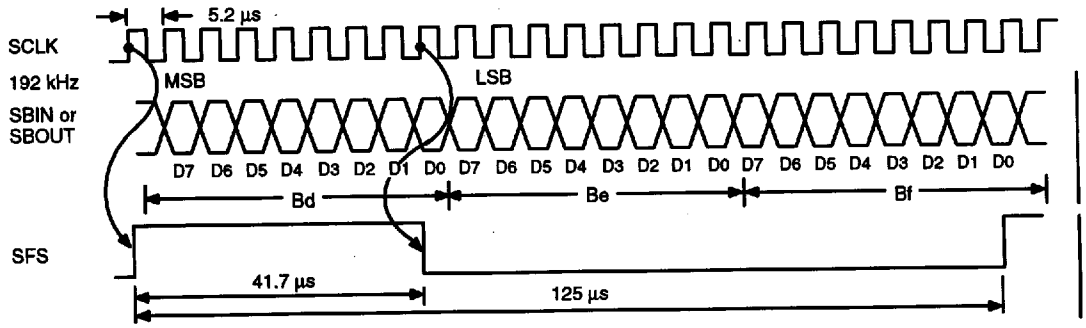
1. Connection of multiple Layer-2 devices to a Layer-1 device (in this case, the Layer-1 device is the S/T Interface LIU). Provision for the connection of non-IOM 2 devices is included.
2. Programming and control of Layer-1 or Layer-2 devices that do not have a microprocessor interface, for example, a U-interface transceiver.

Table 8. Pin Operation versus Peripheral Port Modes

Pin	SBP On	Port Disabled	IOM 2 M Activated	IOM 2 M Deactivated	IOM 2 S* Activated	IOM 2 S* Deactivated
SBIN	IN	Z	IN	IN	IN/OD	OD
SBOUT	OUT	Z	OD	Z	OD/IN	Z
SCLK	OUT	Z	OUT	Low	IN	IN
SFS	OUT	Z	OUT	Low	IN	IN
BCL/CH2STRB	OUT	Z	OUT	Low	Z	Z

IN = Input OUT = Output Z = High Impedance OD = Open Drain Output

*The Am79C30A is a non-Layer 1 component when operated in the slave mode; however, it has a microprocessor interface. As a result, it is required to change the direction of its I/O pins at certain times in order to communicate with both the upstream Layer-1 device and any downstream peripheral devices. In the IOM 2 Slave Mode, the direction of data flow is reversed with respect to the DSC circuit during Sub-frame 0 and during the deactivated state. The rule is that the upstream Layer-1 device only uses Sub-frame 0 and does not reverse its pins. Any non-Layer 1 component that does not contain a microprocessor interface (i.e., program by the DSC circuit over the Monitor Channel in Sub-frame 1) uses Sub-frame 0 to talk to the Layer-1 device and Sub-frame 1 to talk to the DSC circuit. It does not reverse its pins.



Note: SBIN is sampled on the rising edge of SCLK, SBOUT is changed on the falling edge of SCLK.

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Figure 6. Serial Bus Port Mode Timing

3. Inter-chip communication between devices on the bus, for instance, data flow between the DSC circuit MAP and an external speech encryption device.
4. Connection of multiple DLCs to the D Channel, including access arbitration. This function is referred to as the TIC Channel and is not applicable to the DSC circuit environment.

A subset of the first three functions is implemented in the Revision E DSC circuit. The fourth, referred to as the TIC Channel, will not be implemented since it is not useful in the DSC circuit environment.

The IOM 2 Terminal Mode bus consists of three IOM 2 subframes, each containing 32 bits. This 12-byte frame is repeated at 8 kHz, resulting in an aggregate data rate of 768 kb/s. The frame structure is illustrated in Figure 7, and contains the following channels:

- Two 64-kb/s data channels, labeled B1 and B2.
- Two device programming channels, labeled Monitor 0 and 1. Each channel has an associated pair of MX and MR handshake bits that control data flow.
- One 16-kb/s D Channel for signaling and data packets.
- Two Command/Indicate channels, labeled C/I_0, and C/I_1, to provide status and command for devices connected via the monitor channels. The Command/Indicate Channel in the first IOM 2 subframe consists of four bits, providing 16 states in each direction. In the second subframe the C/I Channel is 6 bits, providing 64 states in each direction.
- Two 64-kb/s intercommunication channels, labeled IC1 and IC2, to provide additional interdevice communications bandwidth.

All data transmitted on the IOM 2 Interface via the SBOUT pin is transmitted MSB first, with the exception of D-channel data, which is transmitted LSB first. The receiver operates in a compatible way via the SBIN pin.

DSC/IDC Circuit IOM 2 Terminal Mode Implementation

Data Channels

The B1 and B2 Channels are physically the first two 8-bit time slots after the frame sync pulse. When making a MUX connection to these channels, IOM 2 Channels B1 and B2 correspond to MUX Channels Bd and Be, respectively. When in an IOM 2 Mode, a MUX connection to Channel Bf provides access to one of the two intercommunication channels, as selected in PPCR1.

Command/Indicate Channels

The Peripheral Port supports the C/I Channels of the first and second IOM 2 subframes. The Peripheral Port monitors these two channels, and generates an interrupt any time the received data changes and is stable for two frames. The received data is read from C/I Receive Data Register 0 or 1, and C/I transmit data is written to C/I Transmit Data Register 0 or 1.

D Channel

If the Peripheral Port is configured as IOM 2 master, the DLC will transmit and receive D-channel data to and from the S Interface through the LIU. The D-channel data received from the S Interface is also output on the IOM 2 Interface. D-channel data received from the IOM 2 Interface is disregarded.

If the Peripheral Port is configured as IOM 2 slave, the DLC will transmit and receive D-channel data to and from the IOM 2 Interface. The LIU is not used in this situation, so there is no D-channel data flow between the DLC and LIU.

Monitor Channels

Support for the two Monitor Channels is provided on a one-at-a-time basis. A bit in Peripheral Port Control Register 1 selects which one of the two Monitor Channels is utilized at any time.

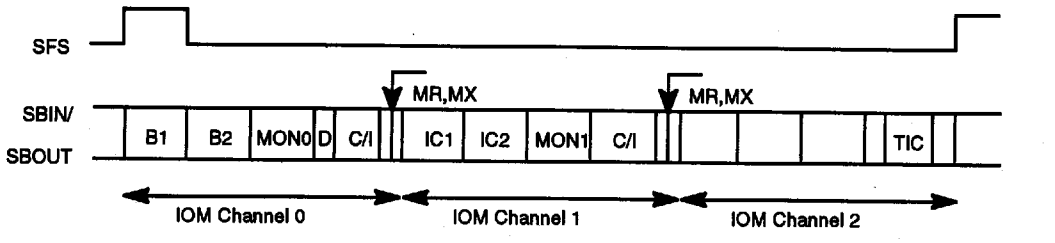

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Figure 7. IOM 2 Terminal Mode Frame Structure

Monitor Channel Procedures

The Monitor Channel operates on an event-driven basis; although data transfers on the bus are synchronized to the frame sync, the flow of data is controlled by a handshake procedure using the outgoing MX and incoming MR bits. Thus, the actual data rate is not fixed, but is dependent upon the response speed of transmitter and receiver. Figure 8 illustrates the sequence of events in the monitor handshake procedure.

Idle State

The outgoing MX and incoming MR bits held inactive for two or more frames indicates that the Monitor Channel is Idle in the outgoing direction.

Start of Transmission

The PPCR1 register is programmed to select one of the two monitor channels. Data is then loaded into the monitor Transmit Data Register, causing the first data byte to be presented to the bus as well as an inactive-to-active transition of outgoing MX. The Monitor Channel transmit buffer available interrupt is also generated when data is placed on the bus, indicating that the next data byte may be written to the buffer. Outgoing MX remains active, and the data is repeated until an inactive-to-active transition of the incoming MR is received.

Subsequent Transmission

Following detection of the first inactive-to-active transition of incoming MR, all following bytes to be transmitted will be presented to the bus coincident with an active-to-inactive transition of outgoing MX. The IOM 2 specification defines a general case (Figure 8a) in which the transmitter waits for an inactive-to-active transition of incoming MR, and a maximum speed case (Figure 8c) in which the transmitter achieves a higher transmission rate by anticipating the falling edge of incoming MR.

The DSC/IDC circuit Monitor Channel transmitter implements the maximum speed case as follows: the second byte is placed onto the bus at the start of the frame following the transition of incoming MR (High to Low), and a Monitor Channel transmit buffer available interrupt is generated. Simultaneously, outgoing MX is returned inactive for one frame, then reactivated. Note that two frames of outgoing MX inactive signifies the end of a message. Outgoing MX and the data byte remain valid until incoming MR goes inactive. The next byte is transmitted during the next frame, meaning one frame after incoming MR goes inactive. In this manner, the transmitter is anticipating incoming MR returning active, which it will do one frame time after it is deactivated, unless an abort is signaled from the receiver. After the last byte of data has been transmitted, indicated by the Monitor Transmit Data Register being empty and the end-of-transmission (EOM) bit being set in PPCR1, outgoing MX is deactivated in response to incoming MR going inactive, and left inactive.

First Byte Reception

At the time the receiver sees the first byte, indicated by the inactive-to-active transition of incoming MX, outgoing MR is by definition inactive. Outgoing MR is activated in response to the activation of incoming MX, the data byte on the bus is loaded into the Monitor Receive Data Register, and a Monitor Channel receive data available interrupt is generated. Outgoing MR remains active until the next byte is received or an end-of-message is detected (incoming MX held inactive for two or more frames).

Subsequent Reception

Data is received into the buffer on each falling edge of incoming MX, and a Monitor Channel receive data available interrupt is generated. Note that the data was actually valid at the time incoming MX became inactive, one frame prior to becoming active. Outgoing MR is deactivated at the time data is read, and reactivated one frame later. The reception of data is terminated by reception of an end-of-message indication, which is incoming MX remaining inactive for two or more frames.

End-of-Transmission (EOM)

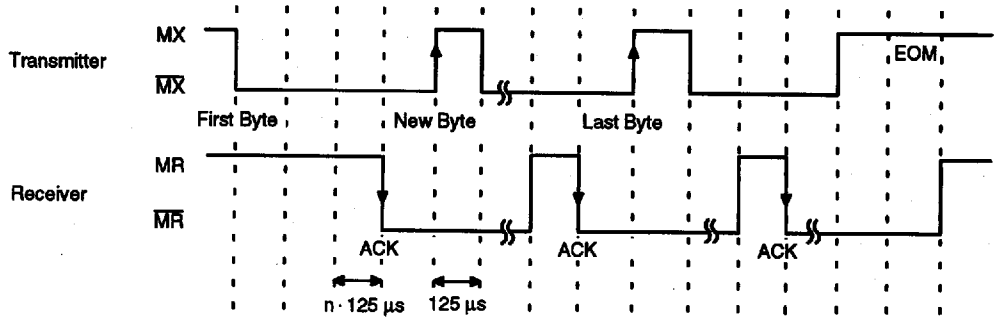
The transmitter sends an EOM in response to the EOM request bit being set in PPCR1. Once the EOM bit is set, the EOM is transmitted as soon as the Monitor Transmit Data Register becomes empty. This is normally done when the last byte of a message has been transmitted. The DSC/IDC circuit transmits an EOM simply by not reactivating MX after deactivating it in response to MR going inactive. The EOM request bit in PPCR1 is automatically cleared when the EOM has been transmitted, indicating that the monitor transmitter is available for a new message.

Abort

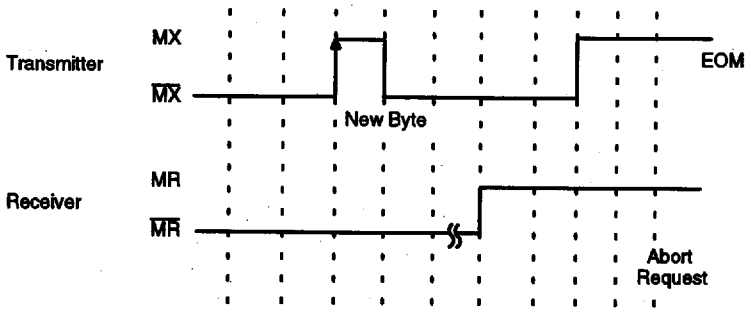
An abort is a signal from the receiver to the transmitter indicating that data has been missed. The receiver sends an abort by holding MR inactive for two or more frames in response to MX going active. An interrupt is generated when an abort is received.

Flow Control

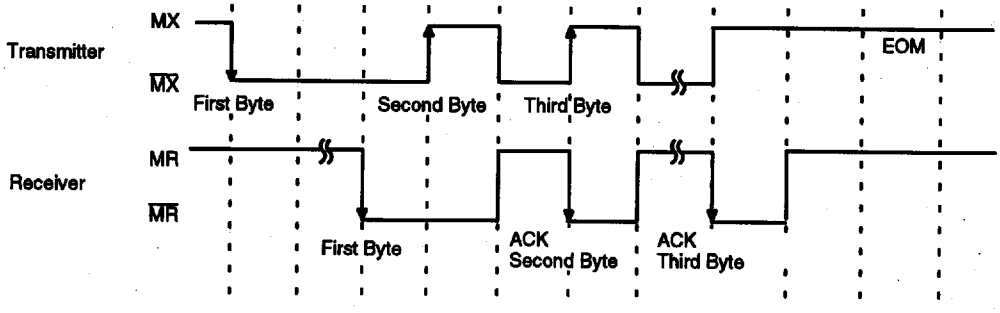
The transmitter is held off until the Monitor Receive Data Register is read, since MR is held active until the receive byte is read. The transmitter will not start the next transmission cycle until MR goes inactive.



a. General Case



b. Abort Request from the Receiver



c. Maximum Speed Case

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Figure 8. Monitor Handshake Timing

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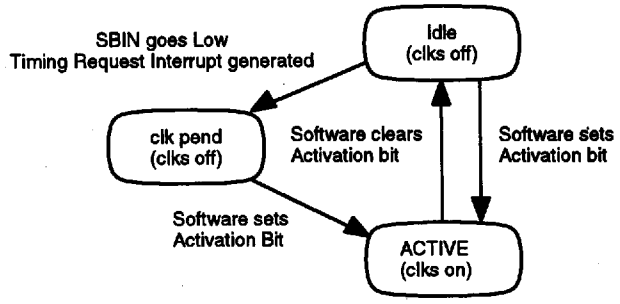
IOM 2 Activation/Deactivation

The IOM 2 Interface includes an activation/deactivation capability (see Figure 9). Activation and deactivation can be initiated from either upstream or downstream components on the bus. When deactivated, the upstream device holds all the clock outputs Low, and the downstream devices force their open drain data outputs to a High-Z state (seen as a High on the system bus due to the external pullup resistor). The activation/deactivation procedure is a combination of software handshakes via the C/I Channel, and hardware indications via the clock and data lines. The IOM 2 specification describes both the hardware and software protocols in detail; the hardware operation supported by the Am79C30A IOM 2 implementation is outlined below.

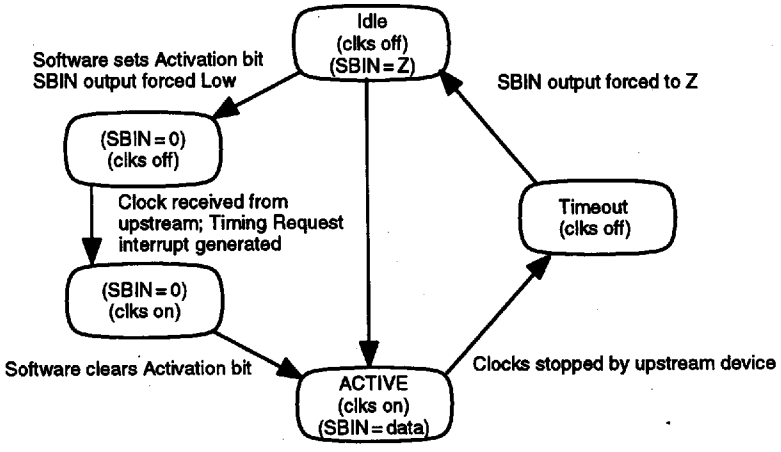
DSC/IDC Circuit as Upstream Device (Clock Master)

Deactivation

Deactivation of the IOM 2 Interface from the Am79C30A operating as an upstream device is initiated and controlled by the microprocessor. A series of software handshakes via the C/I Channel must be performed before the hardware deactivation can take place. The upstream device must issue a deactivation request command on the C/I Channel and wait for a deactivation indication from all downstream units. Once this is received, a deactivation confirmation command must be sent on the C/I Channel by the upstream device. The upstream device will then stop all clocks and hold them Low. On the Am79C30A, the IOM 2 clocks (SCLK, SFS, and BCL/CH2STRB) are stopped and forced Low



Am79C30A as Upstream Device



Am79C30A as Downstream Device

Note: This diagram shows only the portions of the IOM 2 activation/deactivation procedures that are affected by the Am79C30A hardware. The C/I-channel software handshakes are not shown.

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Figure 9. IOM 2 Activation/Deactivation

when the microprocessor clears the activation/deactivation bit in the Peripheral Port Control Register Number 1 (PPCR1). When this bit is cleared, the data output pin (SBOUT) is also forced to High-Z (seen as a High on the system bus due to the external pullup resistor), and the Am79C30A begins monitoring the data input pin (SBIN) for the presence of a timing request from any downstream units.

Activation

Activation can be initiated locally by the processor or remotely by one of the downstream units. To activate locally, the processor sets the activation/deactivation bit in PPCR1 (starting the clocks), and then proceeds through the software activation protocol on the C/I Channel. For remote activation, the upstream device receives a request from the downstream device via the data input pin. When the data input pin (SBIN) goes Low, Am79C30A will generate an IOM 2 timing-request interrupt, Bit 6 in the Peripheral Port Status Register (PPSR). The processor must respond to this interrupt, and restart the IOM 2 clocks by setting the activation/deactivation bit in PPCR1. Once the clocks are running, the downstream device can request full activation via the C/I Channel using the IOM 2 software protocol.

DSC/IDC Circuit as a Downstream Device (Clock Slave)

Deactivation

Deactivation is normally initiated by the upstream device as described above. When the deactivation request is received by the downstream device over the C/I Channel, the processor must respond by sending the deactivation indication over the C/I Channel. The upstream device will then send the deactivation confirmation command over the C/I Channel and stop the IOM 2 clocks. The Am79C30A will detect that the clock has stopped (defined as no clock pulse received for 650 ns) and force itself to the deactivated state. In the deactivated state, SBIN, and SBOUT are both forced to a High-Z state, and the SCLK input is monitored for any rising edge that would indicate an activation request from the upstream device.

Activation

Once again, activation can originate from either the upstream or the downstream device. To activate the interface from the downstream device, the processor sets the activation/deactivation bit in the PPCR1 register. This will force the Am79C30A to pull its data output pin (SBIN in this case, since the I/O pin definition is reversed when talking to the upstream device) Low, causing the upstream device to start the IOM 2 clocks. Once the clocks are running, as indicated by SCLK input going High, the Am79C30A will generate an IOM 2 timing request interrupt (Bit 6 in PPSR). The processor must respond to the interrupt by loading the proper C/I command response into C/ITRDO, then clearing the activation/deactivation bit in PPCR1. This will release the data output pin (SBIN) from being held Low and allow the processor to complete the activation procedure by sending the proper commands over the C/I Channel.

When the activation is originated from the upstream device, the Am79C30A will generate an IOM 2 timing request interrupt (Bit 6 in PPSR) when the IOM 2 clocks become active as indicated by the SCLK input pin going High. The Am79C30A will begin normal IOM 2 transmission/reception as soon as SCLK appears; no intervention from the microprocessor is required. However, the processor must respond to the interrupt and perform the normal C/I Channel software handshakes before activation will be complete.

Peripheral Port Registers

The PP contains the following registers:

Registers	# of Registers	Mnemonic
Peripheral Port Control Register	2	PPCR1, PPCR2
Peripheral Port Status Register	1	PPSR
Peripheral Port Interrupt Enable Register	1	PPIER
Monitor Transmit Data Register	1	MTDR
Monitor Receive Data Register	1	MRDR
C/I Transmit Data Register	2	CITDR0, CITDR1
C/I Receive Data Register	2	CIRDR0, CIRDR1

Peripheral Port Control Register 1 (PPCR1) Default = 01 Hex; Address = Indirect C0 Hex, Read/Write

7	6	5	4	3	2	1	0
MONTR ABORT RQST	MONTR ENABL	MONTR CHANL SELECT	MONTR EOM RQST	IC CHANL SELECT	IOM 2 ACTV/ DEACT	PORT MODE SELECT BIT 1	PORT MODE SELECT BIT 0

Bit	Function
7	**Monitor Channel Abort Request**—This bit is automatically cleared during RESET or manually by software as follows: to send an ABORT message, software should set this bit, wait at least two frames, then clear the bit.
6	**Monitor Channel Enable**—This bit only affects IOM 2 operation. When set, the selected Monitor Channel is enabled. When cleared, both monitor channels are disabled. Whenever the Monitor Channel is disabled, the Monitor Transmit and Receive Data Register (MTDR, MRDR) are updated to their default states: MTDR = FFH, MRDR = 00H.
5	**Monitor Channel Select**—This bit only affects IOM 2 operation. When set, Monitor Channel 1 is used (second subframe). When cleared, Monitor Channel 0 is used (first subframe).
4	**Monitor End-of-Message Request**—When set, this bit forces the Monitor Channel transmitter to send an EOM once all data written into the Monitor Transmit Data Register has been transmitted. This tells the receiving device that the message is complete. The bit is cleared by hardware when the EOM is sent by reset or by software.
3	**IC Channel Select**—This bit only affects IOM 2 operation. When set, the IC2 time slot is used (sixth octet after the frame sync). When cleared, the IC1 time slot is used (fifth octet after the frame sync). The unused channel is always placed in a high-impedance state.
2	**IOM 2 Activation/Deactivation Bit**—This bit only affects IOM 2 operation. Note that this bit controls only the starting and stopping of SCLK, BCL/CH2STRB, SFS, and the state of the SBIN/SBOUT pins; this alone does not constitute activation or deactivation of the IOM 2 bus. The activation/deactivation procedure involves the exchange of a series of commands and indications over the C/I Channel. This procedure, including a state diagram, is detailed in the IOM 2 specification. IOM 2 Master Mode—This bit is set by software. When deactivated, the master will turn on SCLK, BCL/CH2STRB, and SFS clocks via software by setting this bit when the SBIN pin is pulled Low, indicating that a downstream device wishes to communicate over the interface. The IOM 2 activation/deactivation bit is cleared by software or reset. When cleared, the clocks are stopped, and SBIN is monitored for the reactivation request from the slave (SBIN held Low). [Reset defaults the Peripheral Port to SBP operation.] IOM 2 Slave Mode—This bit is set by software to initiate an activation request to the master. When set, the SBIN pin is driven Low, and held Low until the activation/deactivation bit is cleared by software. In response to SBIN going Low the master will start SCLK, which generates a timing request interrupt in the DSC circuit. The activation/ deactivation bit is cleared by software in response to this interrupt.

Peripheral Port Control Register 1 (PPCR1)—(continued) ADV MICRO (TELECOM)

Bit	Function
1–0	**Port Mode Select Field**—These two bits select the configuration of the Peripheral Port as follows:

Bit 1	Bit 0	Function
0	0	Port disabled
0	1	SBP Mode, enabled
1	0	IOM 2 Slave Mode, enabled
1	1	IOM 2 Master Mode, enabled

When the port is disabled, SBOUT, SBIN, and all port-related clocks are placed in a high-impedance state.

When the DSC circuit is reset, this bit field is set to 01, and the port is not enabled until a MUX MCR register is written to. If this bit is cleared prior to such a path being programmed, the port will remain disabled until the bit is set via a software write operation.

Peripheral Port Status Register (PPSR)
Default = Bit 1 = 1, Bits 6-2 and 0 = 0, Bit 7 is Indeterminate; Address = Indirect C1 Hex, Read

7	6	5	4	3	2	1	0
RSRVD	IOM-2 TIME RQST	CHNG IN C/I 1 DATA	CHNG IN C/I 0 DATA	MONTR ABORT RECVD	MONTR EOM RECVD	MONTR XMIT BUFFR AVAIL	MONTR RECV DATA AVAIL

The Peripheral Port Status Register presents various status conditions to the user, and is only used in the IOM 2 Mode. Each of these conditions can generate an interrupt to the user. The interrupts are enabled via the Peripheral Port Interrupt Enable Register. The state of the respective interrupt enable bits does not affect the setting of bits in this register. Bits 6, 3, and 2 are cleared when this register is read. Bit 1 is cleared when the Data Register is written, and Bit 0 is cleared when the Data Register is read. In addition, Bits 3, 2, 1, and 0 are cleared when the Monitor Channel is disabled (via Bit 6 of the PPCR1 Register). Because Bit 7 is reserved, the default value of this register is either 02H or 82H.

Bit	Function
6	**IOM 2 Timing Request**—When the DSC circuit is the upstream device (master mode), this bit is set by hardware to indicate that a downstream device has requested the starting of the IOM 2 clocks. The clocks are started by software. This bit does not indicate the receipt of an activation request on the C/I Channel. When the DSC circuit is the downstream component (slave mode), this bit is set in response to SCLK starting (going High) when the bus is deactivated. *Note: The DSC circuit will not exit Power-Down Mode in response to either a timing request or the clocks being started, if this interrupt is masked. It is essential that an interrupt be generated when the DSC circuit leaves Power-Down Mode. Otherwise, power consumption could increase significantly without the processor's knowledge.*
5	**Change in C/I 1 Channel Status**—This bit is set by hardware to indicate that the contents on the receive side of C/I Channel 1 have changed since the C/I Receive Data Register was last read.
4	**Change in C/I 0 Channel Status**—This bit is set by hardware to indicate that the contents on the receive side of C/I Channel 0 have changed since the C/I Receive Data Register was last read.
3	**Monitor Channel Abort Request Received**—This bit is set by hardware to indicate that an abort request has been received on the monitor channel. This indicates that the receiver on the other end of the Monitor Channel has failed to receive the transmitted data correctly, and wishes that the current transmission be discontinued, and the data transmission repeated via software.
2	**Monitor Channel End-of-Message Indication Received**—This bit is set by hardware to indicate that an EOM has been received on the monitor channel. This indicates that the message currently being received has concluded.
1	**Monitor Channel Transmit Buffer Available**—This bit is set by hardware to indicate that a new byte of data can be loaded into the Monitor Transmit Data Register.
0	**Monitor Channel Receive Data Available**—This bit is set by hardware to indicate that a byte of data has been received on the monitor channel and is available in the Monitor Receive Data Register.

Peripheral Port Interrupt Enable Register (PPIER) = 1
Default = Write = 00 Hex, Read = Bit 7 = 1, Bits 6–0 = 0; Address = Indirect C2 Hex, Read/Write

7	6	5	4	3	2	1	0
PP/MF INT EN	ENABL IOM 2 TIME RQST	ENABL CHNG IN C/I1 DATA	ENABL CHNG IN C/I0 DATA	ENABL MONTR ABORT RECVD	ENABL MONTR EOM RECVD	ENABL MONTR XMIT BUFFR AVAIL	ENABL MONTR RECV DATA AVAIL

The Peripheral Port Interrupt Enable Register provides an individual interrupt-enable bit corresponding with each of the status conditions in the Peripheral Port Status Register. When set, the interrupt is enabled. Clearing the bit disables the interrupt. These bits are set and cleared by software.

Bit	Function

7 **PP/MF Interrupt Enable**—When set, this bit enables the Peripheral Port and Multiframing interrupts. When cleared, the PP and MF interrupts are disabled.

Note: To ensure proper interrupt reporting, software must disable PP/MF interrupts when the interrupt routine is entered and enable them when exiting.

Monitor Transmit Data Register (MTDR) Default = FF Hex; Address = Indirect C3 Hex, Write

7	6	5	4	3	2	1	0
DATA BIT 7 (MSB)	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0 (LSB)

The Monitor Transmit Data Register is the user-visible portion of the Monitor Channel Transmitter Data Buffer. Data is written into this register by the user in response to a monitor transmit buffer available interrupt. It is then transmitted to the receiver on the other side of the IOM 2 bus. The MTDR is emptied when the PP is reset.

Monitor Receive Data Register (MRDR) Default = 00 Hex; Address = Indirect C3 Hex, Read

7	6	5	4	3	2	1	0
DATA BIT 7 (MSB)	DATA BIT 6	DATA BIT 5	DATA BIT 4	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0 (LSB)

The Monitor Receive Data Register is the user-visible portion of the Monitor Channel Receiver Data Buffer. Data is written into this register by the hardware as it is received over the monitor channel. A monitor data available interrupt is generated when the register is loaded. The register is overwritten by hardware only after the register has been read. The default on reset is 00 hex.

C/I Transmit Data Register 0 (C/ITDR0) Default = 0F Hex; Address = Indirect C4 Hex, Write

7	6	5	4	3	2	1	0
RSRVD	RSRVD	RSRVD	RSRVD	C/I0 DATA BIT 3 (MSB)	C/I0 DATA BIT 2	C/I0 DATA BIT 1	C/I0 DATA BIT 0 (LSB)

The C/I Transmit Data Register 0 is the user-visible portion of the C/I Channel 0 transmitter. Data can be written into this register by the user at any time and is transmitted continuously during each subsequent frame until changed. The register is set to its default value, 0F hex (C/I Channel idle), by reset or disabling of the Peripheral Port.

C/I Receive Data Register 0 (C/IRDR0) Default = XF Hex; Address = Indirect C4 Hex, Read

7	6	5	4	3	2	1	0
RSRVD	RSRVD	RSRVD	RSRVD	C/I0 DATA BIT 3 (MSB)	C/I0 DATA BIT 2	C/I0 DATA BIT 1	C/I0 DATA BIT 0 (LSB)

The C/I Receive Data Register 0 contains data valid for two frames from C/I Receive Channel 0. The register is set to its default value of XF hex by a reset or the disabling of the Peripheral Port.

C/I Transmit Data Register 1 (C/I TDR1) Default = 3F Hex; Address = Indirect C5 Hex, Write

7	6	5	4	3	2	1	0
RSRVD	RSRVD	C/I1 DATA BIT 5 (MSB)	C/I1 DATA BIT 4	C/I1 DATA BIT 3	C/I1 DATA BIT 2	C/I1 DATA BIT 1	C/I1 DATA BIT 0 (LSB)

The C/I Transmit Data Register 1 is the user-visible portion of the C/I Channel 1 transmitter. Data can be written into this register by the user at any time. It is transmitted continuously during each subsequent frame until changed. The register is set to its default value, 3F hex (C/I Channel idle), by reset or disabling of the Peripheral Port.

C/I Receive Data Register 1 (C/IRDR1)
Default = Bits 7 and 6 are Indeterminate, Bits 5–0 = 1; Address = Indirect C5 Hex, Read

7	6	5	4	3	2	1	0
RSRVD	RSRVD	C/I1 DATA BIT 5 (MSB)	C/I1 DATA BIT 4	C/I1 DATA BIT 3	C/I1 DATA BIT 2	C/I1 DATA BIT 1	C/I1 DATA BIT 0 (LSB)

The C/I Receive Data Register 1 contains the data (valid for two frames) from C/I Receive Channel 1. The register is set to its default value by a reset or the disabling of the Peripheral Port.

Peripheral Port Control Register 2 (PPCR2)
Default = Bits 7, 6, and 0 = 0, Bit 5 = 1, Bits 4–1 are Indeterminate*; Address = Indirect C8 Hex, Read/Write

7	6	5	4	3	2	1	0
REV CODE BIT 2 (MSB)	REV CODE BIT 1	REV CODE BIT 0 (LSB)	RSRVD	RSRVD	RSRVD	RSRVD	SCLK INVRT ENABL

The Peripheral Port Control Register 2 controls the inversion of the SCLK output in SBP Mode. This provides flexibility in the connection of peripheral devices to the DSC circuit. The hardware revision code is also contained in this register, which allows software to identify the revision of the hardware.

* The default value is revision-level dependent. Revision E will report a hardware revision code of 001.

Bit	Function
7–5	**Hardware Revision Code**—This read-only field reports the hardware revision level. Revision E of the DSC circuit will report a hardware revision code of 001.
0	**SCLK Inversion Enable**—When set, the SCLK output is inverted in SBP Mode. When cleared, the SCLK output is identical to the Revision D DSC circuit. This bit should not be changed while SCLK is enabled.

APPLICATIONS

ISDN Feature Phone

This basic feature phone is the ISDN equivalent to the common analog phone. The keypad can be a simple four-by-four single pole switch matrix or a larger matrix to provide full key system features. The display option illustrated in Figure 10 can be included in any of the applications shown in this section.

ISDN Feature Phone with Parallel and Serial Data Ports Plus Other Peripherals

Access to the CCITT R reference interface is provided via both the serial and parallel ports in Figure 11. This application may easily have voice capability added by using a DSC circuit in place of the IDC circuit. Figure 12 illustrates applications with increased B-channel data processing requirements.

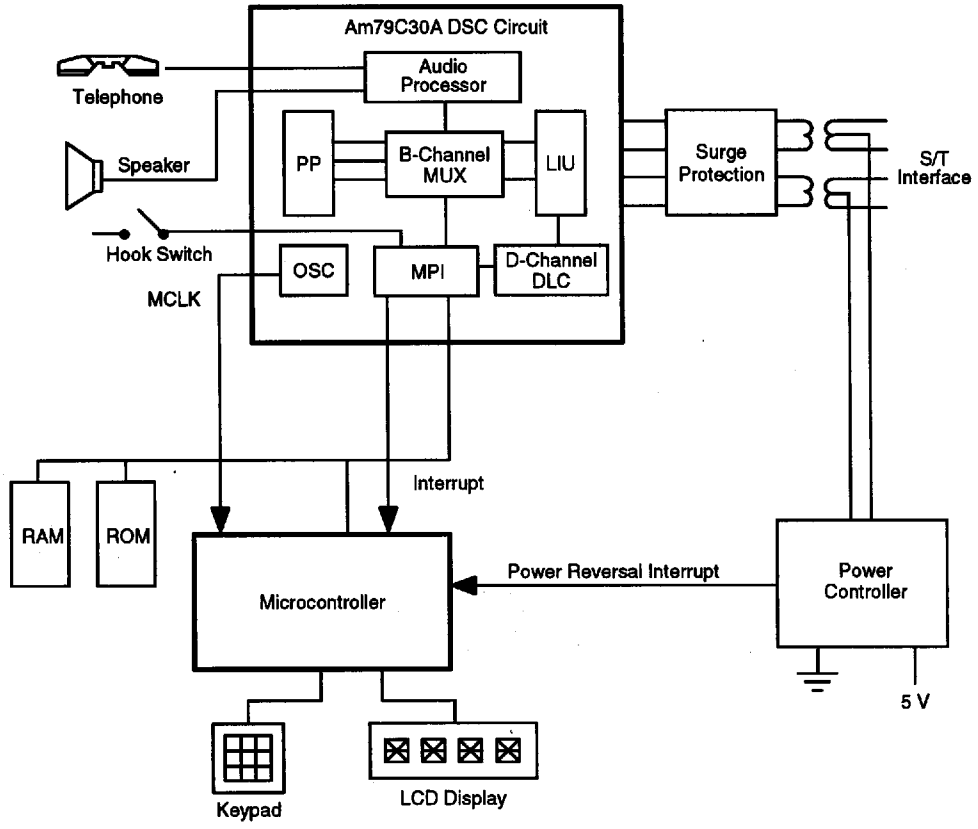

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Figure 10. ISDN Telephone

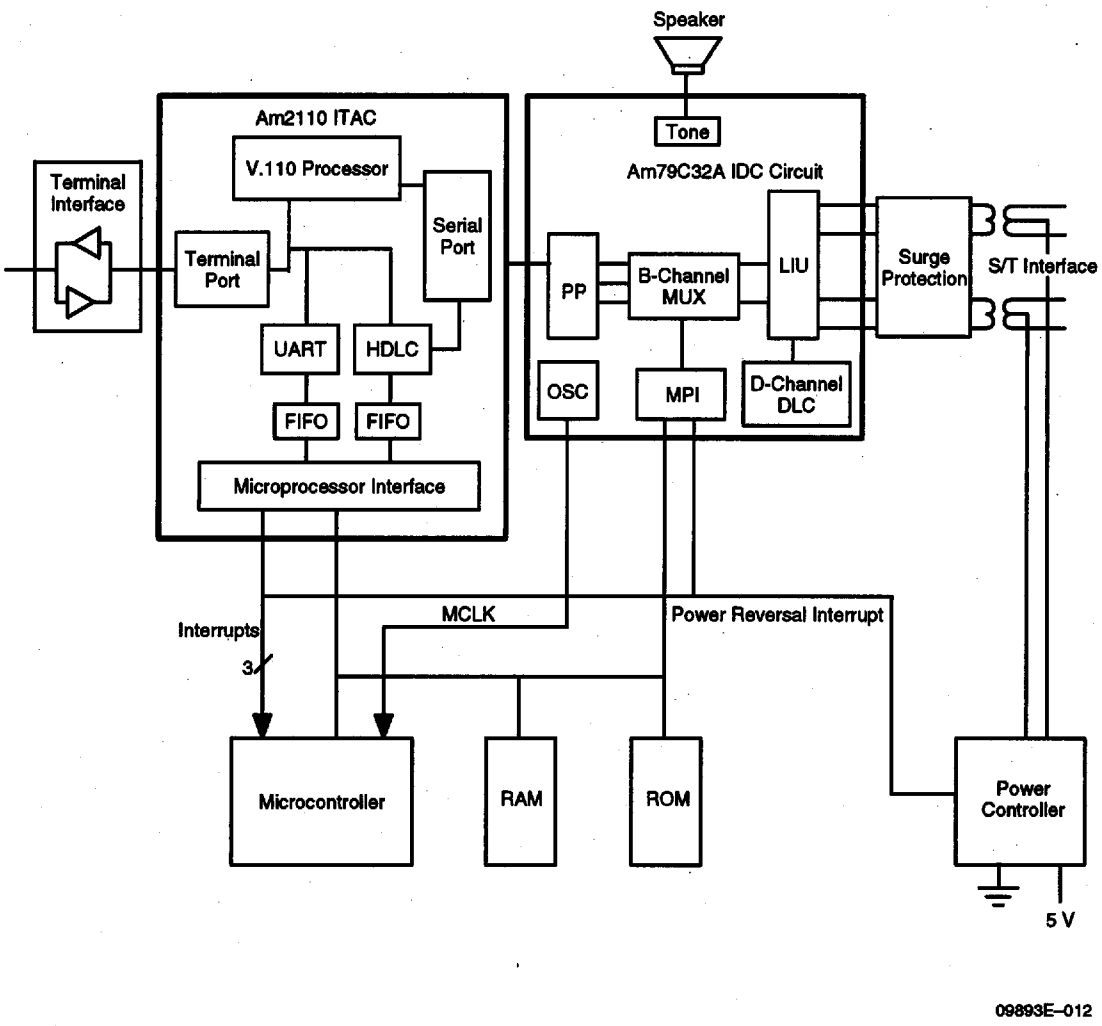

Figure 11. Terminal Adaptor (V.110/V.120) With Voice Upgrade Capability

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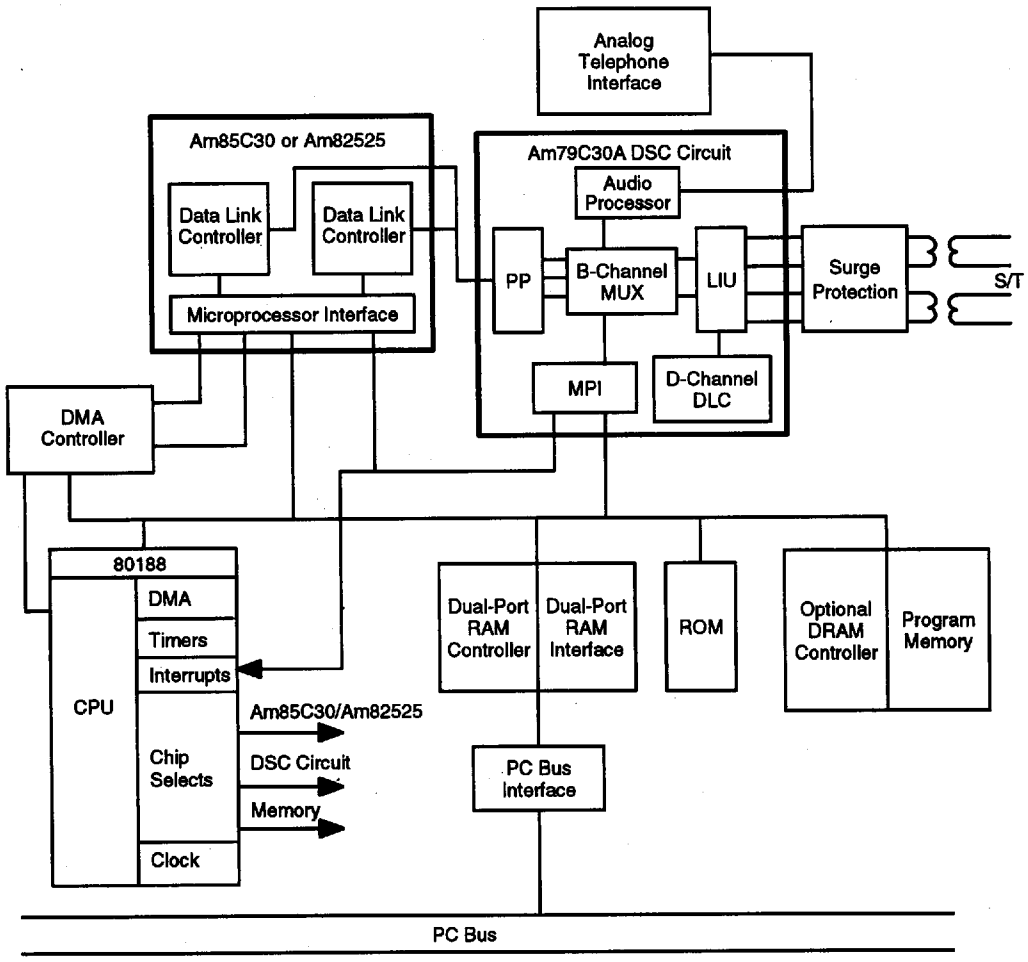

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Figure 12. PC Add-On-Board (1 or 2 Data Channels)

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage temperature ..... –65°C to +150°C
Ambient temperature
with power applied ..... –55°C to +125°C
Supply voltage to ground,
potential continuous ..... 0 V to +7.0 V
Lead temperature (soldering, 10 sec) ..... 300°C
Maximum power dissipation ..... 1.5 W
Voltage from any
pin to V_{SS} ..... V_{SS} – 0.5 V to V_{CC} + 0.5 V
DC input/output current
(except LS1, LS2) ..... 10 mA
DC output current, LS1, LS2 only ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) devices
Operating V_{CC} range with respect
to V_{SS} ..... 4.75 V to 5.25 V
Ambient temperature (T_A) ..... 0°C to +70°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics over Commercial operating ranges (unless otherwise specified)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IH}	Input High Level, except XTAL2		2.0	V_{CC} + 0.25	V
V_{IH2}	Input High Level XTAL2		0.8 V_{CC}	V_{CC} + 0.25	V
V_{IL}	Input Low Level		V_{SS} – 0.25	0.8	V
V_{OL}	Output Low Level, except SBOUT Output Low Level, SBOUT only	I_{OL} = 2 mA I_{OL} = 7 mA		0.4 0.4	V
V_{OH}	Output High Level	I_{OH} = –400 µA = –10 µA	2.4 0.9 V_{CC}		V
I_{OL}	Output Leakage Current	0 < V_{OUT} < V_{CC} Output in High-Z State		±10	µA
I_{IL}	Input Leakage Current Digital Inputs LIN1/LIN2 XTAL2	0 < V_{IN} < V_{CC}		 ±10 ±200 TBD	 µA µA µA
C_I	Input Capacitance Digital Input	Temp = 25°C Freq = 1 MHz		10 (TYP)	pF
C_O	Output Capacitance Digital Input/Output	Temp = 25°C Freq = 1 MHz		15 (TYP)	pF

Table 9. Revision E Power Specifications for CCITT-Restricted Mode Phone Operation

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Typ	Preliminary Max	Unit
I_{CC0}	V_{CC} Supply Current (Power-Down Mode)	V_{CC} = 5.25 V; V_{IH} = V_{CC}; V_{IL} = V_{SS}; Mode = Power-Down; Clocks & Oscillator Stopped; LIU Receiver Enabled; S Interface Silent (INFO 0)	4	5	mW
I_{CC1}	V_{CC} Supply Current (Idle Mode)	V_{CC} = 5.25 V; V_{IH} = V_{CC}; V_{IL} = V_{SS}; Mode = Idle; f_{MCLK} = 384 kHz; LIU Receiver Enabled; S Interface Silent (INFO 0)	20	25	mW
I_{CC2}	V_{CC} Supply Current (Active; Call Set-Up)	V_{CC} = 5.25 V; V_{IH} = V_{CC}; V_{IL} = V_{SS}; Mode = Active, Data Only; f_{MCLK} = 3.072 MHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D Channel Only; S-interface Load = 50 ohms	80	105	mW
I_{CC3}	V_{CC} Supply Current (Active; Voice Mode)	V_{CC} = 5.25 V; V_{IH} = V_{CC}; V_{IL} = V_{SS}; Mode = Active Voice & Data; f_{MCLK} = 384 MHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D Channel and one B Channel; S-interface Load = 50 ohms; AINA = −15 dBm0, 1-kHz Sine Wave; EAR1/EAR2 = −15 dBm0, 1-kHz Tone Driving 600 ohms	155	190	mW
I_{CC4}	V_{CC} Supply Current (Active; Ringing, No Load*)	V_{CC} = 5.25 V; V_{IH} = V_{CC}; V_{IL} = V_{SS}; Mode = Active, Data Only; f_{MCLK} = 384 kHz; LIU Receiver and Transmitter Enabled; S Interface Activated with Data on D Channel Only; S-interface Load = 50 ohms; Secondary Tone Ringer Enabled at 0 dB, 400 Hz, No Load	125	150	mW

Note: All power measurements assume PP disabled or in IOM 2 Deactivated Mode.

*Power Consumption with the output loaded will be $I_{CC4} + \frac{(V_{OUT}, peak)}{R_{LOAD}} (V_{CC})$

For R_{LOAD} = 50 ohms and V_{OUT} = −12 dB (625 mV, peak), the maximum power consumption will be 215 mW.

AC Characteristics

V_{CC} = 5 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; MCLK = 3.072 MHz

MAP Analog Characteristics (Am79C30A Only)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
Z_{IN}	Analog Input Impedance AINA or AINB to AREF	−1.25 V < V_{IN} < +1.25 V f_{IN} < 4 kHz	200			Kohm
V_{IOS}	Allowable Offset Voltage at AINA or AINB	with respect to AREF pin	−5		+5	mV
L_{LS}	Allowable Load LS1 to LS2			R_{LOAD} > 40 ohms and C_{LOAD} < 100 pF		
L_{EAR}	Allowable Load EAR1 to EAR2			R_{LOAD} > 540 ohms and C_{LOAD} < 100 pF		
L_{AREF}	Allowable Load AREF to V_{SS} or V_{CC}			R_{LOAD} > 1 Kohm and C_{LOAD} < 100 pF		
V_{AREF}	Analog Reference Voltage		2.25	2.4	2.55	V

MAP Transmission Characteristics (Am79C30A only)

The half channel parameters are specified from AINA or AINB input pins to a B Channel for the transmit path, and from a B Channel to EAR1/EAR2 or LS1/LS2 pins measured differentially for the receive path. The parameters are applicable for both A- or μ-law conversion. (A-law assumes psophometric filtering, and μ-law assumes c-message weighting.) All parameters are specified with the GR, X, R, GX, and GER filters disabled; STG filter is enabled but is programmed for infinite attenuation.

All limits are guaranteed for V_{CC} = 5 V±5%, T_A = 0°C to 70°C, and programmable filters/gains disabled (0 dB, flat) unless otherwise indicated.

ADV MICRO (TELECOM)

MAP Transmission Characteristics (Am79C30A Only)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Min	Typ	Max	Unit
TXG1	Transmit Absolute Gain (Nominal)	0 dBm0; 1020 Hz; V_{CC} = 5 V; T = 25°C	−0.30		+0.30	dB
TXG2	Transmit Gain Variation vs Temperature and V_{CC}	0 dBm0; 1020 Hz	−0.25		+0.25	dB
TXG3	Transmit Gain Variation vs Programmed Gain in GX	0 dBm0; 1020 Hz	−0.15		+0.15	dB
TXG4	Transmit Gain Variation vs Programmed Gain in GA	0 dBm0; 1020 Hz	−0.25		+0.25	dB
RXG1E	Receive Absolute Gain at EAR1/EAR2 (Nominal)	0 dBm0; 1020 Hz; V_{CC} = 5 V; T = 25°C; R_{LOAD} > 540 ohms	−0.30		+0.30	dB
RXG1L	Receive Absolute Gain at LS1/LS2 (Nominal)	0 dBm0; 1020 Hz; V_{CC} = 5 V; T = 25°C; R_{LOAD} > 40 ohms	−0.50		+0.50	dB
RXG2	Receive Gain Variation vs Temperature and V_{CC}	0 dBm0; 1020 Hz	−0.25		+0.25	dB
RXG3	Receive Gain Variation vs Programmed Gain in GR and GER	0 dBm0; 1020 Hz	−0.25		+0.25	dB
TXF	Transmit Frequency Response (Attenuation vs Frequency Relative to −10 dBm0 at 1020 Hz)—see Figure 13	*50 Hz–60 Hz < 300 Hz 0.3 kHz–3.0 kHz 3.0 kHz–3.4 kHz 3.4 kHz–3.6 kHz 3.6 kHz–3.9 kHz 3.9 kHz–4.0 kHz	24.0 −0.25 −0.25 −0.25 −0.25 0.0 9.0		 +0.25 +0.9 	dB dB dB dB dB dB dB
RXF	Receive Frequency Response (Attenuation vs Frequency Relative to −10 dBm0 at 1020 Hz)—see Figure 17	< 300 Hz 0.3 kHz–3.0 kHz 3.0 kHz–3.4 kHz 3.4 kHz–3.6 kHz 3.6 kHz–3.9 kHz 3.9 kHz–4.0 kHz	−0.25 −0.25 −0.25 −0.25 0.0 9.0		 +0.25 +0.9 	dB dB dB dB dB dB
TXD	Transmit Group Delay Variation vs Frequency at −10 dBm0 Relative to Minimum Delay Frequency—see Figure 14	500 Hz–600 Hz 600 Hz–1000 Hz 1.0 kHz–2.6 kHz 2.6 kHz–2.8 kHz			750 380 130 750	μs μs μs μs
RXD	Receive Group Delay Variation vs Frequency at −10 dBm0 Relative to Minimum Delay Frequency—see Figure 18	500 Hz–600 Hz 600 Hz–1000 Hz 1.0 kHz–2.6 kHz 2.6 kHz–2.8 kHz			750 380 130 750	μs μs μs μs
TXSTD	Transmit Signal/Total Distortion vs Level; CCITT Method 2, 1020 Hz (Transmit Gain = 0dB)—see Figure 16	0 to −30 dBm0 −40 dBm0 −45 dBm0	35.0 29.0 24.0			dB dB dB
RXSTD	Receive Signal/Total Distortion vs Level; CCITT Method 2, 1020 Hz (Transmit Gain = 0dB)—see Figure 20	0 to −30 dBm0 −40 dBm0 −45 dBm0	35.0 29.0 24.0			dB dB dB

*Measured with the high pass filter and auto-zero enabled in MMR2.

MAP Transmission Characteristics (Am79C30A Only)—(continued)

Parameter Symbol	Parameter Descriptions	Test Conditions	Preliminary Min	Typ	Max	Unit
TXGT	Transmit Gain Tracking vs Level; CCITT Method 2, 1020 Hz (Transmit Gain = 0 dB)—see Figure 15	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.3 −0.6 −1.6		+0.3 +0.6 +1.6	dB dB dB
RXGT	Receive Gain Tracking vs Level; CCITT Method 2, 1020 Hz (Receive Gain = 0 dB)—see Figure 19	+3 to −40 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.3 −0.6 −1.6		+0.3 +0.6 +1.6	dB dB dB
TXICN	Transmit Idle Channel Noise AINA or AINB Connected to AREF	GX = 0 dB, GA = 0 dB GX = 6 dB, GA = 0 dB GX = 6 dB, GA = 6 dB GX = 6 dB, GA = 12 dB GX = 6 dB, GA = 18 dB		−82 −79 −76 −73 −70	−78 −75 −72 −69 −66	dBm0 dBm0 dBm0 dBm0 dBm0
RXICN	Receive Idle Channel Noise	GR = 0 dB, GER = 0 dB GR = −12 dB, GER = 0 dB		−90 −80	−85 −75	dBm0 dBm0

*Measured with the high pass filter and auto-zero enabled in MMR2.

Notes: The following test conditions apply to all MAP tests:

1. An external 1-Kohm ±5% resistor and 2200-pF ±10% capacitor are connected in series between the CAP1 and CAP2 pins for all transmit tests.
2. All tests are half-channel with the sidetone path enabled but programmed for infinite attenuation (STG = 9008 hex).
3. Transmit specs are guaranteed for both AINA and AINB inputs with the auto-zero and high-pass filters enabled in MMR2.
4. Transmit specs are tested and guaranteed with the input signal source referenced to AREF; see test circuit below.
5. Receive specs are guaranteed for both EAR1/EAR2 and LS1/LS2 outputs measured differentially. Some degradation in performance may occur if used single ended rather than differential.

Transmitter 0-dB Reference Point:

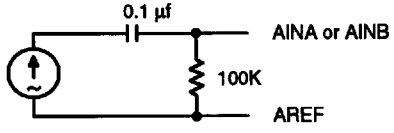
Nominal input voltage at AINA or AINB will produce a 0-dBm, 1-kHz digital code at the transmit output with all transmit gains at 0 dB.

A law = 625 mV rms
μ law = 620 mV rms

Receiver 0-dB Reference Point:

Nominal output voltage between EAR1/EAR2 or LS1/LS2 resulting from a 0-dBm, 1-kHz digital code at the receive input with all receive gains at 0 dB.

A law = 1.25 V rms
μ law = 1.2 V rms



Transmit Test Circuit with Input Source Referenced to AREF

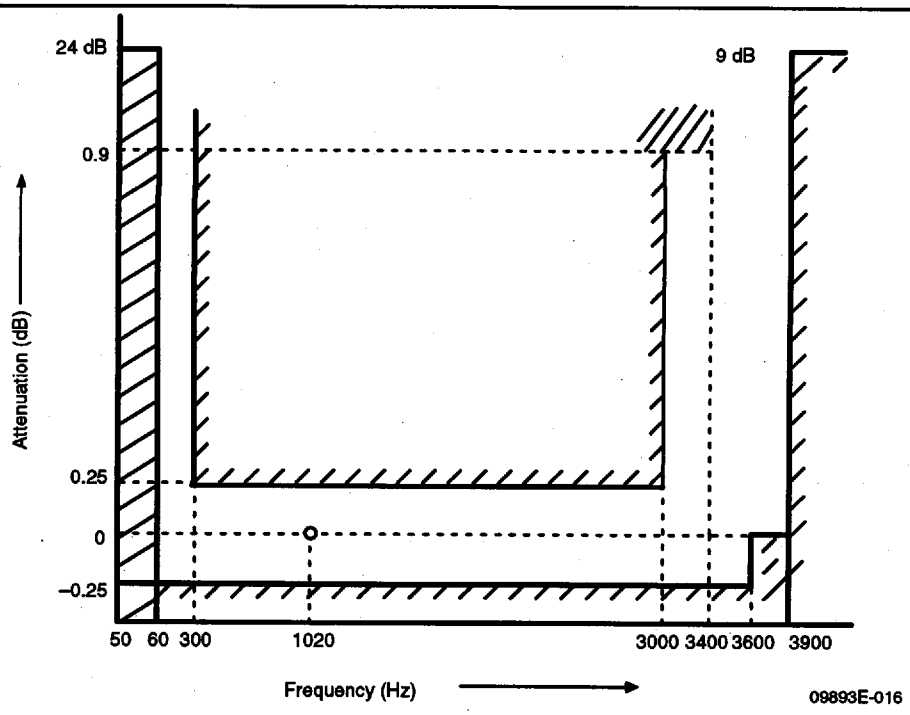


Figure 13. Attenuation/Frequency Distortion (Transmit)

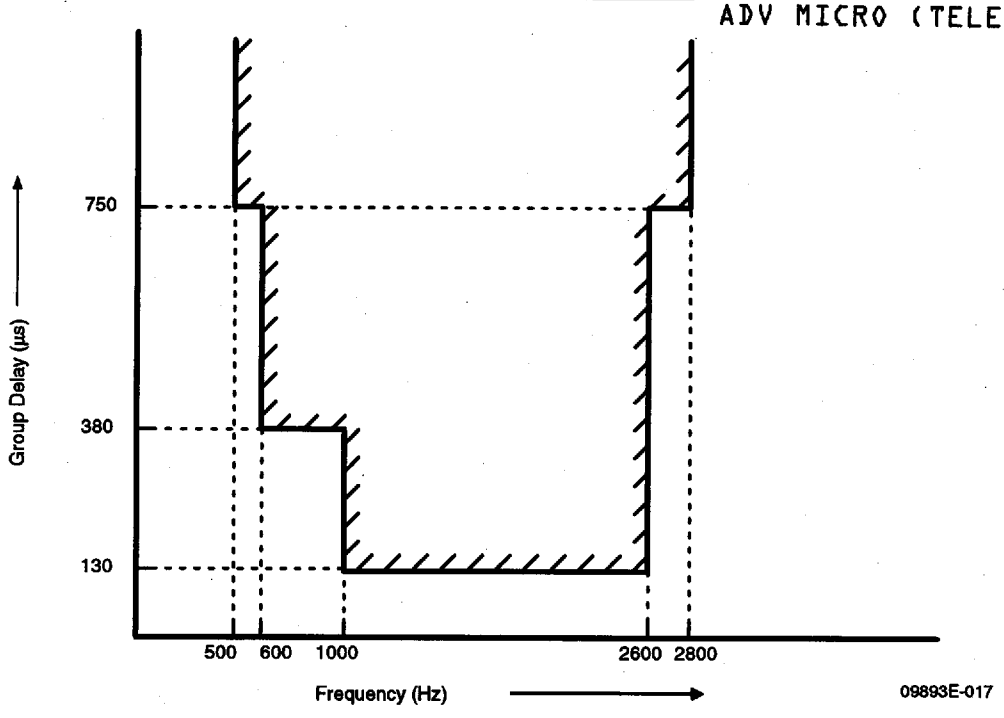


Figure 14. Group Delay Variation with Frequency (Transmit)

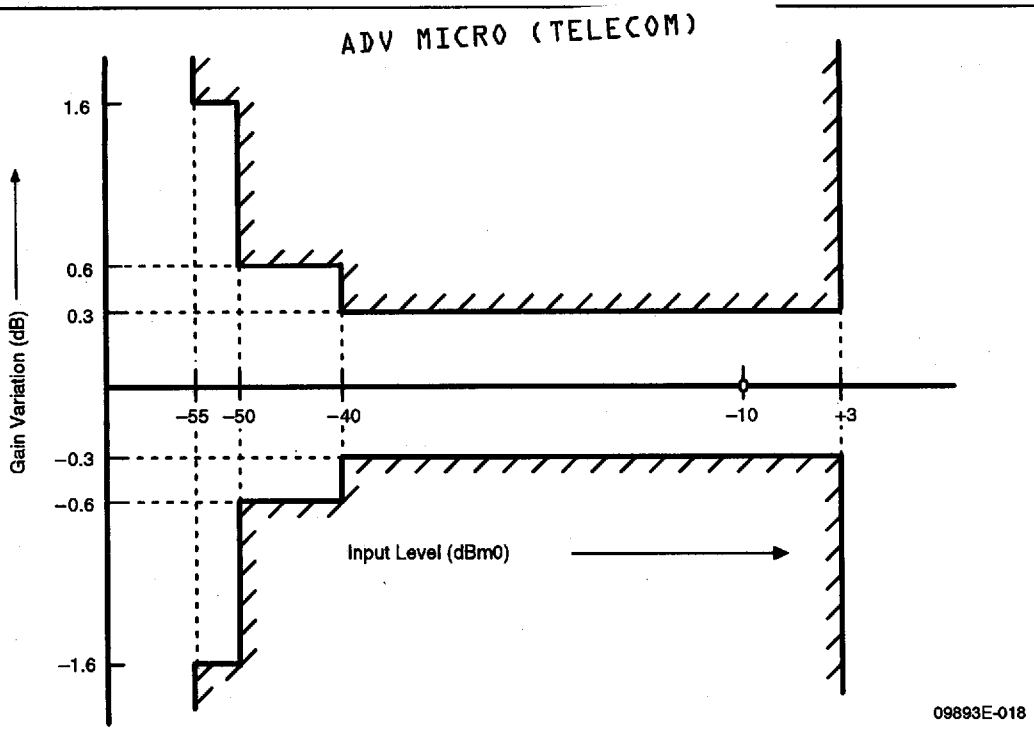


Figure 15. Gain Tracking Error (Transmit) (CCITT Method 2 at 1020 Hz)

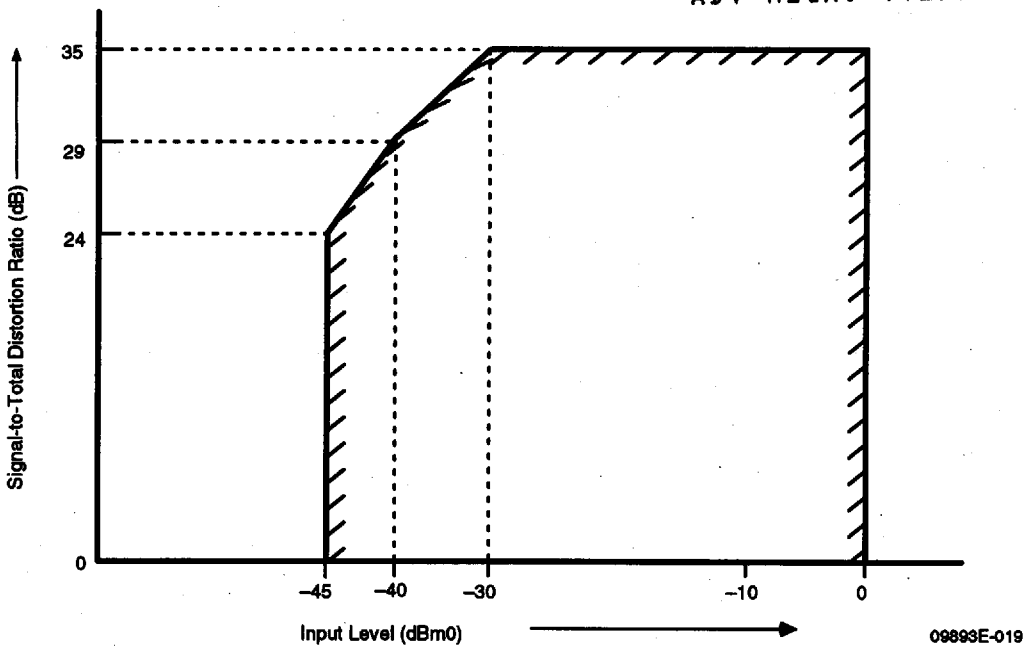


Figure 16. Signal-to-Total Distortion Ratio (Transmit) (CCITT Method 2 at 1020 Hz)

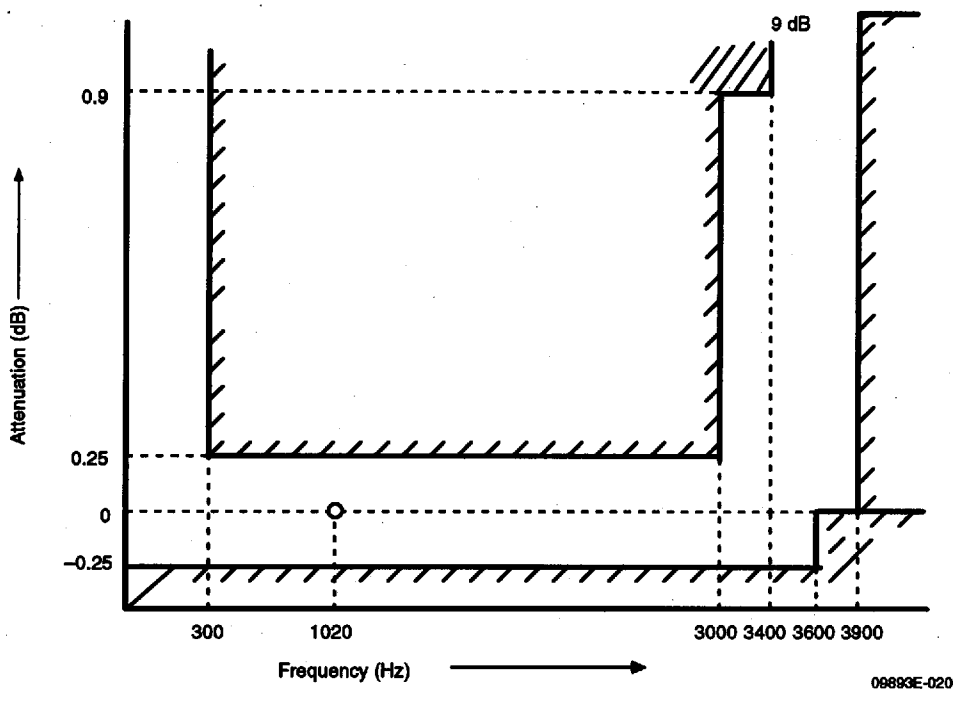


Figure 17. Attenuation/Frequency Distortion (Receive)

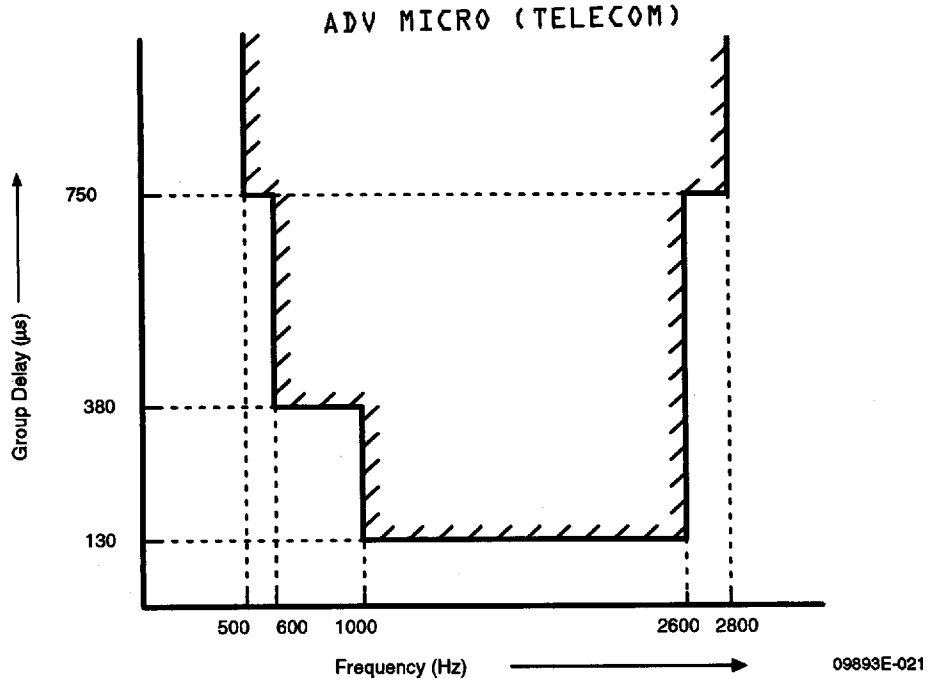


Figure 18. Group Delay Variation with Frequency (Receive)

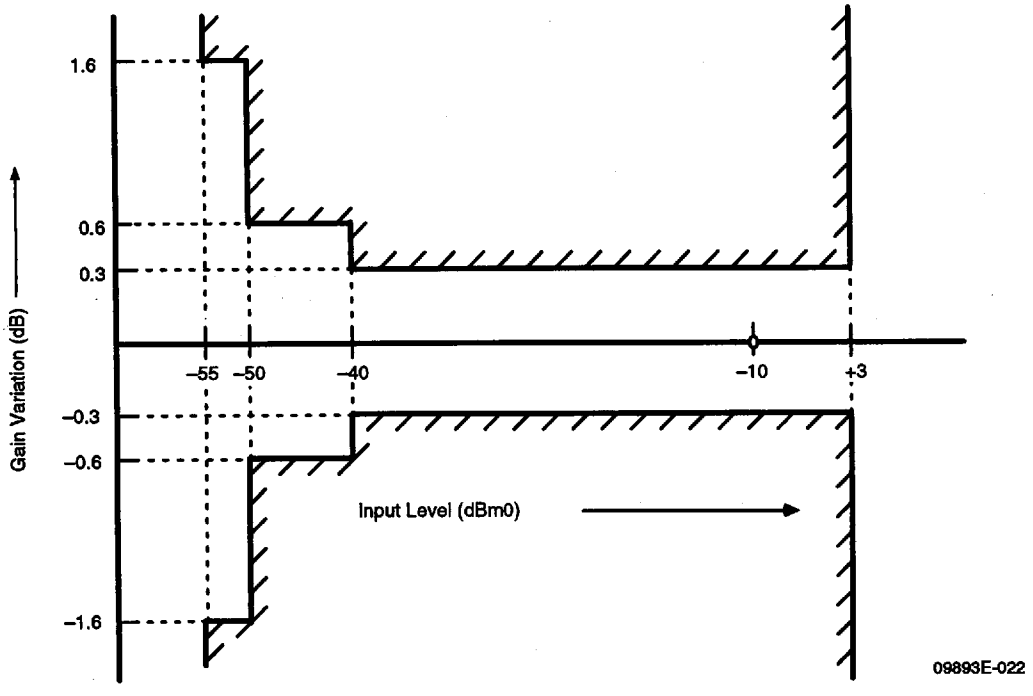


Figure 19. Gain Tracking Error (Receive) (CCITT Method 2 at 1020 Hz)

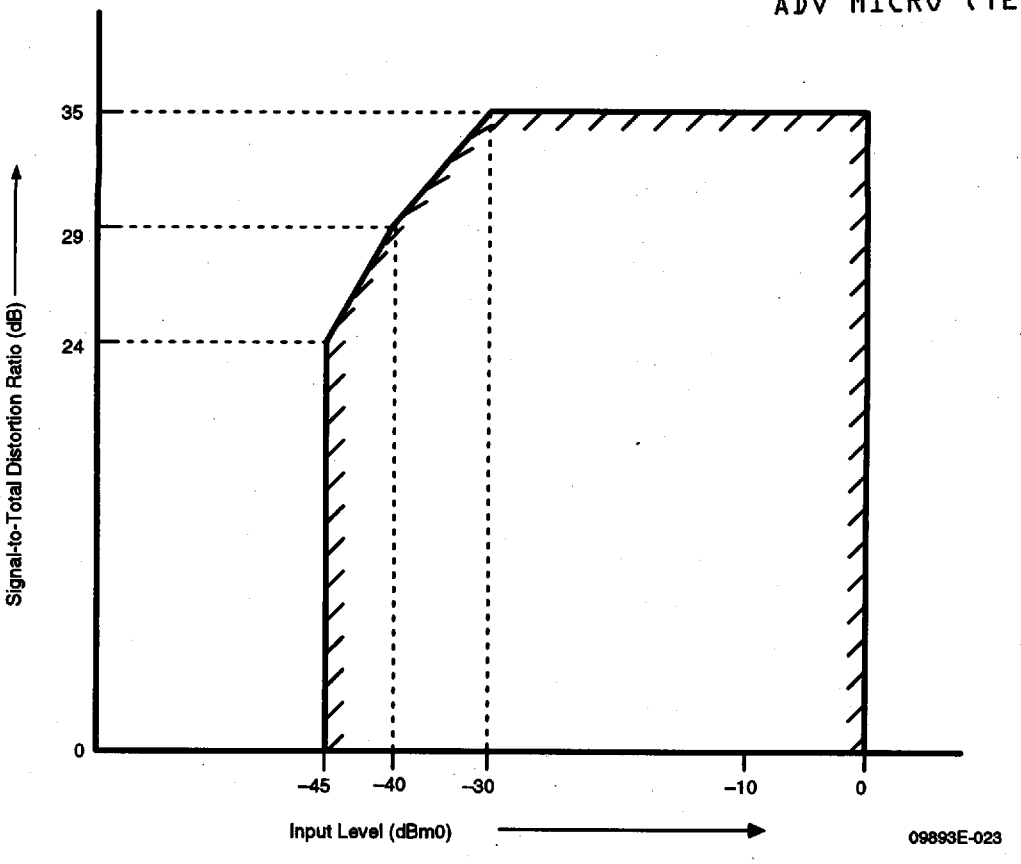


Figure 20. Signal to Total Distortion Ratio (Receive) (CCITT Method 2 at 1020 Hz)

LIU Characteristics

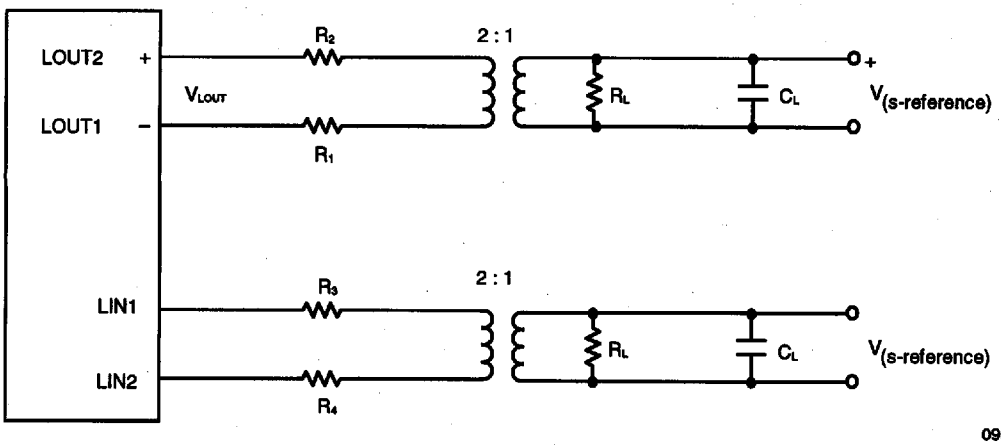
All of the parameters below are measured at the chip terminals and are consistent with 2:1 transformers.

Parameter Symbol	Parameter Descriptions	Preliminary			Unit
		Min	Typ	Max	
V_{LOUT}	Output mark amplitude measured between LOUT2 and LOUT1 (Note 1)	2.210	2.326	2.442	V
V_{LIN}	Receivable input level measured between LIN2 and LIN1, with noise added as specified by CCITT I.430 section 8.6.2.1 (Note 2)	530		1800	mV
Z_{OUT}	Output impedance measured between LOUT2 and LOUT1 spacing condition	20			Kohm
Z_{IN}	Input impedance measured between LIN2 and LIN1	20			Kohm
J	Timing extraction jitter on LOUT	−7		+7	%
PD	Total phase deviation (LOUT with respect to LIN)	−7		+15	%
PU	Pulse unbalanced measured between LOUT2 and LOUT1 (Note 1)	−5		+5	%
PW	Output pulse width measured between LOUT2 and LOUT1 (Note 1)	4.7	5.2	5.7	µs

Note 1. See the equivalent test load circuit and pulse template in Figures 22 and 23.

Note 2. The 530-mV receive input level is equivalent to 9.0 dB of attenuation from a nominal transmit level when measured at the LIN pins. Allowing 0.5-dB loss in the isolation transformer, and 1.0-dB loss in the input isolation resistors, this level will guarantee compliance to the CCITT receiver sensitivity spec of 7.5 dB when measured at the S reference point.

Note 3. Typical receiver performance is 220 mV.



$V_{(S\text{-interface})}$: Transmitter output at the S-interface reference point.
R_L is the termination impedance at the S Interface.
C_L is the effective capacitance at the S Interface.
R_1 and R_2 are the transmitter output series resistors; their value depends upon the characteristics of the pulse transformer (see equations below).
R_3 and R_4 are required for multipoint operation to prevent loading of the line when power is removed from the terminal.

Figure 21. System Interface to LIU

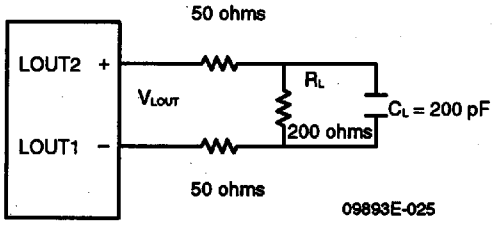


Figure 22. Equivalent Test Load Conditions

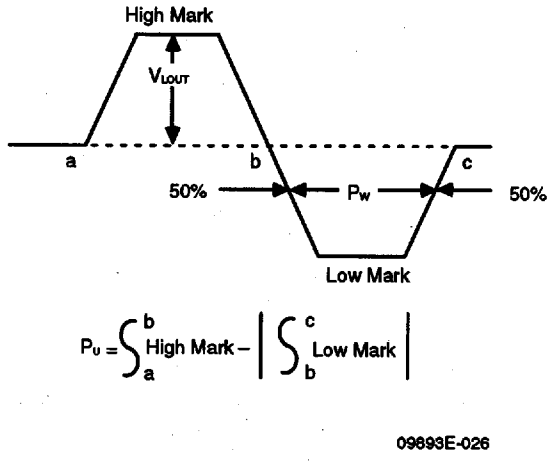
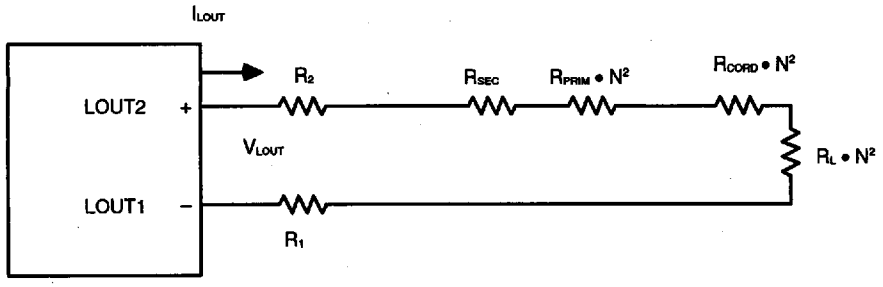


Figure 23. Differential Output Signals Between LOUT2, and LOUT1 (Using the Test Circuit in Figure 23)



RSEC is the DC impedance of the transformer secondary (IC side of transformer).
RPRIM is the DC impedance of the transformer primary (line side of transformer).
RCORD is the DC impedance of the TE connecting cord; typically 4–6 ohms.
N is the transformer turns ratio (N = 2 for Am79C30A/32A).
RL is the S-interface line impedance (50 ohms).
ILOUT is the desired load current for the CCITT transmission templates (7.5 mA for 50-ohm line).
VLOUT is the nominal output voltage from the DSC/IDC line driver.

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Figure 24. Equivalent DC Circuit at LOUT Pins for calculation of R_1 and R_2

Series Resistor Calculations

$$I_{LOUT} = \frac{V_{LOUT}}{R_1 + R_2 + R_{SEC} + (R_{PRIM} \bullet N^2) + (R_L \bullet N^2) + (R_{CORD} \bullet N^2)}$$

$$R_1 + R_2 = \frac{(V_{LOUT})}{(I_{LOUT})} - R_{SEC} - (R_{PRIM} \bullet N^2) - (R_L \bullet N^2) - (R_{CORD} \bullet N^2)$$

Let $R_1 = R_2$

$$R_1 = R_2 = \frac{1}{2}\left\{\frac{V_{LOUT}}{I_{LOUT}} - R_{SEC} - (R_{PRIM} \bullet N^2) - (R_L \bullet N^2) - (R_{CORD} \bullet N^2)\right\}$$

$N = 2$
$R_L = 50$ ohms
$V_{LOUT} = 2.326$ V
$I_{LOUT} = 7.5$ mA

$$R_1 = R_2 = 55.067 - 1/2\ \{R_{SEC} + (4 \bullet R_{PRIM}) + (4 \bullet R_{CORD})\}$$

This equation should be used to determine the value of R_1 and R_2 for the particular transformer used by each customer.

Microprocessor Read/Write Timing

Microprocessor Read Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_{RLRH}	$\overline{RD}$ Pulse Width	200		ns
t_{RHRL}	Read Recovery Time (Notes 1, 2)	200		ns
t_{AVRL}	Address Valid to $\overline{RD}$ Low	20		ns
t_{AHRH}	Address Hold After $\overline{RD}$ High	10		ns
t_{RHCH}	$\overline{RD}$ High to $\overline{CS}$ High (Note 7)	0		ns
t_{RACC}	Read Access Time (Note 3)		80	ns
t_{RHDZ}	$\overline{RD}$ High to Data Hi-Z		50	ns
t_{RDCS}	$\overline{RD}$ Low to $\overline{CS}$ Low (Note 4)		30	ns

Microprocessor Write Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_{WLWH}	$\overline{WR}$ Pulse Width	200		ns
t_{WHWL}	Write Recovery Time (Note 1)	200		ns
t_{AVWL}	Address Valid to $\overline{WR}$ Low	20		ns
t_{AHWH}	Addess Hold After $\overline{WR}$ High (Note 8)	10		ns
t_{WHCH}	$\overline{WR}$ High to $\overline{CS}$ High (Note 7)	0		ns
t_{DSWH}	Data Setup to $\overline{WR}$ High	100		ns
t_{DHWH}	Data Hold After $\overline{WR}$ High	10		ns
t_{WRCS}	$\overline{WR}$ Low to $\overline{CS}$ Low (Note 4)		30	ns

Note 1: The read/write recovery time of 200 ns holds in all cases except when a write command register operation is followed by a read data register operation when accessing the MAP coefficient RAM. This operation requires a minimum recovery time of 450 ns.

Note 2: Successive reads of the D-Channel Receive Buffer require a minimum cycle time (t_{RLRH} + t_{RHRL}) of 480 ns.

Note 3: Read access time is measured from the falling edge of $\overline{CS}$ or the falling edge of $\overline{RD}$, whichever occurs last.

Note 4: $\overline{CS}$ may go Low before either $\overline{RD}$ or $\overline{WR}$ goes Low.

Note 5: In minimal systems, $\overline{CS}$ may be tied Low.

Note 6: Read and write indirect register operations cannot be mixed without at least one write command register operation between them.

Note 7: $\overline{CS}$ may go High before either $\overline{RD}$ or $\overline{WR}$ goes High.

Note 8: If $\overline{CS}$ goes High before $\overline{WR}$ goes High, the minimum Address Hold time becomes 12 ns.

Note 9: $\overline{RD}$ and $\overline{WR}$ pulse width, Address setup and hold, and Data setup and hold timing are measured from the points where both $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ are Low simultaneously.

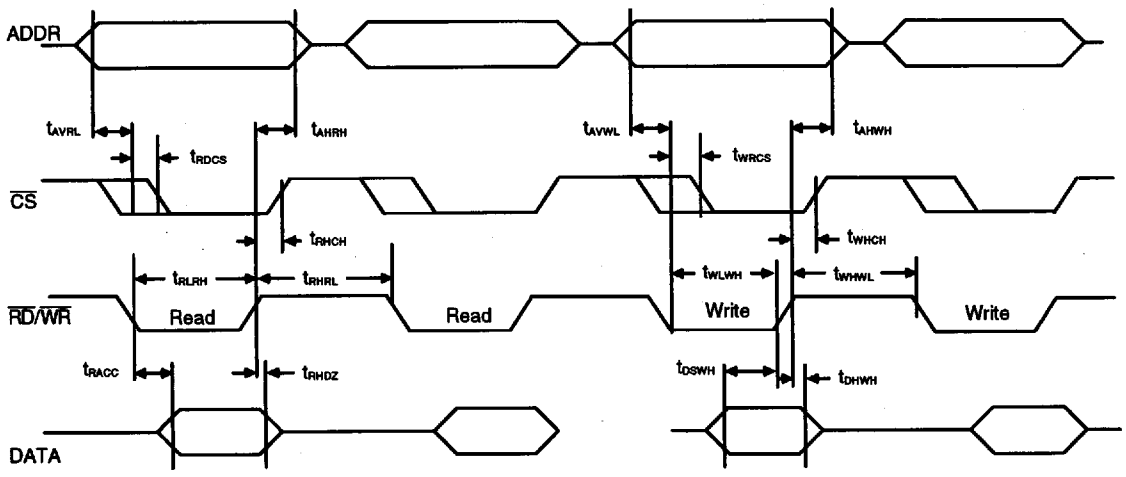

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Figure 25. Microprocessor Read/Write Timing

Interrupt Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_{INTC}	$\overline{INT}$ Cycle Time	125		µs
t_{REC}	$\overline{INT}$ Recovery Time	500		ns

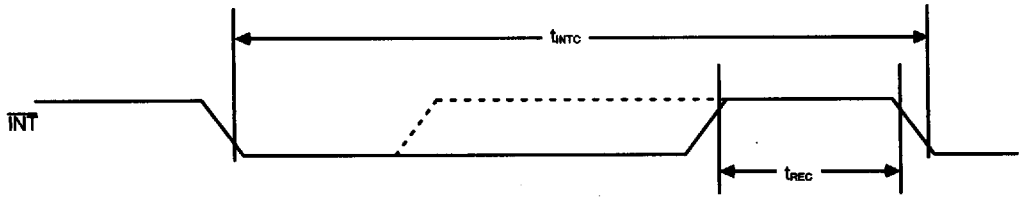

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Figure 26. $\overline{INT}$ Timing

Reset and Hookswitch Timing

Reset Timing

Parameter Symbol	Parameter Description	Min	Max	Units.
t_{RES}	Reset Pulse Width	1		µs
t_{PHRL}	Power Stable to Reset Low	1		µs
t_F	Reset Transition Fall Time		1	ms
t_R	Reset Transition Rise Time		20	µs

Hookswitch Timing

Parameter Symbol	Parameter Description	Min	Max	Units
t_B	Debounce Time	16	16.25	ms
t_1	HSW Detected to $\overline{INT}$ Delay	0	370	µs

Note: Due to clock start-up times, the hookswitch Min and Max Debounce times are approximately 3 ms greater in Power-Down Mode.

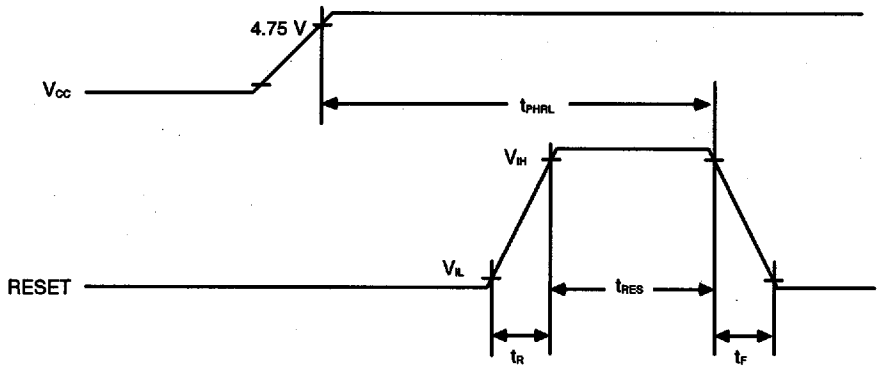

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Figure 27. Reset Timing

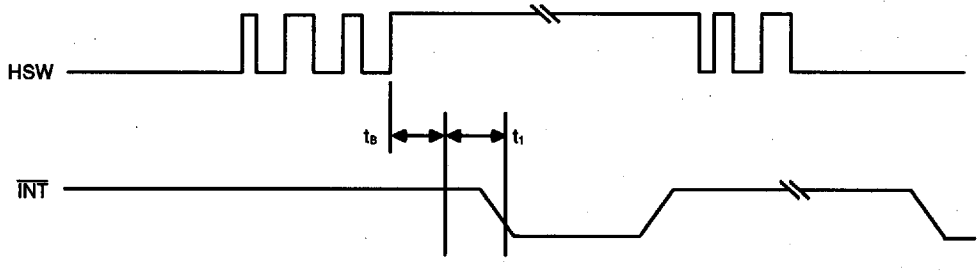

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Figure 28. Hookswitch Debounce Timing

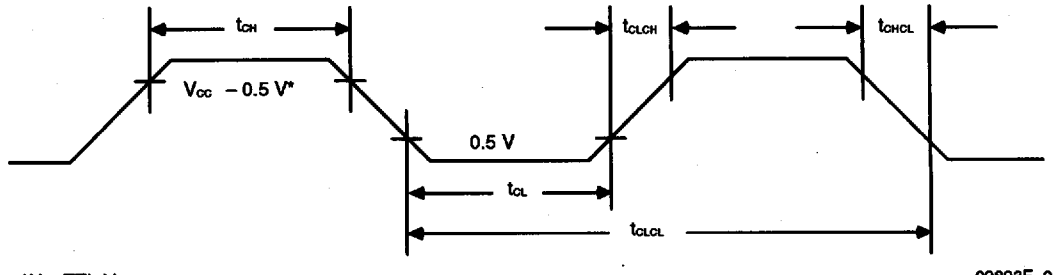
OSC (XTAL2) Timing

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
t_{CLCL}	Oscillator Period		81.374	81.387	ns
t_{CH}	High Time		33		ns
t_{CL}	Low Time		33		ns
t_{CLCH}	Rise Time			10	ns
t_{CHCL}	Fall Time			10	ns

Frequency = 12.288 MHz ±80 ppm.

MCLK Timing

Parameter Symbol	Parameter Description		Test Conditions	Min	Max	Units
t_D	XTAL2 $V_{CC}/2$ to MCLK $V_{CC}/2$		MCLK Load < 80pF		60	ns
t_{RISE1}	Rise Time		MCLK Load < 80pF 0.5 V to (V_{CC}–0.5V)		15	ns
t_{RISE2}	Rise Time		MCLK Load < 40pF 1.0 V to 3.5 V		5	ns
t_{FALL1}	Fall Time		MCLK Load < 80pF (V_{CC}–0.5V) to 0.5 V		15	ns
t_{FALL2}	Fall Time		MCLK Load < 40pF 3.5 V to 1.0 V		5	ns
t_{PWH}	High Pulse Width	12.288 MHz	MCLK Load < 80pF	33		ns
		6.144 MHz		73		ns
		4.069 MHz		114		ns
		3.072 MHz		155		ns
		1.536 MHz		317		ns
		768 kHz		643		ns
		384 kHz		1.294		µs
t_{PWL}	Low Pulse Width	12.288 MHz	MCLK Load < 80pF	33		ns
		6.144 MHz		73		ns
		4.096 MHz		114		ns
		3.072 MHz		155		ns
		1.536 MHz		317		ns
		768 kHz		643		ns
		384 kHz		1.294		µs



*Not TTL V_{IH}

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Figure 29. External Clock Driver (XTAL2) Timing

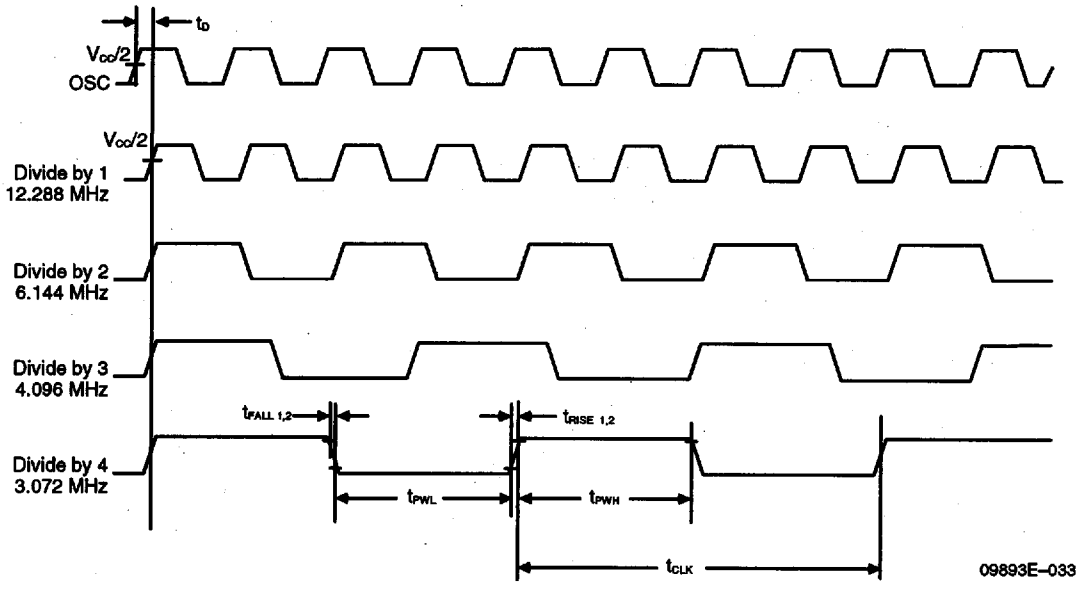
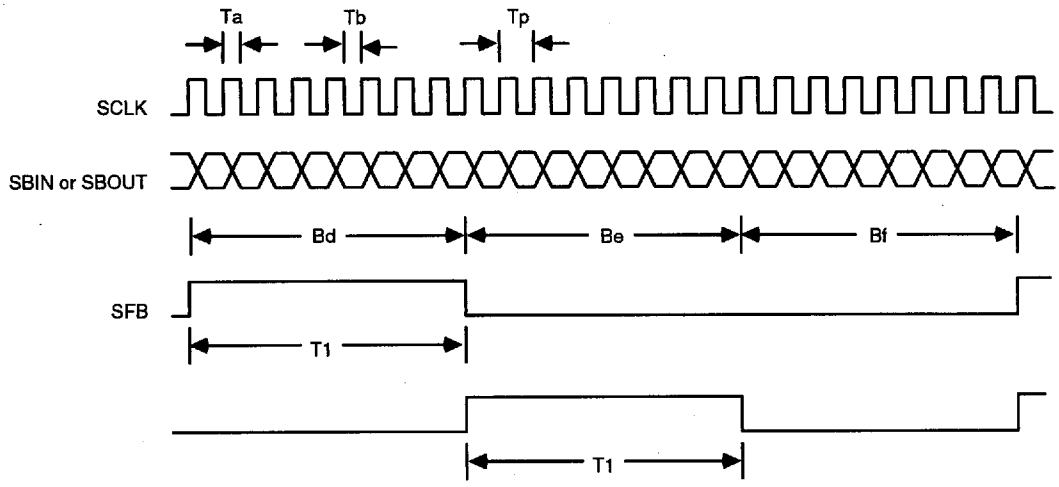


Figure 30. OSC/MCLK Timing

SBP Mode Timing

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Tp*	SCLK		5.025	5.392	µs
Ta	High time		2.594	2.615	µs
Tb*	Low time		2.431	2.777	µs
t_{RISE}	SCLK rise time	SCLK Load < 80pF		20	ns
t_{FALL}	SCLK fall time	SCLK Load < 80pF		20	ns
t_{MCSC}	MCLK to SCLK @6.144 MHz	MCLK Load < 80pF SCLK Load < 80pF		60	ns
t_{CHFS}	SCLK High to frame sync		50	250	ns
t_{CLDO}	SBOUT Data available	SBOUT/SFS Load = 80 pF	50	250	ns
t_{DICH}	SBIN set-up time		200		ns
t_{CHDZ}	SBIN hold time		0		ns

* The frequency of SCLK is f_{XTAL2}/64. Tp and Tb are based on this SCLK frequency, but include a ±163-ns allowance for internal phase lock loop correction.



Notes: 1. For PPCR2(0) = 0, SBIN data is sampled on the rising edge of SCLK, SBOUT data is changed on the falling edge of SCLK.
For PPCR2(0) = 1, SBIN data is sampled on the falling edge of SCLK; SBOUT data is changed on the rising edge of SCLK.
2. T1 width is eight SCLK periods.

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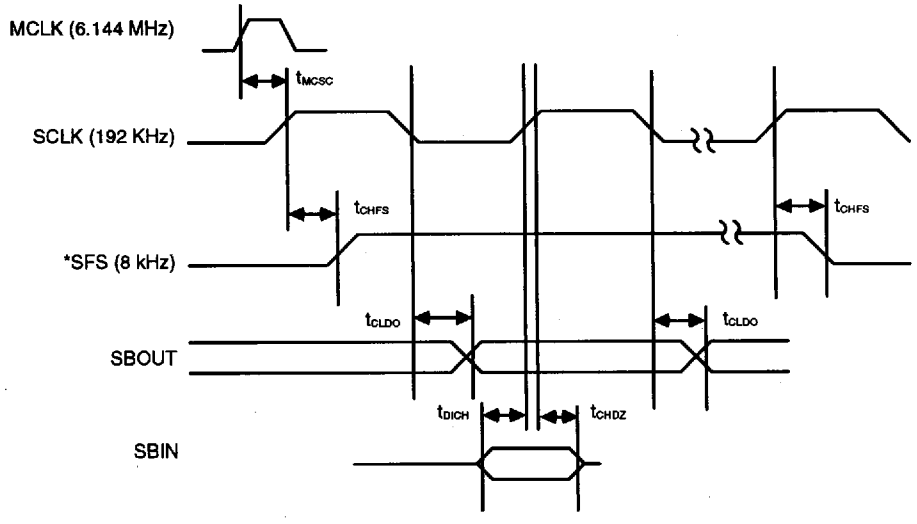
Figure 31. SBP Mode Timing



Note 1. CH2STRB timing is identical to SFS timing, but delayed by eight SCLK cycles.
Note 2. This timing diagram reflects SCLK for PPCR2(0)=0. For PPCR2(0)=1, the diagram is identical except that the SCLK waveform should be inverted.

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Figure 32. SBP Mode MCLK/SCLK/SFS Timing

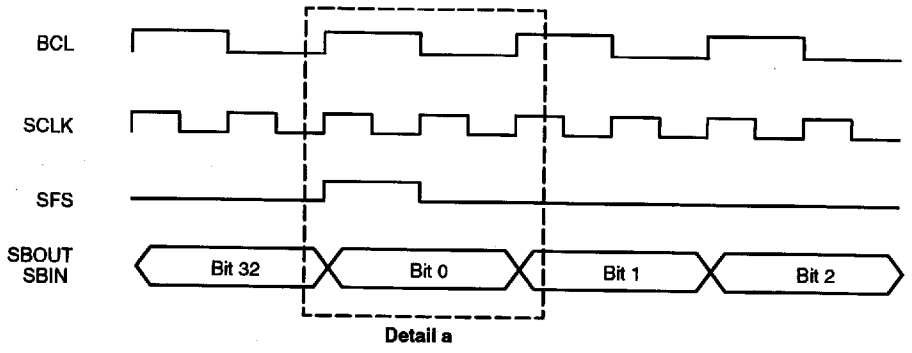
IOM 2 Master Mode Timing

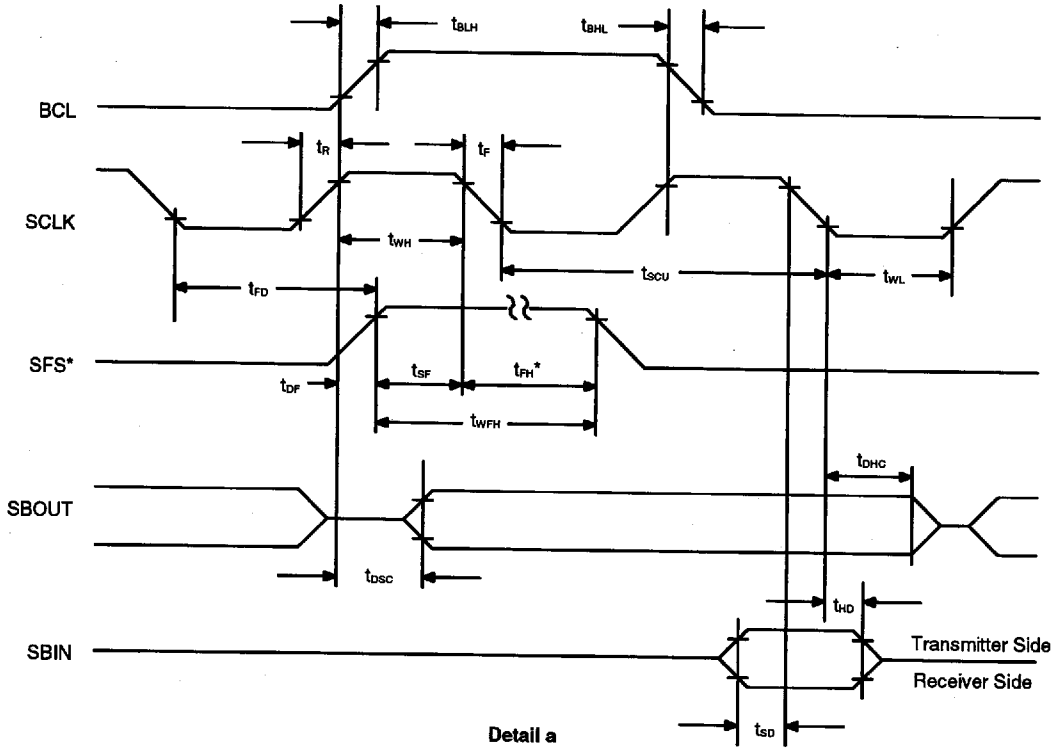
Parameter	Signal	Abbr	Test Condition	Min	Max	Units
Data Clock Rise/Fall	SCLK	t_R, t_F	$C_L = 150$ pF		50	ns
Clock Period	SCLK	t_{SCL}	1.536 MHz ±100 PPM ±163 ns*	487	815	ns
Pulse Width	SCLK	t_{WH}, t_{WL}		260		ns
Frame Sync	SFS	t_R, t_F	$C_L = 150$ pF		50	ns
Frame Sync Setup/Clock	SFS	t_{SF}	$C_L = 150$ pF	50		ns
Frame Sync Delay/Clock	SFS	t_{FD}	$C_L = 150$ pF	0		ns
Frame Sync Hold/Clock	SFS	t_{FH}	$C_L = 150$ pF	50	$t_{WL}+50$	ns
Frame Delay	SFS	t_{DF}	$C_L = 150$ pF	$-t_{WL}$	50	ns
Data Delay/Clock	SBOUT	t_{DSC}	$C_L = 150$ pF		100	ns
Data Hold/Clock	SBOUT	t_{DHC}	$C_L = 150$ pF	70		ns
Data Setup	SBIN	t_{SD}		$t_{WH}+20$		ns
Data Hold	SBIN	t_{HD}		50		ns

IOM 2 Slave Mode Timing

Parameter	Signal	Abbr	Min	Max	Units
Data Clock Rise/Fall	SCLK	t_R, t_F		60	ns
Clock Frequency (1/period)	SCLK	$1/t_{SCLK}$	1.536 MHz ±100 PPM ±163 ns*		Hz
Clock Delay High/Low	BCL	t_{BLH}, t_{BHL}		30	ns
Pulse Width	SCLK	t_{WH}, t_{WL}	240		ns
Frame Sync Rise/Fall	SFS	t_R, t_F		60	ns
Frame Set-up	SFS	t_{SF}	70		ns
Frame Hold/Clock	SFS	t_{FH}	20		ns
Frame Delay/Clock	SFS	t_{FD}	0		ns
Frame Width High	SFS	t_{WFH}	130		ns
Frame Width Low	SFS	t_{WFL}	t_{SCLK}		ns
Data Delay/Clock	SBOUT	t_{DSC}		100**	ns
Data Hold/Clock	SBOUT	t_{DHC}	70		ns
Data Set-up	SBIN	t_{SD}	$t_{WH}+20$		ns
Data Hold	SBIN	t_{HD}	50		ns

*The ±163-ns value can occur once per frame for digital phase lock loop correction.
**$C_L = 150$ pF





* In Master Mode, SFS is 16 SCLK cycles + set-up time + hold time in length

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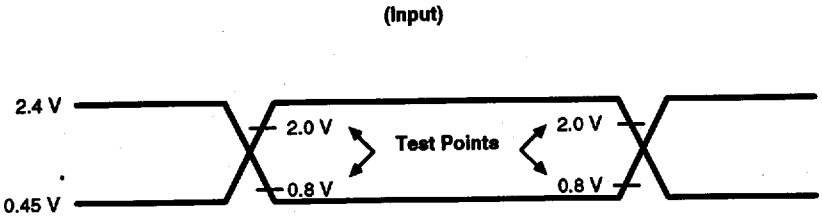
Figure 33. IOM 2 Timing

Switching Test Conditions



Note: AC testing inputs are driven at 2.4 V for a logical 1, and 0.45 V for a logical 0. Timing measurements are made at 2.0 V and 0.8 V for a logical 1, and a logical 0, respectively.

Figure 34. Switching Test Input/Output Waveform

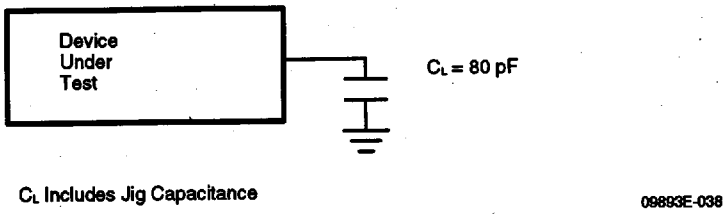


Figure 35. Switching Test Load Circuit

KEY DESIGN HINTS FOR THE DSC/IDC CIRCUIT

Due to the high level of integration of the Am79C30A/32A DSC/IDC circuit, it is easy to overlook important design information when reading the data sheet. The following list of key design hints has been compiled to streamline the design process. A comprehensive series of ISDN application notes and tutorials is available from Advanced Micro Devices; please contact an AMD sales office or factory for current information.

- The AREF pin *must* be used to bias the AINA and AINB inputs. There is a datasheet parameter, Vios, which states that the analog inputs must be biased to within 5 mV of AREF. AREF is *nominally* 2.4 V; normal device-to-device variation will exceed the 5-mV Vios specification. If a voltage other than AREF is used, transmission performance at very low signal levels will be degraded.
- The recommended method of biasing the AINA and AINB inputs is to use a 15–100 Kohm resistor between the input and AREF. The signal source should be AC-coupled to the analog input. Take care that the RC formed by the biasing resistor and blocking capacitor does not distort the input signal.
- The AREF output must not be loaded with a capacitor, since it may cause the internal buffer amplifier to become unstable. For some applications involving significant gain external to the DSC circuit, the AREF output may require a simple RC noise filter. In this case, the AREF output should be isolated from the capacitor by a resistance of greater than 1 Kohm to ensure stability.
- The analog gain selection value (in MMR3) should be written before the MAP is enabled.
- The MAP auto-zero function (MMR2) should be enabled before the MAP is enabled.
- The DSC/IDC circuit should be provided with decoupling capacitors, situated as close as possible to the package power leads. In general, 0.1-µF ceramic capacitors are sufficient, but bulk decoupling capacitors will be required if the LS1 and LS2 loudspeaker outputs are driving a heavy load.
- The DSC/IDC circuit is constructed on a single substrate, and therefore the device power pins must not be from separate supplies. If there is a DC offset between the analog and digital power-supply pins, excessive current may flow through the device substrate.
- The LS1, LS2, EAR1, and EAR2 outputs are intended to be used differentially. Although it is possible to use only a single output, the rejection of power-supply noise and internal digital noise is improved if the outputs are used differentially.
- Be certain to observe the maximum loading specification for the LS and EAR outputs. When used differentially, the EAR outputs must see a minimum of 540 ohms between them. Similarly, the LS outputs must see a minimum of 40 ohms. The maximum capacitive loading in either case is 100 pF.
- The LS and EAR outputs need not be matched to the load. The LS and EAR outputs are voltage drivers, and do not assume the presence of any particular load impedance. If the maximum loading specification is met, the LS and EAR outputs will function satisfactorily. In some cases, an external resistor may be used to center the desired output volume—for instance, while driving a 150-ohms earpiece with the EAR outputs.
- If using an EAR or LS output in a single-ended fashion, AC-couple the pin to the load. If not, the excessive DC current will cause signal distortion.
- When using programmable gains and filters in the MAP, consider the dynamic range effects such as truncation error and clipping. In case of questions in any particular application, please contact the AMD applications staff for assistance.
- All MAP tone generators are referenced with respect to the +3-dBm0 overload voltage—that is, a 0-dB tone yields a +3-dBm0 output. Take care to avoid clipping when adding tones to signals as, for example, when generating DTMF waveforms.
- The RC connected to CAP1/CAP2 must be situated as close as possible to the DSC circuit package to reduce the amount of noise coupled in from other signal traces.
- Observe the XTAL2 frequency accuracy requirement of 12.288 MHz ± 80 ppm. Since crystals from different manufacturers will vary, the DSC circuit oscillator output frequency at the MCLK pin must be measured and, if necessary, the value of the crystal load capacitors should be adjusted as part of the initial design procedure. An application note of oscillator considerations is available from AMD (ISDN System Engineering Application Note, order #12557).
- If driving the XTAL2 pin with the external oscillator, it is necessary to observe the datasheet input voltage and rise/fall time requirements. Note that the XTAL2 levels are not TTL-compatible.
- Take care in board layout of the DSC circuit, as with any sensitive analog device. An application note of DSC circuit board layout hints is available from AMD (ISDN Systems Engineering Application Note, order #12557).
- The sidetone path defaults to –18-dB attenuation. If disabling the sidetone path is desired, the sidetone block must be enabled and programmed for infinite attenuation.
- Consider the LIU transformers, series resistors, and IC LIU output drivers as a functional unit. Transformers that meet CCITT I.430 requirements with other

transceivers are not necessarily appropriate for use with the DSC circuit, and vice versa.

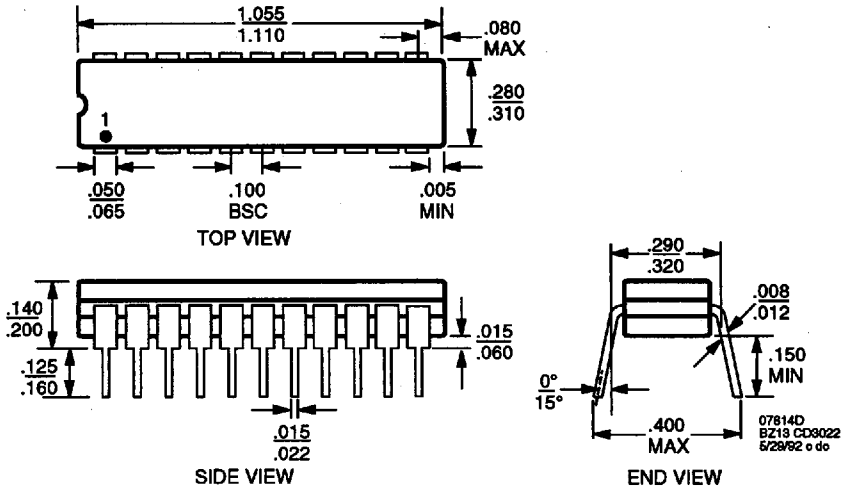
- Interrupts should be masked when reading or writing any indirect or multibyte DSC circuit registers to prevent the possibility of an interrupt occurring and destroying the contents of the Command Register.
- If the MAP and secondary tone ringer are disabled, the EAR, AREF, and LS outputs are high-impedance. If the MAP is enabled, the unselected audio output is high-impedance.
- The MAP should not be enabled until after the LIU has achieved synchronization. This will eliminate the possibility of audible distortion when the internal device timing is re-synchronized to the S Interface.
- To make optimum use of the MAP digital signal processsing chain, use digital gain (GX) for fine adjustment, and analog gain (GA) for coarse adjustment.
- The user must program the Secondary Tone Ringer Frequency Register (STFR) with a legal value *before* enabling the secondary tone ringer.
- In order to exit Power-Down Mode due to LIU activation, *both* the F7 interrupt and the DSC/IDC circuit interrupt pin must be enabled. In order to exit Power-Down Mode due to IOM 2 activation, *both* the IOM 2 Timing Request interrupt and the DSC/IDC circuit interrupt pin must be enabled.
- The MAP auto-zero function must be enabled *prior* to enabling the MAP. For all normal applications, the auto-zero function should always be enabled.
- To ensure proper operation of the filters (X and R) and gains (GX, GR, GER, STGR, and ATGR), these register blocks should not be accessed more frequently than 128-µs intervals. This allows the internal buffers to the map to operate properly since they are updated only once per frame.

PHYSICAL DIMENSIONS

Preliminary; package in development. BSC is an ANSI standard for Basic Space Centering. Dimensions are measured in inches or millimeters.

T-90-20

CD022



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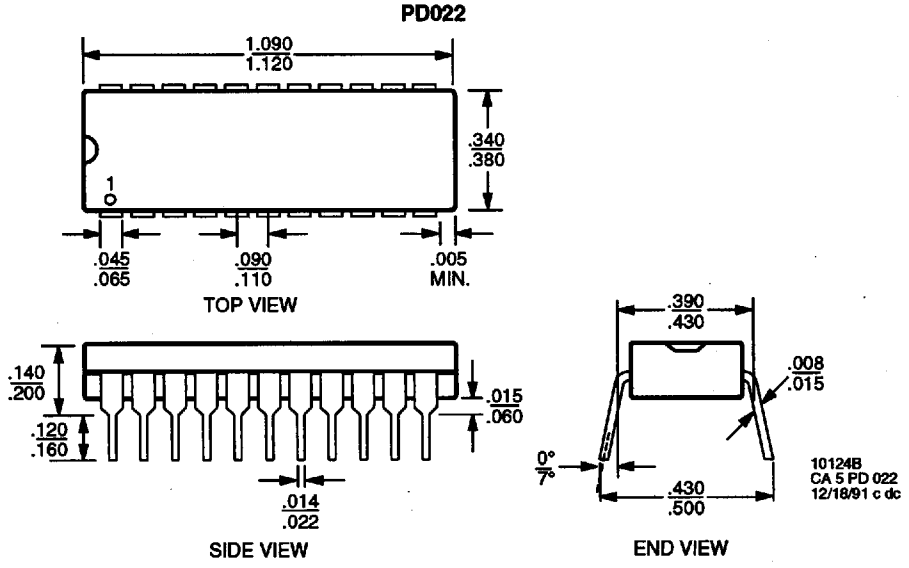

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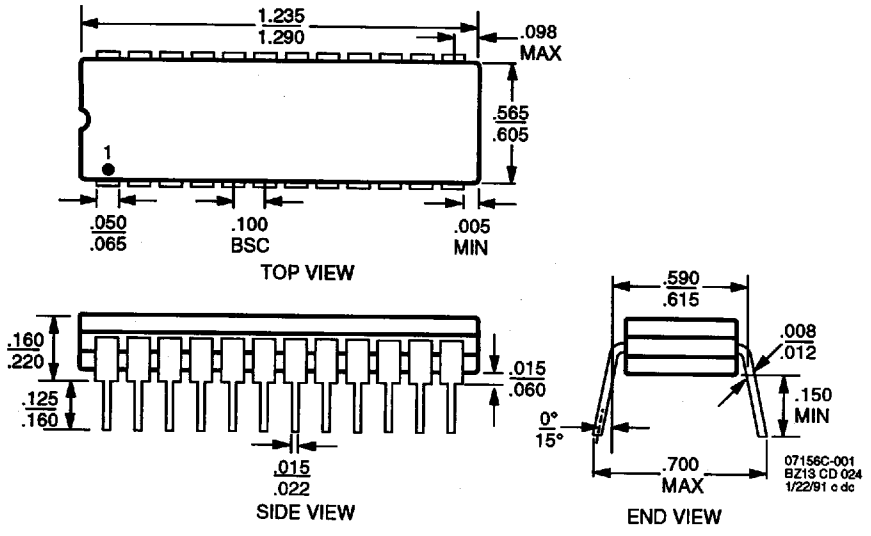
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.015
.022
SIDE VIEW
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.615
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1/22/91 c dc

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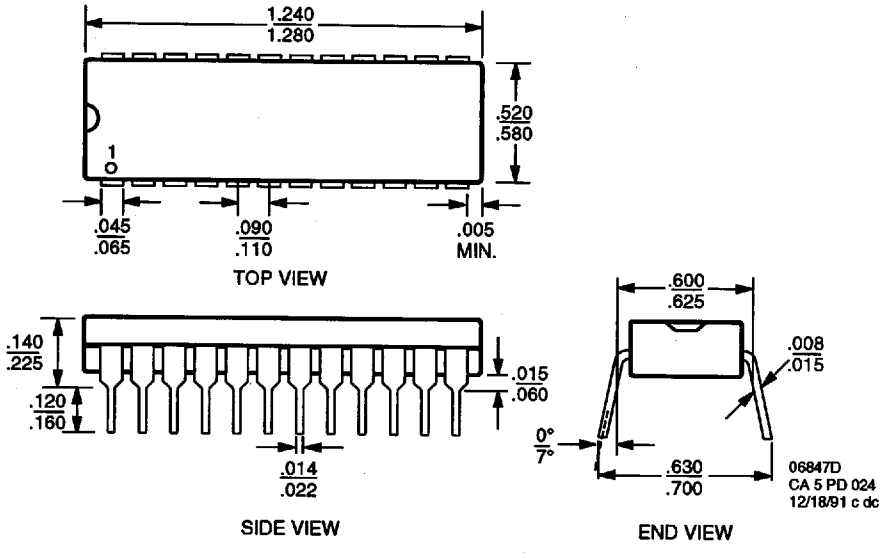
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SIDE VIEW
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12/18/91 c dc

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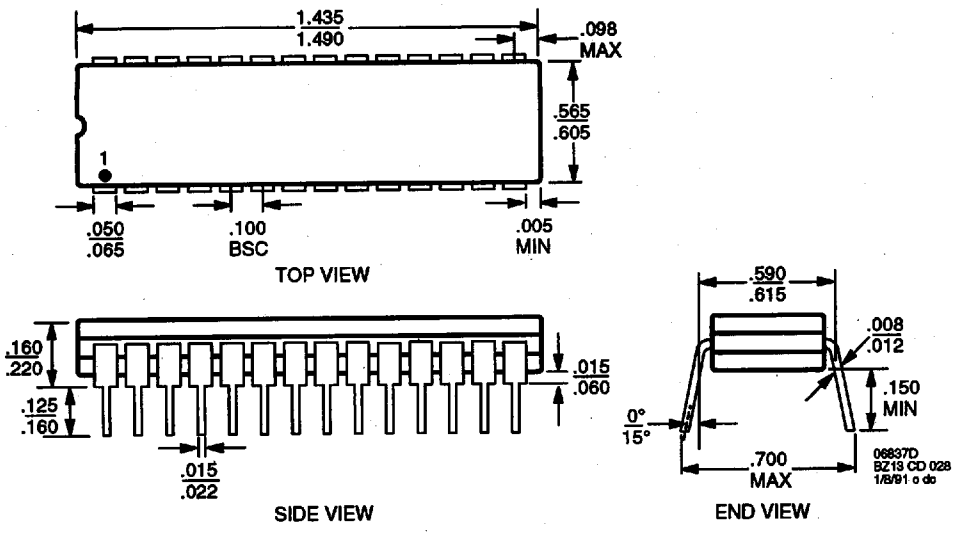
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.022
SIDE VIEW
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MAX
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06837D
BZ13 CD 028
1/8/91 o dc

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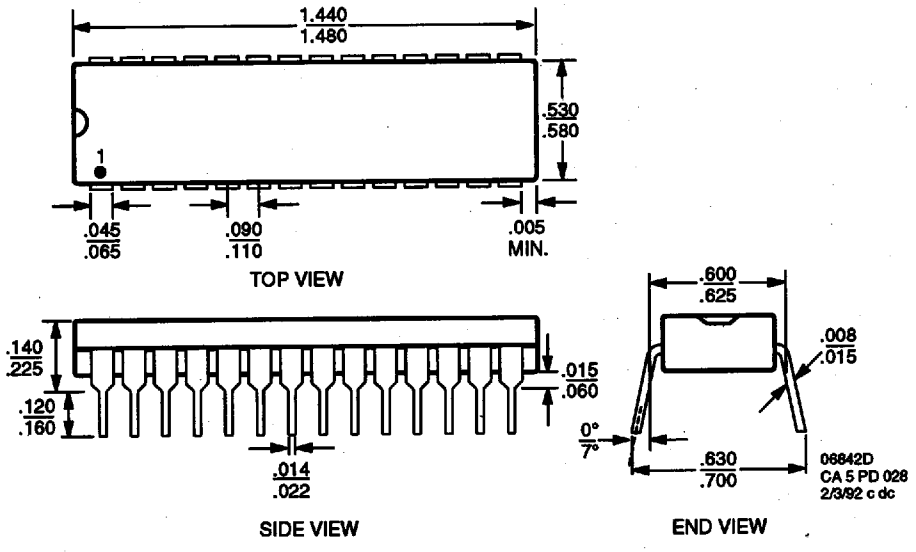
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SIDE VIEW
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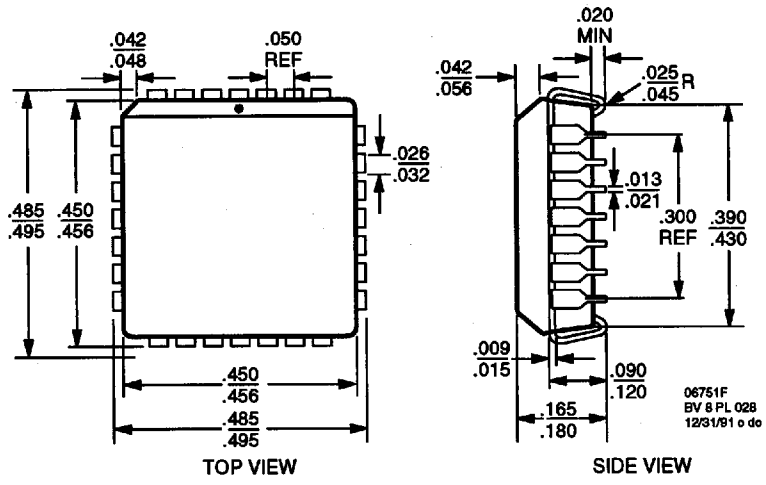
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SIDE VIEW

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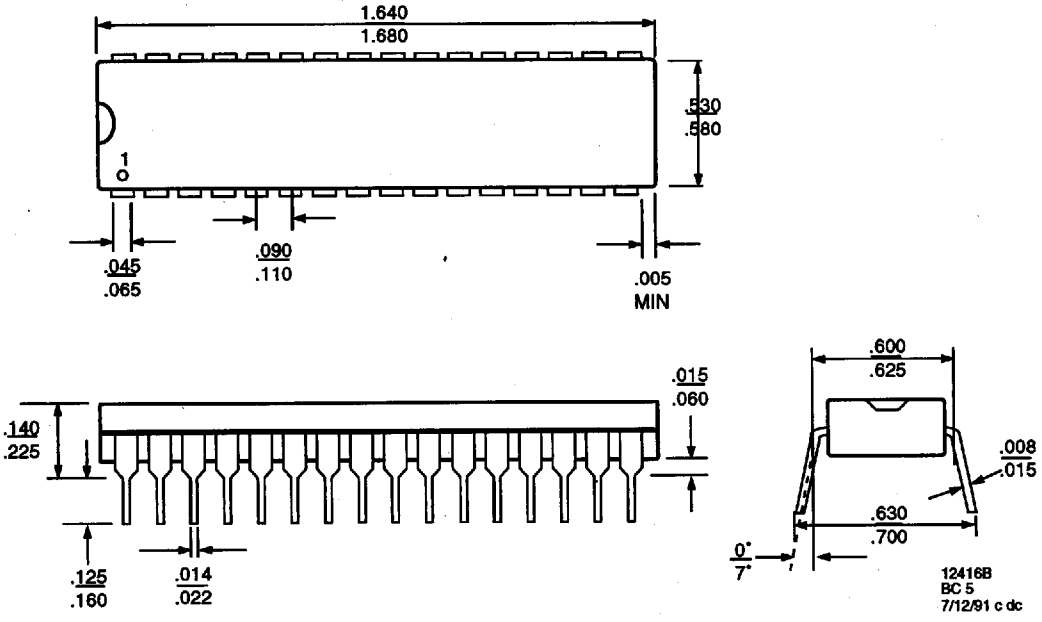
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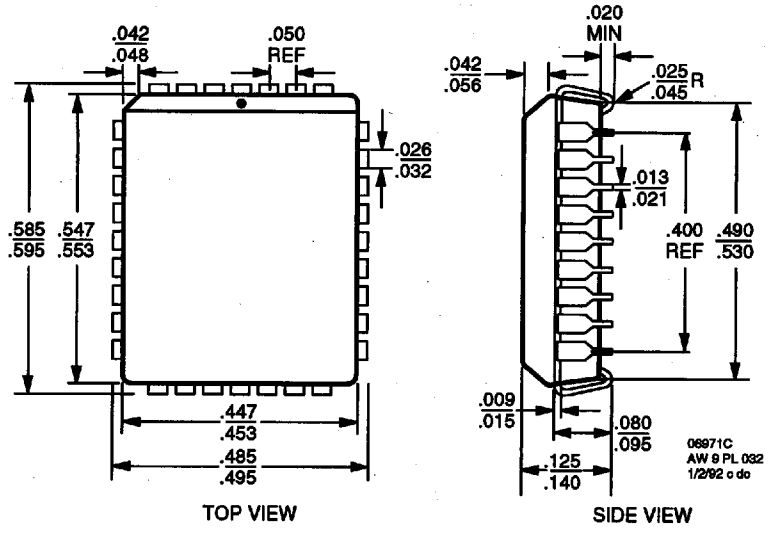
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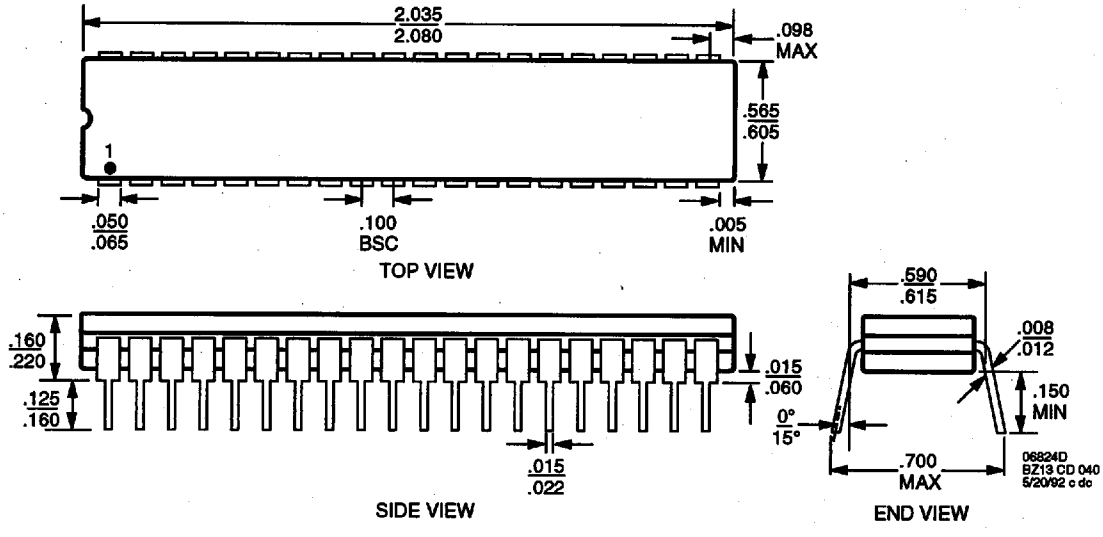
CD040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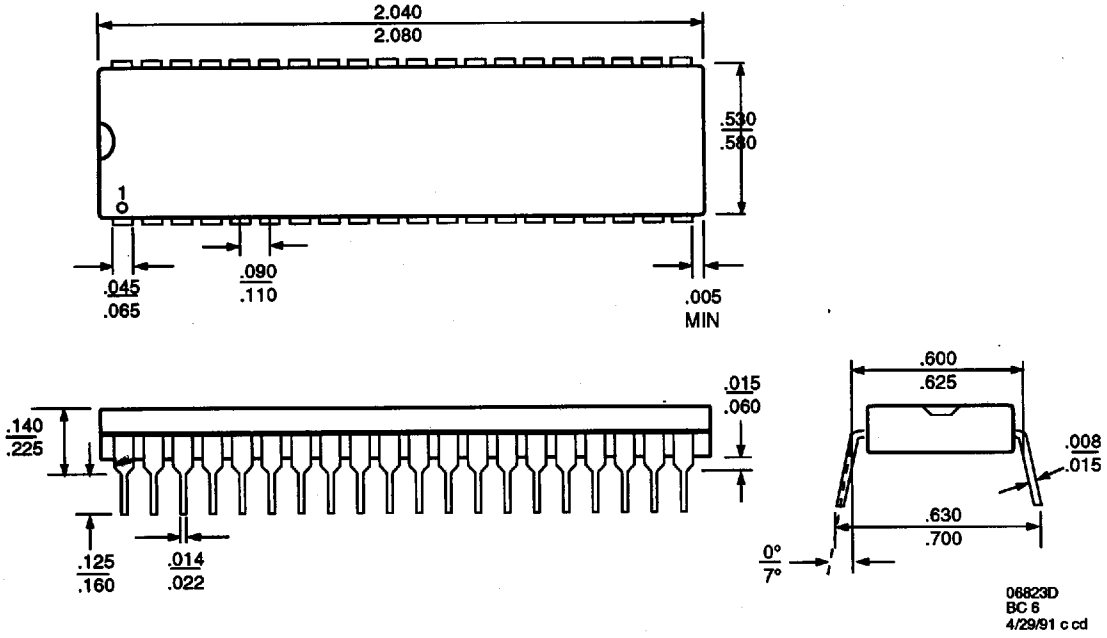
END VIEW

PD 040



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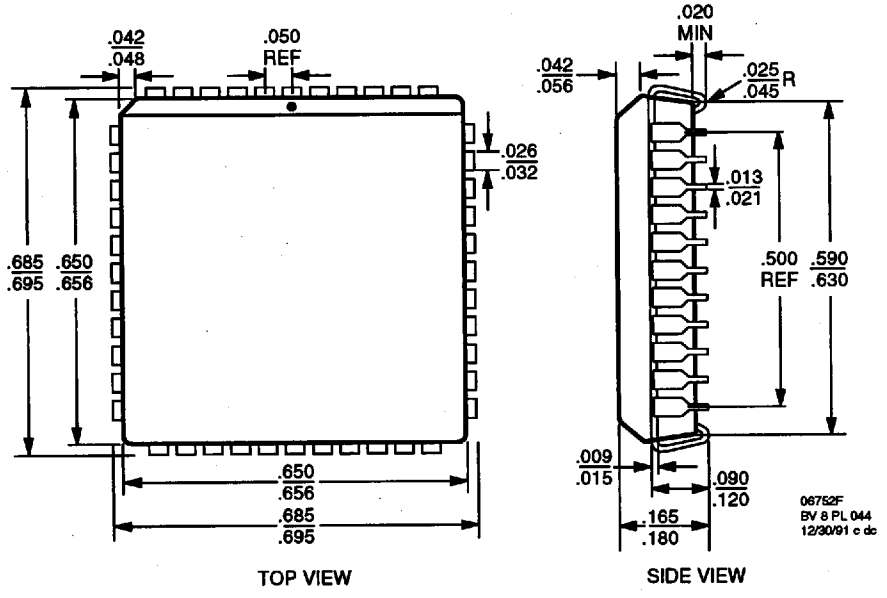

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